Stacked-NMOS Triggered Silicon-Controlled Rectifier for ESD Protection in High/Low-Voltage-Tolerant I/O Interface

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***Abstract*—A stacked-NMOS triggered silicon-controlled rectifier (SNTSCR) is proposed as the electrostatic discharge (ESD) clamp device to protect the mixed-voltage I/O buffers of CMOS ICs. This SNTSCR device is fully compatible to general CMOS processes without using the thick gate oxide to overcome the gate-oxide reliability issue. ESD robustness of the proposed SNTSCR device with different layout parameters has been investigated in a 0.35-μm CMOS process. The HBM ESD level of the mixed-voltage I/O buffer with the stacked-NMOS channel width of 120 μm can be obviously improved from the original $\sim$ 2 kV to be greater than 8 kV by this SNTSCR device with a device dimension of only $60\ \mu\text{m}/0.35\ \mu\text{m}$.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, mixed-voltage I/O buffer, silicon-controlled rectifier (SCR).**

I. Introduction

With THE mix of power supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3]. To solve the gate-oxide reliability issue without using the additional thick gate oxide process [4], the stacked-MOS configuration had been widely used in the mixed-voltage I/O buffers [5]–[7]. In such mixed-voltage I/O circuits, the pull-up PMOS, connected from the I/O pad to VDD power line, has the self-biased circuits for tracking its gate and n-well voltages. There is no any parasitic diode connected from the pad to VDD power line to avoid the leakage current path through the output PMOS, when the high-voltage input signals enter to the I/O pad. Because of the limitation of placing a diode from the pad to VDD in the mixed-voltage I/O circuits, the positive-to-VSS ESD voltage zapping on the I/O pad cannot be diverted from the pad to VDD power line and cannot be discharged through the additional power-rail (VDD-to-VSS) ESD clamp circuit [8]. Such positive-to-VSS ESD current on the I/O pad is totally discharged through the stacked NMOS in the snapback breakdown condition. The ESD robustness of the stacked NMOS in mixed-voltage I/O with different layout style and circuit design had been reported in [9]. From the measured results in [9], the NMOS in stacked configuration has a higher trigger voltage ($Vt1$), a higher snapback holding voltage (Vsb), and a lower secondary breakdown current ($It2$) compared to the single NMOS. Therefore, such mixed-voltage I/O circuits with stacked NMOS often have much lower ESD level, as compared to the I/O circuits with a single NMOS under the positive-to-VSS ESD stress condition. Without the gate oxide in the device structure to avoid the gate-oxide reliability issue, the field-oxide device (FOD) had been often used as the ESD protection device in CMOS ICs. However, the process migration to shallow trench isolation (STI) increases the snapback trigger voltage of such FOD devices to become greater than that of the stacked NMOS in the mixed-voltage I/O circuits [9]. Thus, the FOD devices are no longer effective to protect the mixed-voltage I/O circuits in the deep-submicron CMOS processes.

To sustain a high ESD level within a much smaller silicon area, the low-voltage-triggering SCR (LVTSCR) device [10] had been reported as one of the most effective ESD clamp devices in CMOS ICs. But, such an LVTSCR device cannot be directly applied to protect the mixed-voltage I/O buffers due to the gate-oxide reliability issue on the thin-oxide NMOS, if the inserted NMOS has no thick gate oxide. In this letter, a new ESD protection device, the stacked-NMOS triggered SCR device (SNTSCR), is proposed to significantly improve ESD robustness of the mixed-voltage I/O buffers without using the thick gate oxide. This SNTSCR device is fully process-compatible for general CMOS processes without causing the gate-oxide reliability problem. The current–voltage (I-V) characteristics and ESD robustness of the proposed SNTSCR device under different gate biases and layout parameters are investigated in details.

II. Stacked-NMOS Triggered Silicon-Controlled Rectifier

The cross-sectional view and layout of the stacked-NMOS triggered silicon-controlled rectifier (SNTSCR) device are shown in Fig. 1(a) and (b), respectively. This SNTSCR can be realized in general CMOS processes without any extra process modification. The SNTSCR device is disposed on the bond pad to protect the mixed-voltage I/O circuits from ESD damage.

In the SNTSCR device, two NMOS transistors (Mn1 and Mn2) are stacked in the cascoded configuration, where the drain of Mn1 is across the junction between an N-well region and

Manuscript received January 22, 2002; revised April 8, 2002. This work was supported in part by the National Science Council of Taiwan, R.O.C., and the Industrial Technology Research Institute, Taiwan. The review of this letter was arranged by Editor S. Kawamura.

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Publisher Item Identifier S 0741-3106(02)05343-0.

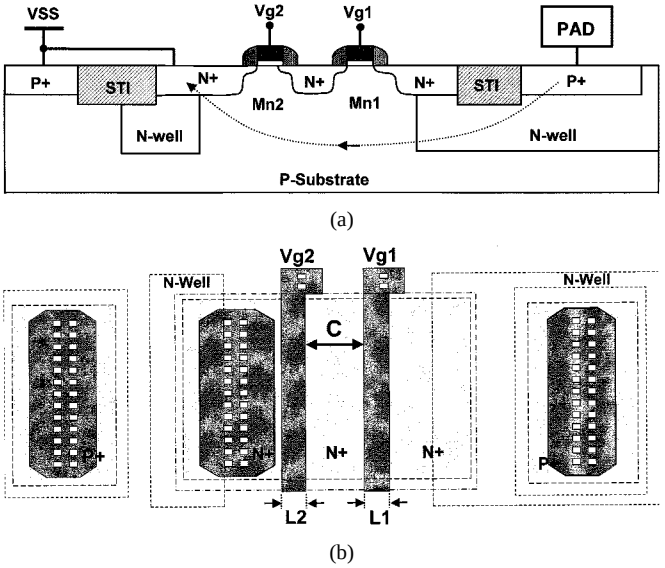


Fig. 1. (a) Cross-sectional view and (b) the corresponding layout pattern of the proposed SNTSCR device in a p-substrate CMOS process.

the p-substrate. The p^+ diffusion, N-well, p-substrate and n^+ diffusion to form a lateral SCR device between the I/O pad and VSS is indicated by the dashed line in Fig. 1(a). The purpose of Mn1 and Mn2 connected in stacked configuration is to sustain the high voltage level of input signals without causing gate oxide reliability issue in the SNTSCR device under the normal circuit operating condition. If only single NMOS is inserted in the lateral SCR device, such as the traditional LVTSCR [10], the voltage across gate oxide will be greater than VDD when a high-voltage signal enters into the I/O pad. This causes the gate oxide reliability issue on the traditional LVTSCR for long-time operation. During ESD stress condition, Mn1 and Mn2 are both turned on by suitable gate-biased design to trigger the lateral SCR on for discharging ESD current. Without using the thick gate oxide in CMOS process, the proposed SNTSCR device has no gate-oxide reliability issue for using to protect the mixed-voltage I/O circuits.

III. Experimental Results

To investigate the characteristics of the SNTSCR device, three layout parameters [C, $L1$ and $L2$ shown in Fig. 1(b)] of the layout pattern are adjusted. C is the poly-to-poly spacing across the center common n^+ diffusion. $L1$ and $L2$ are the channel lengths of the Mn1 and Mn2, respectively. Such SNTSCR devices with different layout parameters but with a fixed channel width of 60 μm have been fabricated in a 0.35-μm CMOS process.

The current–voltage I–V characteristics of the SNTSCR device with $C = 0.5\,\mu$m and $L1 = L2 = 0.35\,\mu$m under different gate biases of V_g1 and V_g2 are measured in Fig. 2. The trigger voltage (Vt) of the SNTSCR device decreases from 10 V to 6 V, when the gate bias increases from $V_g1 = Vg2 = 0$ V to $V_g1 = V_g2 = 0.5$ V. As $V_g1 = V_g2 > 0.6$ V, both the Mn1 and Mn2 are turned on to trigger SNTSCR on, therefore the V_t decreases to around $1 \sim 2$ V.

The impacts of layout parameters on V_t of the SNTSCR device are measured and compared in Fig. 3(a) and (b), under different gate biases ($V_g1 = V_g2$). In Fig. 3(a), the $L1$ and $L2$ are fixed at 0.35 μm, but the spacing C is changed. The shorter spacing C causes a lower trigger voltage on the SNTSCR device. In Fig. 3(b), the spacing C is fixed at 0.5 μm, but the $L1$ and $L2$ are changed. The shorter $L1$ and $L2$ channel lengths

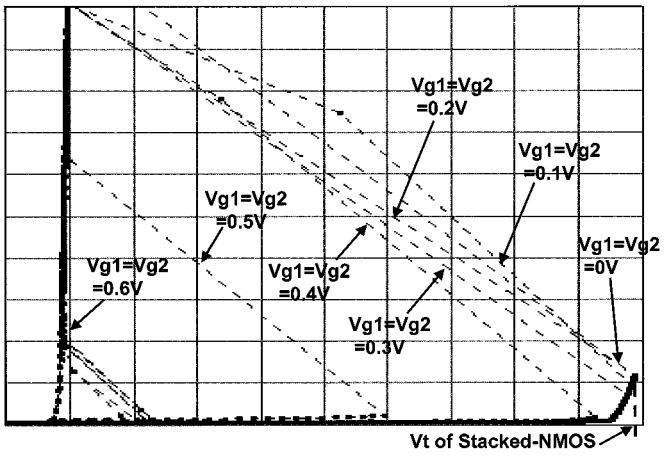
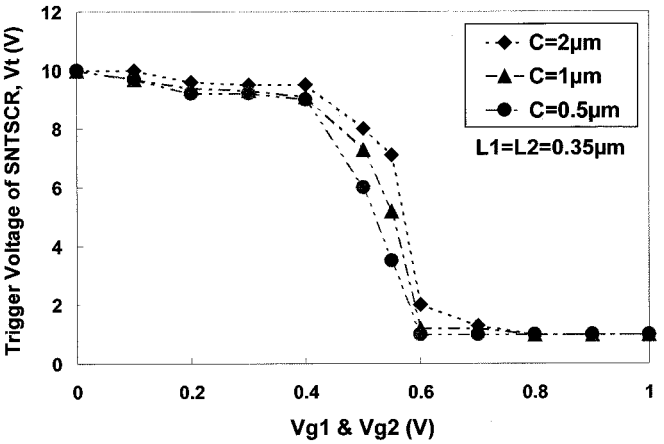
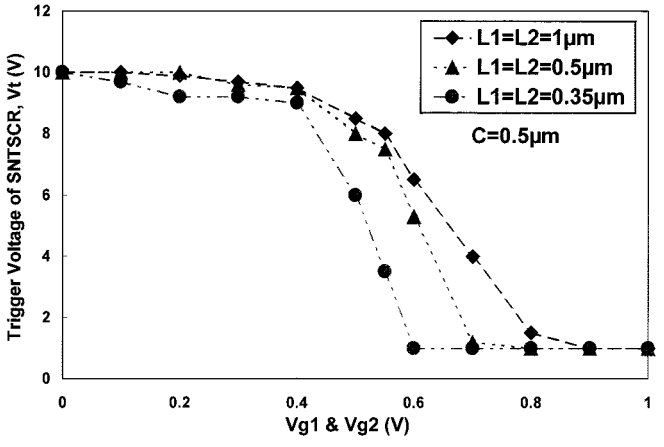


Fig. 2. The measured I–V curves of the fabricated SNTSCR devices with $C = 0.5\,\mu$m and $L1 = L2 = 0.35\,\mu$m under different gate biases (X-axis: 1 V/div; Y-axis: 1 mA/div).

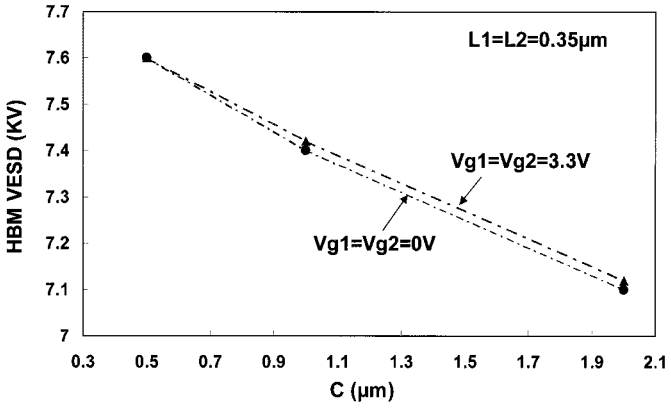


(a)

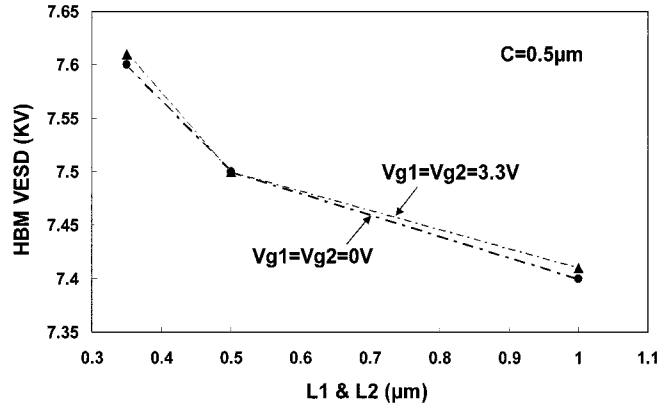


(b)

Fig. 3. Dependence of the trigger voltage on the gate bias voltage of the SNTSCR devices with (a) the different layout spacing C (where $L1 = L2$ is fixed at 0.35 μm) and (b) the different layout parameters of $L1$ and $L2$ (where C is fixed at 0.5 μm).



(a)



(b)

Fig. 4. Dependence of the HBM ESD level on (a) the layout parameter C and (b) the layout parameters $L1$ and $L2$ of the SNTSCR devices under different gate biases ($Vg1 = Vg2$). Failure criterion: $I_{\rm leakage} > 1\ \mu$A @ Vbias $= 5$ V.

also cause a lower trigger voltage on the SNTSCR device. The holding voltage of SNTSCR device is around ~ 1 V, which is not obviously changed by the different layout parameters on C, $L1$ and $L2$.

The impacts of layout parameters and gate biases on the human-body-model (HBM) [11] ESD level of the SNTSCR device are measured and compared in Fig. 4(a) and (b) under the positive-to-VSS ESD stress condition. The failure criterion is defined at the leakage current greater than 1 μA under the voltage bias of 5 V. In Fig. 4(a), the dependence of HBM ESD level on the layout parameter C with fixed channel lengths of $L1 = L2 = 0.35\ \mu$m in the SNTSCR device is shown. In Fig. 4(b), the dependence of HBM ESD level on the channel lengths of $L1$ and $L2$ with fixed layout parameter $C = 0.5\ \mu$m in the SNTSCR device is shown. The HBM ESD robustness of the SNTSCR device is degraded when the layout parameters C, $L1$, and $L2$ are increased. With shorter layout parameters (C, $L1$, and $L2$), which imply a smaller turn-on resistance, the SNTSCR device has a higher ESD level. The gate biases on $Vg1$ and $Vg2$ do not obviously improve the ESD level of the SNTSCR device, but it can trigger on the SNTSCR earlier to discharge ESD current.

Based on above experimental investigation, this SNTSCR has been used to protect the mixed-voltage I/O buffer. An ESD detection circuit is designed to provide suitable gate biases to trigger on the gates of SNTSCR during ESD stress conditions. On the contrary, this ESD detection circuit must keep the SNTSCR off, when the IC is under normal circuit operating conditions. The ESD detection circuit, designed by using the gate-coupling technique with consideration on gate-oxide reliability issue, had been reported in [12]. The HBM ESD level of the mixed-voltage I/O buffer with the stacked-NMOS channel width of 120 μm can be obviously improved from the original $\sim$ 2 kV to be greater than 8 kV by this SNTSCR device with a device dimension of only $60\ \mu{\rm m}/0.35\ \mu$m.

IV. Conclusion

The I–V characteristics of the new SNTSCR device for on-chip ESD protection under different gate biases and layout parameters have been investigated in details in CMOS process. This SNTSCR device can sustain a much higher ESD level within a much smaller layout area, which is very attractive to modern high-integration SoC. Without using the thick gate oxide, this SNTSCR device is fully process-compatible to general subquarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits against ESD damage.

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