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were obtained from Microparticles GmbH. Deionized water (18.2 MΩ cm) was prepared in a Millipore Milli-Q Plus 185 purification system. Octa(3-aminopropyl)aminosilsesquioxanes (NSi8) were prepared according to a procedure previously reported to obtain a 0.47 M NSi8 solution [17]. NSi8-capped silver nanoparticles, NSi8-Ag, were produced by adding aliquots of a sodium borohydride solution (4.5×10^{-2} M) to a 2.2×10^{-4} M silver salt NSi8 solution under vigorous stirring until the mixture turned deep brown-yellow. The NSi8-Ag nanoparticle solution was then used without further purification. Extinction spectra were recorded with a Cary 4E UV-vis spectrophotometer in the diffuse reflectance mode. High-resolution transmission electron microscopy (HRTEM) imaging was performed using a Philips CM12 microscope operated at 120 kV and equipped with an energy dispersive X-ray analyzer.

The LbL assembly of NSi8-capped silver nanoparticles with PSS on silica or PS spheres was performed after precoating the spheres with a PAH primer layer (from a 10.7 mM PAH solution, 0.5 M NaCl, pH 6) for PS spheres or a PDDA primer layer (from a 1 wt.-% solution, 0.5 M NaCl, pH 6.5) for silica spheres. The colloids were alternately exposed to a 5.8 mM PSS solution for 10 min (pH 2, without added salt) and to a NSi8-Ag solution for 90 min. This exposure time was derived from an adsorption study of NSi8-Ag on quartz-PDDA/PSS substrate, by monitoring the intensity of the plasmon absorption as a function of dipping time; these experiments indicated that about 80 min was necessary to reach the adsorption plateau. The primer layer was adsorbed by first adding 20 μL of a 10 wt.-% PS particle (925 nm in diameter) or silica (450 nm) dispersion to 1.5 mL of the PAH or PDDA solution, respectively, shaking for 10 min, centrifuging (4200 g, 7 min for PS spheres, or 3800 g, 7 min for silica spheres), and then washing (2 mL of water). The centrifugation/washing cycles were repeated at least 4 times to remove unadsorbed polyelectrolyte. Similarly, the next PSS layer was adsorbed by redispersing the coated particles in 1.5 mL of PSS solution with the same procedure, except that the pH of the rinsing water was fixed to 2. Rinsing the PSS layer at pH 2 was found to be essential in promoting an acid-base interaction with NSi8 [22]. The resulting coated colloids were dispersed in 10 mL of the NSi8-Ag solution and shaken for 90 min, followed by centrifugation (same conditions as above, without washing). This procedure was typically repeated 4 times to reach adsorption saturation; i.e., until an excess of NSi8-Ag was detected in the supernatant. The coated particles were then extensively washed with water (3×10 mL) at pH 5. This sequence of adsorption/centrifugation/redispersion was repeated n times to alternately coat the colloids with PSS and NSi8-Ag, leading to PS-PAH/(PSS/NSi8-Ag)$_n$ or silica-PDDA/(PSS/NSi8-Ag)$_n$. Calcination of the PS coated spheres was performed by heating (4.3 K min^{-1}) at 500 °C under nitrogen for 5 h and at 570 °C under oxygen for another 6 h.

Received: January 18, 2002

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A Silicon Nanowire with a Coulomb Blockade Effect at Room Temperature**

By *Shu-Fen Hu*,* *Wei-Zhe Wong*, *Shiue-Shin Liu*, *Yung-Chun Wu*, *Chin-Lung Sung*, *Tiao-Yuan Huang*, and *Tzong-Jer Yang*

Single-electron transistors (SETs), which utilize the Coulomb blockade effect arising from the electrostatic charging energy of a single electron,[1] are one of the promising candidates for future integrated circuits due to their extremely low power consumption and high density integration. For room-temperature operation, a nanoscale ultramicroscopic structure is required. It is therefore necessary to decouple the artificial confinement of electrons in the semiconductor structure in one or more spatial dimensions, leading to two-, one-, or zero-dimensional electronic systems.[2,3] In the past decade, nanoscale semiconductor structures have been studied extensively in an effort to understand the size-quantization effects in such materials. Single-electron conductance oscillations[4] and Coulomb blockade effects[1] have been observed in mesoscopic low-dimensional structures. For example, Coulomb blockade effects were demonstrated by Yano et al. in polycrystalline silicon structures by taking advantage of the nonuniformity in thickness of the sufficiently thin film so a natural potential difference occurs between individual Si grains.[5] Coulomb blockade effects were also observed by Ng et al. at low temperatures (i.e., no higher than 70 K) in hydrogenated amorphous silicon recrystallized by electron beam annealing.[6] The conduction mechanism was modeled on the combi-

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[**] This work was financed by contracts NSC90-2721-2317-200 and NSC90-2215-E-317-002 supported by the National Science Council. We thank Prof. Simon M. Sze for his critical reading of the manuscript. We also acknowledge the technical support given by the National Nano-Device Laboratories.

  0935-9648/02/1005-0736 $ 17.50+.50/0

nation of carrier hopping between trapping sites in amorphous regions or at grain boundaries with additional Coulomb blockade effects, as well as confinement due to potential fluctuations arising from dopant distribution. Concurrently, devices based on silicon-on-insulator (SOI) wafers using separation by implanted oxygen (SIMOX) have recently received a lot of attention, as the SOI structure is conducive to obtaining thin devices, thus alleviating the undesirable effect of a bulk Si wafer.[7–11] In this paper, we present our experimental results on narrow thin silicon wires with a final width and thickness of 29 and 3 nm, respectively, on SIMOX wafers. The room-temperature Coulomb blockade effects and the influence of a capacitively coupled gate on the transport properties of the conducting silicon quantum wires were studied.

A schematic of the narrow silicon wire fabricated in this study is shown in Figure 1a. The enlarged high-resolution transmission electron microscopy (HRTEM) image of the

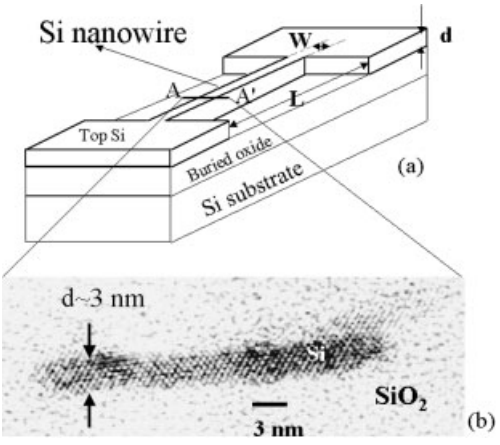

Fig. 1. a) Schematic diagram of a Si quantum wire. b) Cross-sectional view of a high-resolution TEM image of the profile of the silicon nanowire along AA′. Lateral crystallite dimensions of d~3 nm and W~29 nm were confirmed.

cross-sectional profile along AA′ of the narrow wire is shown in Figure 1b. An abrupt interface between the oxide and the silicon is observed. Dark regions as well as gray regions are observed within the silicon layer. The dark orderly "lattice-like" areas are nanocrystalline Si regions that are separated by the SiO_2 amorphous phase (gray regions). The separation between crystalline planes in the image was measured to be ~5 Å, in excellent agreement with the Si lattice constant of 5.43 Å. The lateral crystal dimensions d~3 nm and W~29 nm are also confirmed by the cross-sectional view in Figure 1b.

Current–voltage characteristics measured at T = 300 K as a function of the source–drain bias for narrow wires with various lengths are shown in Figure 2. It can be seen that these nanowires display a very low current regime over a considerable voltage range around zero bias, an indication of the Coulomb blockade effect. Similar transport properties, albeit at temperatures below 77 K, have been reported previously in narrow indium oxide wires,[12] titanium wires,[13] and silicon wires.[6,9,14] When the drain bias is sufficiently high, the current blockade through the wire can be lifted. This is due to the additional energy, which enables the electrons to occupy higher orbital states in the confined quantum wire, thus opening a large energy window for tunneling.

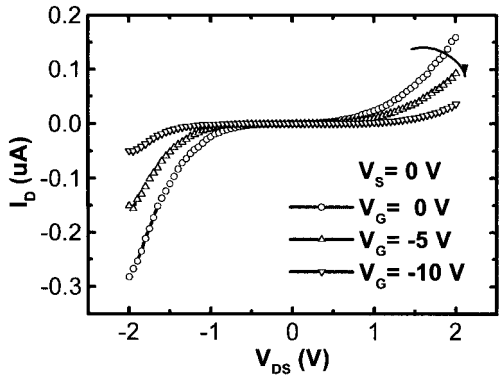

Fig. 2. Current–voltage characteristics measured at room temperature (300 K) of silicon wire at gate voltage of 0, –5, and –10 V. The wire length is 1 μm.

The effects of a capacitively coupled gate on the transport properties of nanowires were also studied. The gate electrode was formed by a probe tip, which was placed in direct contact with the oxide on top of a wire of length 1 μm. The room-temperature drain–source and current–voltage characteristics of a wire with an active width ~29 nm and thickness ~3 nm were measured with different gate voltages V_G=0, –5, and –10 V. The results are shown in Figure 2. Gate coupling was weak due to the relatively thick oxide (~500 nm) used in this study. Nevertheless, it can be seen clearly that a more negative gate bias gives rise to a wider blockade region. To gain more insight into this phenomenon, the source potential with respect to the grounded drain potential, V_{SD}, was repeatedly scanned from –2 V to 2 V with the gate potential, V_G, fixed at –10 V. The drain current, I_D, was plotted as a function of V_{SD}. The resultant I–V characteristics are shown in Figure 3. The Coulomb blockade effect can be seen clearly. In addition, the blockade region becomes wider after each repetitive scan. The corresponding tunneling spectra (dI/dV vs. V) are shown in Figure 4. The tunneling spectra appear to be asymmetrical with several peaks (as indicated by arrows in Fig. 4) in the positive and negative bias regions. The conductive peaks in

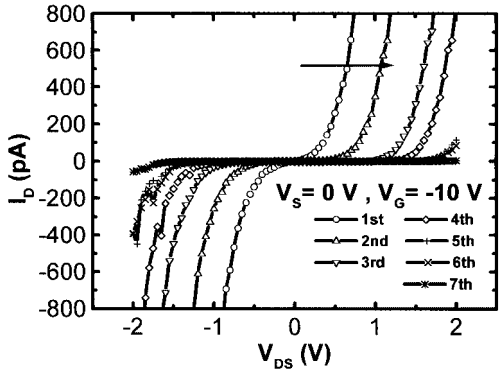

Fig. 3. Current–voltage characteristics of silicon wire at room temperature (300 K) measured after each repetitive scanning. V_G is fixed at –10 V. The wire length is 1 μm.

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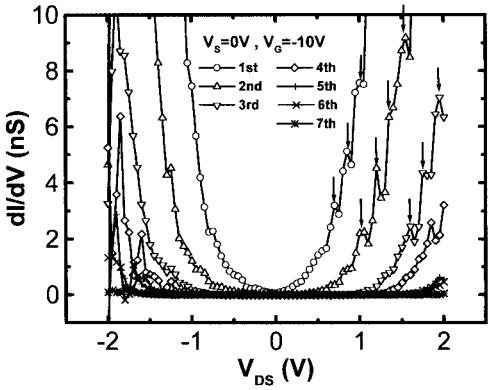

Fig. 4. Conductance (dI_D/dV_D) oscillations of silicon wire plotted as a function of V_{DS} at room temperature (300 K) measured after each repetitive scanning. V_G is fixed at –10 V. The wire length is 1 μm.

the positive bias region as shown in Figure 4 are much higher and better resolved than the peaks in the negative bias region. It should be noted that conductance, on the other hand, increases more rapidly at negative bias than at positive bias. The peaks also appear to occur periodically under positive drain–source bias. The oscillation period ΔV is roughly 0.15–0.2 V. Assuming a dominant charging island, the island capacitance ($C_g = e/\Delta V$) is estimated to be $e/2\Delta V$ = ~4–5×10^{-19} F.

Next, the *I–V* characteristics were again measured by repetitively scanning V_{SD} from –2 V to 2 V, with the gate voltage, V_G, fixed at 10 V. The resultant *I–V* characteristics are plotted in Figure 5. It can be seen that the blockade region becomes narrower with each repetitive scan, which is the exact opposite of what occurs when a negative fixed voltage is applied, as previously shown in Figure 3. The measurements were taken over a period of several days and the small discrepancy in the magnitude of the current between Figures 3 and 5 is probably due to a change in the trapped charges along the wire. Generally, the contribution of many impurities averages to a conductance constant that depends only on their density, and not their exact location. However, in small nanostructures such as quantum point contacts, the total scattering matrix through the structure, including impurities and roughness, depends on the exact location of the impurities and boundary fluctuations.[15] Randomly distributed electron islands separated by tunneling barriers could be formed by dopant fluctuations within the nanostructure.[16] If such inhomogeneous effects[15] are important, the conductance in a sample with a slightly different impurity configuration will be completely different. Figure 6 illustrates the formation of a single-electron structure in these nanowires due to the aforementioned dopant fluctuations.[16] In a one-dimensional picture the edge of the conduction band, E_C, varies due to the local variation of the doping level along the wire, leading to local regions with Fermi level, E_F, below E_C, where isolated electron islands are formed (Fig. 6a). Since a series of SETs is formed, these structures do not display conductance peaks with an exact periodicity. When the electron density is further lowered by charge trapping (assuming a uniform charge trapping for simplicity) after the application of a negative gate voltage with respect to the wire, more isolated electron islands with E_F lower than E_C are formed as depicted in Figure 6b.

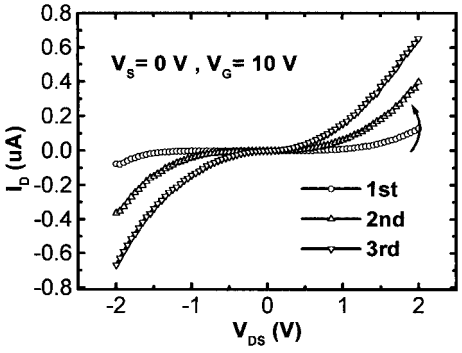

Fig. 5. Current–voltage characteristics of silicon wire at room temperature (300 K) measured after each repetitive scanning. V_G is fixed at +10 V. The wire length is 1μm.

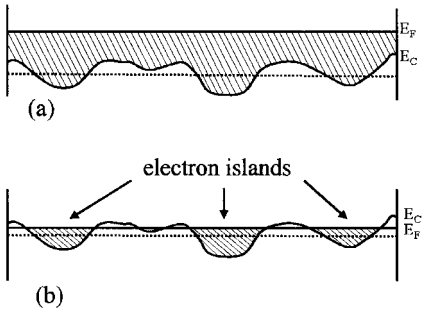

Fig. 6. Schematics of the potential fluctuations along a highly doped silicon nanowire [16]. a) Isolated electron islands are formed due to dopant fluctuations, leading to a series of SETs. b) More isolated electron islands with E_F lower than E_C are formed as a result of charge trapping after the application of a negative gate bias. The dotted horizontal line is the average value of the conduction band E_C.

Recently, Cui and Lieber reported the assembly of well-defined, n- and p-type Si nanowire building blocks into functional electronic devices.[17] Their studies demonstrate a rational approach to building key nanoscale electronic devices from Si nanowires that have controlled carrier type and concentration. However, our study is concentrated on Coulomb blockade effects and the influence of a capacitively coupled gate on the transport properties of the conducting silicon quantum wires.

In summary, we have fabricated an extremely narrow, thin silicon wire on SIMOX wafer. The nanowire features a lateral dimension of 3 nm × 29 nm, as confirmed by a cross-sectional view of the HRTEM image. Coulomb blockade effects are observed in the structure at room temperature. The formation of isolated electron islands when the Fermi level becomes locally lower than the conduction band edge due to dopant fluctuation is proposed to explain the observed effects. Furthermore, the Coulomb blockade region is modulated by the applied gate bias. While a negative gate bias is found to increase the Coulomb blockade region, a positive gate bias acts to reduce it. Charge trapping causing a shift in the Fermi level with re-

  0935-9648/02/1005-0738 $ 17.50+.50/0

spect to the conduction band edge is proposed to explain the observed gate bias effects. Based on our discoveries of this charging phenomenon, the corresponding single-electron memory devices may have potential applications.

Experimental

The narrow silicon wires in this study were fabricated using SIMOX wafers with <100> p-type Si substrates, featuring a thin 60 nm silicon layer on top of 400 nm of buried SiO_2. The top 60 nm silicon layer was doped by phosphorus ion implantation to a concentration of 2×10^{14} ions/cm^2 and with an energy of 40 kV. The doping level is sufficiently high to achieve a sheet resistance of around 965–1118 Ω/□. The silicon layer was thinned down by sacrificial oxidation, followed by oxide stripping. 80 nm wide silicon wires were then defined by direct e-beam writing using a Leica Weprint 200 system with a NEB22A photoresist. Once again, the 80 nm silicon wires were further narrowed by sacrificial oxidation. Finally, a 20 nm gate oxide was grown at 925 °C for 43 min in oxygen, which further reduced the silicon wire's thickness and width. A 500 nm passivating oxide layer was then deposited, followed by contact opening and aluminum metallization for electrical connection. High-resolution transmission electron microscopy (HRTEM) with a JEOL-4000EX electron microscope operating at 400 kV was employed to examine structural aspects of the Si wire. A HP4156C precision semiconductor parameter analyzer was used to measure the electrical properties.

Received: January 22, 2002
Final version: March 7, 2002

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Room-Temperature, Tunable Gain Media from Novel II–VI Nanocrystal–Titania Composite Matrices**

By *Vikram C. Sundar*, *Hans-Jürgen Eisler*, and *Moungi G. Bawendi**

Chemically synthesized semiconductor nanocrystals (NCs) offer the promise of a color-tunable, flexible, all-purpose chromophore system, in which strong quantum confinement of the carriers leads to unique, size-dependent linear and nonlinear optical properties.[1] For example, the reduced dimensionality, and the resulting quantum confinement, of carriers in NCs should facilitate the development of temperature insensitive and easily tunable gain media.[2,3] Recently, Klimov et al.[4] reported the first observation of amplified spontaneous emission (ASE) at 80 K in closed-packed films of CdSe NCs, and deduced the necessary parameters to facilitate stimulated emission. Although such films possessed the requisite high NC concentration necessary for ASE, they lacked the stability or processability to be incorporated into more complicated structures. In this report, we describe new chemistry to stabilize high volume fractions of NCs within an inorganic, sol–gel titania matrix, which yields high-quality waveguides. The unique optical properties of the NCs are combined with the superior stability of the titania matrix to produce composites with narrow gain profiles, that are tunable through most of the visible spectrum (550 nm to 650 nm), and that can operate at 80 K and room temperature. Finally, the added ability of the NCs to tune the refractive index of the composite NC–titania films is exploited to create more complicated multilayer waveguide structures that show ASE *simultaneously* at spectrally distinct regions while being excited with a *single* source; a first step towards the production of a NC-based white laser.

Previous efforts at stabilizing II–VI NCs in sol–gel matrices consisted of sequestering a Cd^{2+} salt or precursor within a borosilicate glass or matrix and subsequent exposure to a chalcogenide source.[5,6] Growth of particles was then done thermally within the media. Such attempts usually resulted in composites with less than optimal size-distributions, poor luminescence qualities and low volume fractions; all features that hinder the observation of ASE with such matrices. An alternative strategy involves decoupling the synthesis of the NCs from the preparation of the matrix. Although, Ptatschek et al. synthesized CdSe NC-matrix composites using amine-terminated silane coupling groups to sequester the NC within the matrix,[7] observation of ASE from the composites was

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[**] We thank the NSF funded MIT Harrison Spectroscopy Laboratory for support and for use of its facilities. We thank Dr. S. Miller for help with the lasers. HJE acknowledges support from the DFG. This research was supported in part through the NSF-Materials Research Science and Engineering program, and by the Packard Foundation.

  0935-9648/02/1005-0739 $ 17.50+.50/0