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Substrate-triggered ESD clamp devices for use in power-rail ESD clamp circuits ☆

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Abstract

New electrostatic discharge (ESD) clamp devices for using in power-rail ESD clamp circuits with the substrate-triggered technique are proposed to improve ESD level in a limited silicon area. The parasitic n–p–n and p–n–p bipolar junction transistors (BJTs) in the CMOS devices are used to form the substrate-triggered devices for ESD protection. Four substrate-triggered devices are proposed and investigated in this work, which are named as the substrate-triggered lateral BJT, the substrate-triggered vertical BJT, the substrate-triggered double BJT, and the double-triggered double BJT. An RC-based ESD-detection circuit is used to generate the triggering current to turn on the proposed substrate-triggered devices. In order to trigger on the parasitic bipolar transistors more effectively, the symmetric multiple-cell square-type layout method is used to realize these substrate-triggered devices. The power-rail ESD clamp circuits with such substrate-triggered devices have been fabricated in a 0.6-μm CMOS process. Experimental results have shown that the substrate-triggered device with double-BJT structure can provide 200% higher ESD robustness in per silicon area, as compared to the NMOS with the traditional gate-driven design. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: Electrostatic discharge; Substrate-triggered technique; Electrostatic discharge clamp circuit; Secondary breakdown current (I_{t2}); Bipolar junction transistor

1. Introduction

Whole-chip electrostatic discharge (ESD) protection has become an important reliability design for deep-submicron CMOS ICs. In the input/output ESD protection circuits, the ESD protection devices with larger device dimensions are often drawn in the multiple finger-type layout style. To enhance uniform turn-on phenomena among the multiple fingers of the ESD protection devices, the gate-coupled technique had been reported to improve ESD level of ESD protection circuits [1,2]. But, the second breakdown current (I_{t2}) and ESD level of NMOS device had been found to be suddenly degraded if the NMOS gate voltage was somewhat over biased [3–6]. Therefore, the gate-coupled design has to be carefully optimized to avoid the sudden degradation on ESD robustness [3,4]. However, even if there were suitable ESD protection circuits around the input and output pads, the internal circuits were still vulnerable to ESD damages [7–11].

Since the ESD stress may have positive or negative voltage on an input (or output) pin with respect to the grounded V_{DD} or V_{SS} pins, there are four different ESD-testing pin combinations at each input (output) pin, which are shown in Fig. 1(a) and (b). For a comprehensive ESD verification, two additional ESD-testing pin combinations, the pin-to-pin ESD stress and the V_{DD}–V_{SS} ESD stress in Fig. 1(c) and (d), had been also specified to verify the whole-chip ESD reliability [12]. These two additional ESD-testing pin combinations

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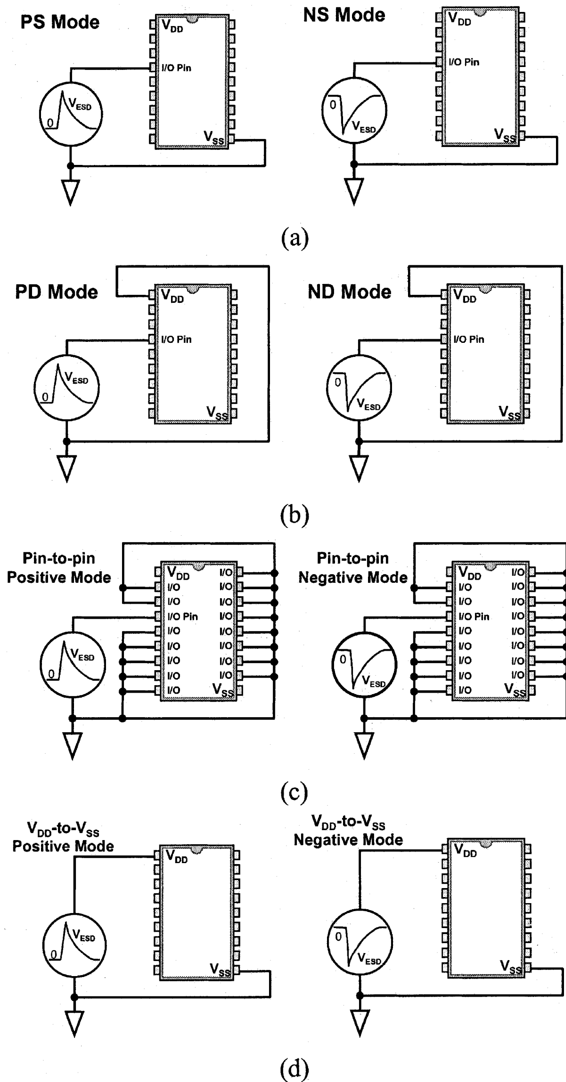


Fig. 1. (a) Positive and negative ESD stress on an input (or output) pin with respect to the grounded V_{SS}. (b) Positive and negative ESD stress on an input (or output) pin with respect to the grounded V_{DD}. (c) The pin-to-pin ESD stress: the ESD voltage is applied to an input (or output) pin while all other input or output pins are grounded but the V_{DD} and V_{SS} pins are floating. (d) The V_{DD}–V_{SS} ESD stress: the ESD voltage is directly applied to the V_{DD} pin with the V_{SS} pin grounded but all input and output pins are floating.

often lead to more complex ESD current paths from the input or output pins through the power lines into the internal circuits, which will cause some unexpected damages on the internal circuits even if there are input and output ESD protection circuits in the ICs [7–11]. The ESD current discharging paths in an IC during the pin-to-pin ESD stress is illustrated in Fig. 2(a), where a positive ESD voltage is applied to an input pin with

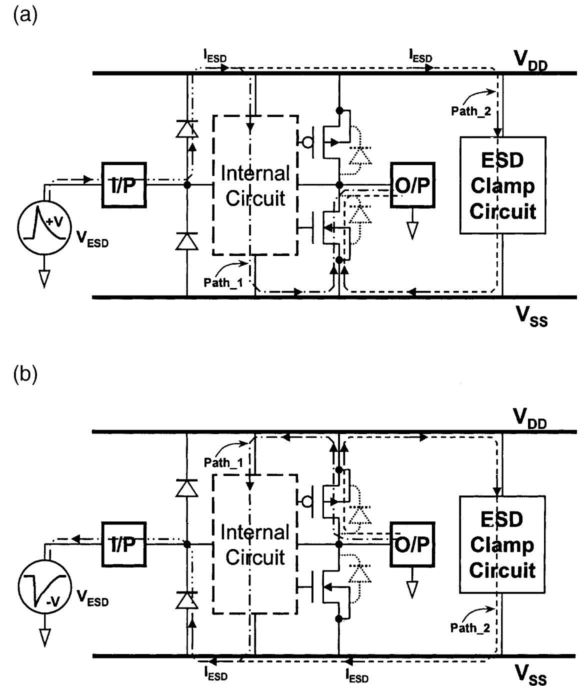


Fig. 2. The ESD current discharging paths in an IC during the (a) positive, and (b) negative, pin-to-pin ESD stress conditions. If the IC has no effective ESD clamp circuit between the V_{DD} and V_{SS} power rails, the ESD current is discharged through the Path_1, which often causes ESD damage located at the internal circuits. If the IC has an effective ESD clamp circuit between the V_{DD} and V_{SS} power rails, the ESD current is discharged through the Path_2.

some output pin relatively grounded, but the V_{DD} and V_{SS} pins are floating. The ESD current will be diverted from the input pad to the floating V_{DD} power line through the forward-biased diode in the input ESD protection circuit. The ESD current flowing on the V_{DD} power line can be conducted into the internal circuits through the connection of V_{DD} metal line. Then, the ESD current is discharged through the internal circuits and may cause random ESD damage in the internal circuits, as the current Path_1 shown in Fig. 2(a). If there is an effective ESD clamp circuit across the V_{DD} and V_{SS} power lines, the ESD current can be discharged through the current Path_2 in Fig. 2(a). Therefore, the internal circuits can be safely protected against the ESD damages under a negative ESD stress, the similar ESD current paths are shown in Fig. 2(b). Thus, an effective ESD clamp circuit with a quick turn-on speed across the power rails is necessary for protecting the internal circuits against ESD damage.

To overcome such unexpected ESD damage on the internal circuits beyond the input or output ESD protection circuits, some ESD clamp circuits across the V_{DD}

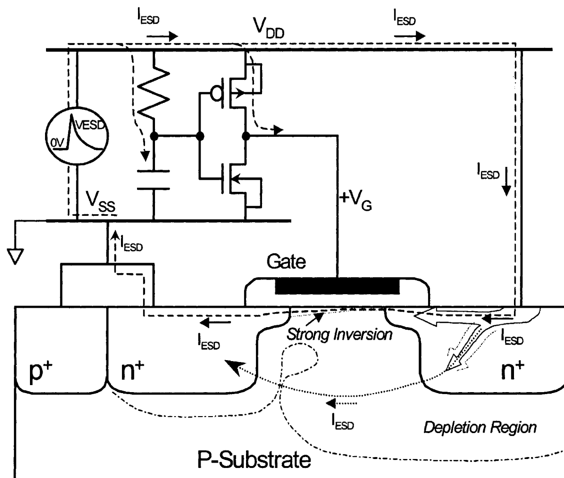


Fig. 3. The schematic diagram of the RC-based ESD clamp circuit with a gate-driven NMOS as the ESD clamp device between the V_{DD} and V_{SS} power rails.

and V_{SS} power rails had been reported [12–20]. In Refs. [12–15], an RC-based ESD-detection circuit was used to turn on an NMOS to bypass the ESD current from V_{DD} to V_{SS}. The schematic circuit diagram of such a traditional design by gate-driven technique is illustrated in Fig. 3 with the cross-sectional view of NMOS device structure. During the ESD stress, the RC-based ESD-detection circuit conducts some ESD voltage from V_{DD} power rail to bias the gate of the ESD-clamp NMOS. The positive gate voltage causes a strong inversion along the NMOS channel and leads to the ESD current focussing at the lightly doped drain (LDD) peak structure. The ESD current, flowing through the very shallow junction depth of the LDD peak structure and the inversion layer along the channel, causes a very low ESD level on the NMOS. The over-biased gate voltage on NMOS had been reported to cause a lower second breakdown current (I_{t2}) or ESD level on the NMOS devices [3–6], as compared to a gate-grounded NMOS. In order to sustain a desired 3-kV human body metal (HBM) ESD level, the ESD-clamp NMOS was designed with a huge device dimension of $W/L = 8000$ μm/0.8 μm in Ref. [13]. Such a huge ESD-clamp NMOS generally occupies a much more silicon area, which also causes a cost issue to IC products.

In Refs. [16–18], the diode string with multiple stacked diodes was reported as the ESD-clamp device across the power rails of an IC. The diode in the forward-biased condition can sustain a much higher ESD level than it in the reverse-biased condition. But, the forward-biased diode string conducts a considerable leakage current across the V_{DD} and V_{SS} power rails, when the IC with normal power supplies is operating in a higher temperature. In Refs. [19,20], the lateral SCR device in CMOS process were used as the ESD-clamp device across the V_{DD} and V_{SS} power rails. The lateral SCR device can sustain a very high-ESD stress with a much smaller silicon area, as compared to other ESD protection devices. But, the lateral SCR may be triggered on to cause latchup problem by overshooting noise pulses across the power rails [21–25], when the IC is in the normal operation condition with power supplies. In the system-level ESD testing [26] or the V_{DD}-transient latchup testing [27], the SCR used as the ESD-clamp device across the power rails could be triggered on by the overshooting noise pulses to cause a serious latchup problem in CMOS ICs. Thus, an area-efficient and latchup-free ESD clamp circuit with quick turn-on speed across the power rails is strongly urged by the scaled-down CMOS ICs.

Recently, the substrate-triggered technique was reported to improve ESD level of NMOS devices in deep-submicron CMOS technologies for I/O ESD protection [28–31]. The potential of local substrate under the NMOS device is charged up in ESD-stress condition by both circuit design and suitable layout arrangement to earlier initiate the bipolar action of the NMOS device. When the parasitic lateral n–p–n bipolar junction transistor (BJT) in the NMOS device is turned on, the ESD current is discharged through the BJT path in the NMOS structure. Such an ESD current discharging path is far away from the NMOS drain LDD peak and the NMOS surface channel. Therefore, the NMOS can sustain a higher ESD level by the substrate-triggered design, as compared to the gate-driven or gate-grounded design.

In this paper, four substrate-triggered devices for using in the power-rail ESD clamp circuits are proposed and investigated [32]. The parasitic lateral and vertical bipolar transistors in the NMOS or PMOS structures are used to discharge the ESD current, which are turned on by the substrate-triggered design. Therefore, the proposed ESD-clamp devices can sustain a much higher ESD level within a smaller silicon area.

2. Substrate-triggered ESD clamp devices

ESD robustness of CMOS devices is strongly dependent on the device structure, layout style, and layout spacing. If the ESD current is uniformly discharged through the parasitic lateral BJT of the MOS structure, the ESD current flows away from both the shallow surface channel and the LDD peak of MOS device. Therefore, the MOS device can sustain a much higher ESD stress. To induce the ESD current flowing through the parasitic lateral BJT away from the surface channel of MOS device, the substrate-triggered technique is proposed in this work to significantly improve ESD robustness of the ESD clamp devices.

To investigate the efficiency of the substrate-triggered technique, four substrate-triggered devices with different devices structures are fabricated and investigated in a 0.6-μm CMOS process. In order to enhance the more uniform turn-on phenomena and the BJT action in the ESD clamp device, the cell-based square-type layout method [33] is used to realize these four substrate-triggering devices.

2.1. Substrate-triggered lateral BJT device

The schematic cross-sectional view of the substrate-triggered lateral BJT (STLB) device with its corresponding control circuit is shown in Fig. 4(a), where the base of the lateral n–p–n BJT is controlled by the RC-based ESD detection circuit. During the ESD transition, the voltage on the capacitor C is initially kept at a low level due to the RC time delay in the ESD-detection circuit [12–15]. The RC value is often designed around 0.1–1 μs to distinguish the ESD transition or the normal V_{DD} power-on transition. To efficiently turn off the surface channel of NMOS, the gate of NMOS is directly connected to ground (V_{SS}). The inverter in Fig. 4(a) is self-biased by the ESD energy and provides a trigger current, into the p-substrate from the node n2. The trigger current, flowing in the local p-substrate region, forward biases the base–emitter junction of the parasitic lateral n–p–n BJT of the gate-grounded NMOS device. The parasitic lateral n–p–n BJT is therefore triggered on, and the ESD current is discharged through the lateral n–p–n BJT, which is far from the surface channel and the LDD peak of the gate-grounded NMOS. To improve the turn-on speed of the lateral BJT, an N-well structure is especially inserted under the NMOS source region to collect the triggering current in the local substrate. This N-well structure also increases the equivalent base resistance of the lateral n–p–n BJT to improve its turn-on speed. Therefore, the bipolar action in the NMOS device can be earlier initiated to bypass the ESD current in the ESD-stress condition.

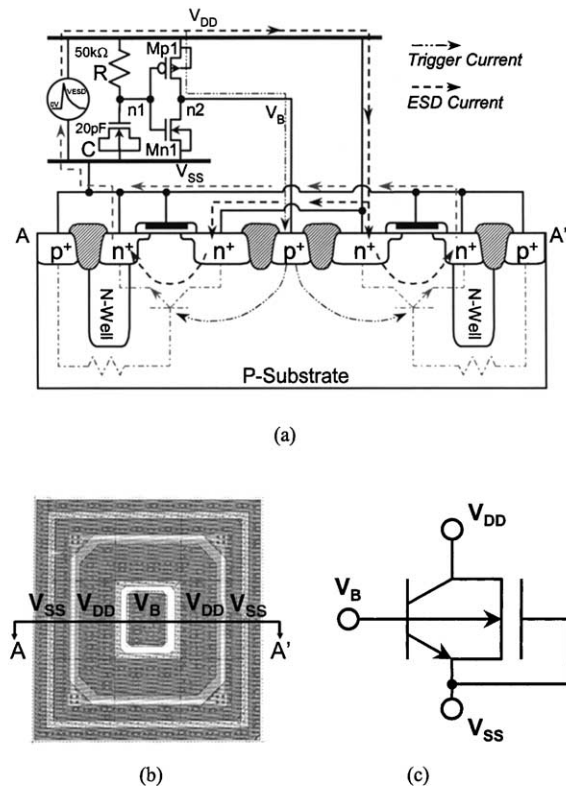
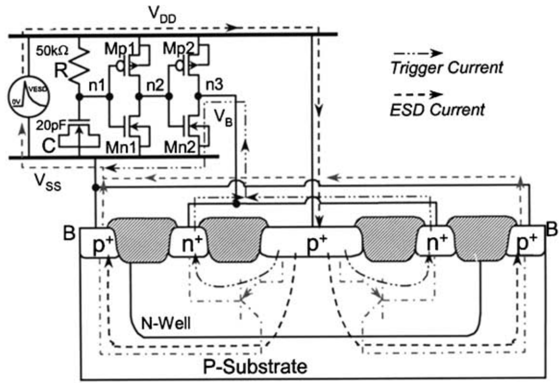


Fig. 4. (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered lateral BJT (STLB) device, (b) the layout of a unit cell of the STLB device and (c) the symbol of STLB device.

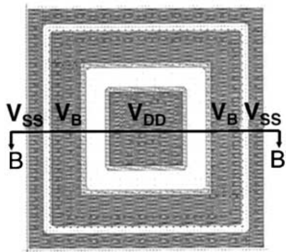
The practical layout of a unit cell of the STLB device is drawn in Fig. 4(b), and its symbol is shown in Fig. 4(c). To connect the gate of the NMOS to ground, the width of the gate is locally extended to the four corners in the unit cell. The device cross-sectional view along the line A–A′ of Fig. 4(b) is corresponding to that drawn in Fig. 4(a). The P^+ diffusion connected to the trigger node V_B is drawn at the center of the cell, and the P^+ diffusion connected to V_{SS} surrounds the whole unit cell at the outside. By using such a layout arrangement and the additional N-well inserted under the NMOS source region, the bipolar action of the NMOS can be earlier triggered on for effective ESD protection purpose. A unit cell of the STLB device realized in a 0.6-μm CMOS process occupies a silicon area of 47.7×47.4 μm^2. A STLB device with a larger device dimension can be assembled by a plurality of such cells.

2.2. Substrate-triggered vertical BJT device

The vertical p–n–p BJT is also designed to discharge the ESD current across the power rails. The ESD clamp circuit with the schematic cross-sectional view of the substrate-triggered vertical BJT (STVB) device is shown in Fig. 5(a). The vertical BJT is formed by the p^+ diffusion (connected to V_{DD}) in the N-well, the N-well (connected to V_B), and the p-substrate (connected to V_{SS}). To trigger on the vertical p–n–p BJT, the base node (N-well) of the vertical p–n–p BJT has to be kept at a low-voltage level during the ESD transition. On the contrary, the base node (N-well) must be kept at the voltage level of V_{DD} to turn off the BJT when the IC is in normal operation condition. To achieve such requirement, two-stage inverters are inserted in the ESD detection circuit between the RC and the vertical BJT, as that shown in Fig. 5(a). The two inverters are self-biased by the ESD energy to keep the node V_B at a low-voltage



(a)



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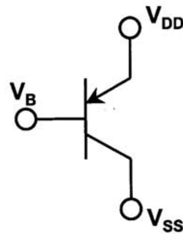
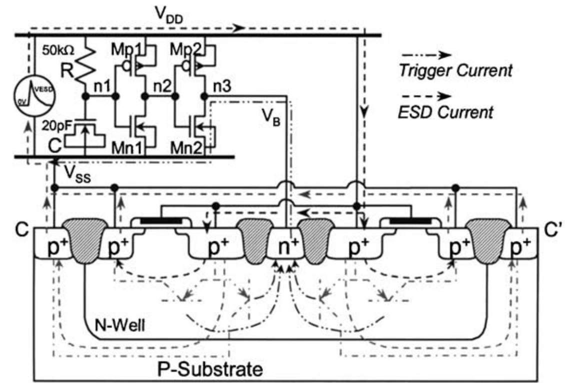
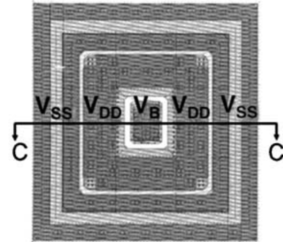


(c)

Fig. 5. (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered vertical BJT (STVB) device, (b) the layout of a unit cell of the STVB device and (c) the symbol of STVB device.



(a)



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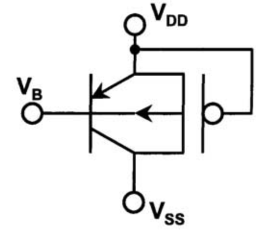

(c)

Fig. 6. (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered double BJT (STDB) device, (b) the layout of a unit cell of the STDB device and (c) the symbol of STDB device.

level in the ESD-stress condition, but the node V_B is biased at V_{DD} when the IC is in normal operation condition.

The practical layout of a unit cell of the STVB device is shown in Fig. 5(b), and its symbol is shown in Fig. 5(c). The device cross-sectional view along the line B–B′ of Fig. 5(b) is corresponding to that drawn in Fig. 5(a). A unit cell of the STVB device realized in a 0.6-μm CMOS process occupies a silicon area of 40.5×40.5 μm^2. A STVB device with a larger device dimension can be assembled by a plurality of such cells.

2.3. Substrate-triggered double BJT device

To make a complementary design to the STLB (with NMOS), the parasitic p–n–p BJT in the PMOS device is also designed to discharge the ESD current across the power rails. The ESD clamp circuit and the schematic cross-sectional view are shown in Fig. 6(a). In Fig. 6(a), the source and gate of the ESD-clamp PMOS are connected together to V_{DD}. The drain of the ESD-clamp PMOS is connected to V_{SS}. When this ESD clamp circuit is stressed by a positive ESD, the surface channel of the ESD-clamp PMOS is kept off. A lateral p–n–p BJT is formed by the drain and source of the PMOS. There is also a parasitic vertical p–n–p BJT within this device structure to constitute the *double* BJT structure in meanwhile. The vertical p–n–p BJT is formed by the source of the PMOS, the N-well, and the grounded p-substrate, as that shown in Fig. 6(a).

The substrate-triggered technique is used to trigger on the double BJT structure. To trigger on the double BJT, the base (N-well) of the double BJT has to be kept at a low-voltage level during the ESD transition. But, the base (N-well) has to be kept at the voltage level of V_{DD} when this circuit is under normal operation condition. In the normal operation condition, the node n1 on the capacitance C is charged up to V_{DD}. Therefore, the node n3, connected to the n$^+$ diffusion in the N-well, is biased at the voltage level of V_{DD} to keep the parasitic p–n–p BJTs off in the substrate-triggered double BJT (STDB) device. During the ESD transition, the node n1 in Fig. 6(a) is initially kept at a low-voltage level before the capacitance C is charged up to a high-voltage level. The node n2 in Fig. 6(a) is therefore charged to a

high-voltage level by the ESD energy. Thus, the node n3 (also the node V_B) is kept at a low-voltage level. The emitter–base junction of the parasitic p–n–p BJTs in the STDB device is forward biased to turn on the STDB device during the ESD transition.

The practical layout of a unit cell of the STDB device is shown in Fig. 6(b), and its symbol is shown in Fig. 6(c). To connect the gate of the PMOS, the width of the gate is locally extended to inner at the four corners in the unit cell. The device cross-sectional view along the line C–C′ of Fig. 6(b) is corresponding to that drawn in Fig. 6(a). A unit cell of the STDB device realized in a 0.6-μm CMOS process occupies a silicon area $67.1 \times 67.1\ \mu m^2$. A STDB device with a larger device dimension can be assembled by a plurality of such cells.

2.4. Double-triggered double BJT device

To provide more current discharging path in per silicon area of the ESD clamp device, a double-triggered design is shown in Fig. 7(a) with the double-triggered double BJT (DTDB) device. The double BJT structure is the same as that in the STDB device. The double-triggered design is achieved by applying the trigger voltage to the gate of ESD-clamp PMOS and the trigger current to the base of double BJT structure. Both the PMOS device and the double BJT structure can be quickly turned on to provide more ESD current discharging path in the device structure. The trigger circuit to turn on the DTDB is similar to that with the STDB device. During ESD transition, the ESD detection circuit provides a trigger current (voltage) into the N-well (gate) to turn on the DTDB device. While the IC is in the normal operation condition, the node V_B is biased at V_{DD} voltage level. Therefore, the DTDB device is kept off.

The practical layout of a unit cell of the DTDB device is shown in Fig. 7(b), and its symbol is shown in Fig. 7(c). To connect the gate of the PMOS, the width of the gate is locally extended at the top and bottom sides in the unit cell. The device cross-sectional view along the line D–D′ of Fig. 7(b) is corresponding to that drawn in Fig. 7(a). A unit cell of the DTDB device realized in a 0.6-μm CMOS process occupies a silicon area of $67.1 \times 67.1\ \mu m^2$. A DTDB device with a larger device dimension can be assembled by a pluarality of such cells.

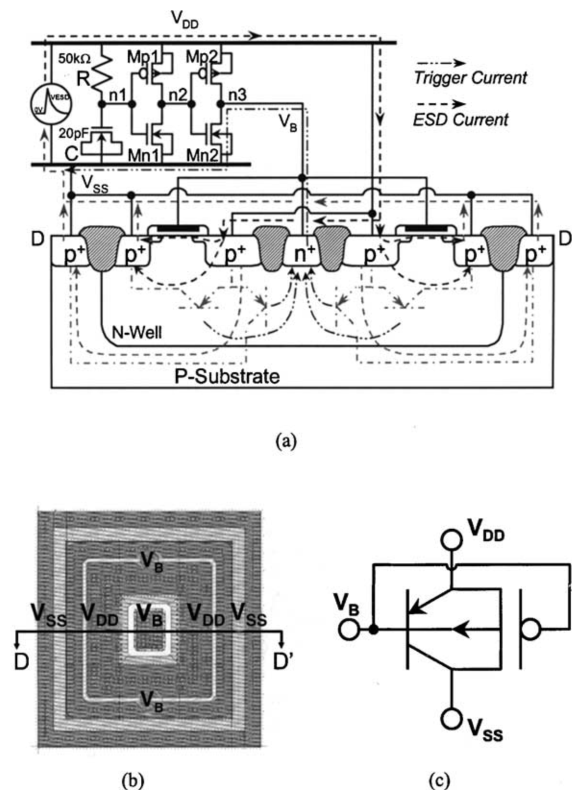

Fig. 7. (a) The schematic diagram of the ESD clamp circuit with the double-triggered double BJT (DTDB) device, (b) the layout of a unit cell of the DTDB device and (c) the symbol of DTDB device.

3. Circuit simulation

To verify the actual operations of the RC-based ESD-detection circuits, the power-rail ESD clamp circuits with the STLB and DTDB devices are simulated by HSPICE in both the ESD stress condition and the normal V_{DD} power-on condition.

3.1. ESD stress condition

A voltage pulse with a pulse width of 100 ns and a rise time of 2 ns is used to stimulate the rising edge of an HBM ESD voltage. The RC-based ESD-detection circuits are designed to detect such a fast rising voltage on V_{DD} and therefore to turn on the ESD clamp device. The pulse height of the applied voltage pulse used in this simulation is selected to 8 V, which is smaller than the breakdown voltage of the proposed ESD clamp devices. The RC-based ESD-detection circuits are designed to turn on the ESD clamp devices during the ESD stress condition, before the ESD clamp devices are broken down by overstress ESD voltage. Therefore, the power-rail ESD clamp circuits can be really triggered on earlier to bypass the ESD current, before the internal circuits are damaged by the ESD energy.

The simulated results are shown in Fig. 8(a) and (b), where an 8-V voltage pulse is applied to the V_{DD} power rail and the V_{SS} power rail is relatively grounded. Due to the time delay from the RC circuit of $R = 50\ k\Omega$ and

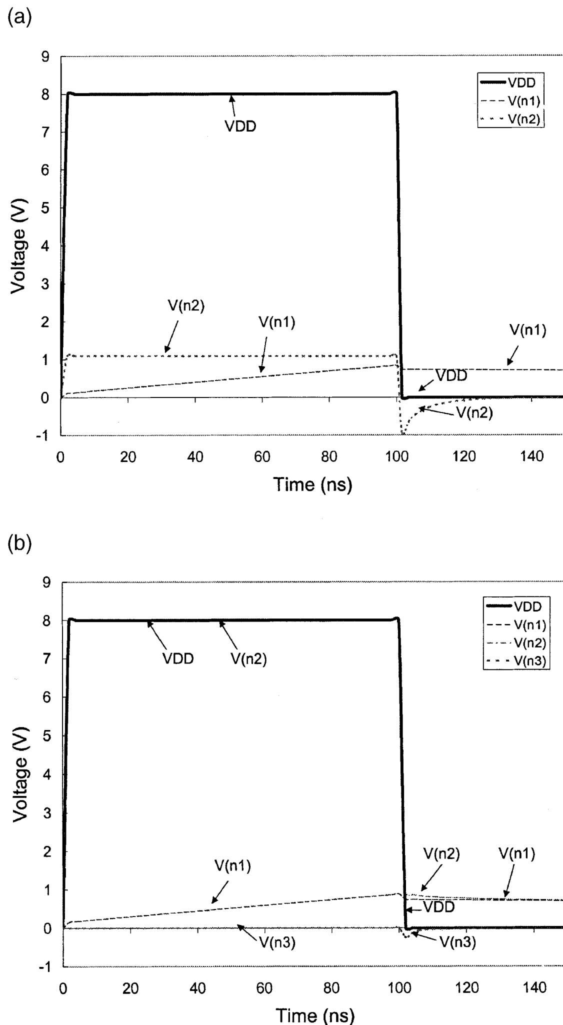

Fig. 8. The HSPICE simulated voltage waveforms for (a) the ESD clamp circuit with the STLB device, and (b) the ESD clamp circuit with the DTDB device, under the triggering of an 8-V voltage pulse with 100-ns pulse width and 2-ns rise time to simulate the ESD stress condition.

$C = 20$ pF, the voltage on the node n1 in Figs. 4(a) and 7(a) increases much slower than that on V_{DD} power line, as the V(n1) curves shown in Fig. 8(a) and (b), respectively. Because the node n1 is kept at a low-voltage level by the RC delay circuit, the PMOS (Mp1) of the inverter in the ESD-detection circuit is turned on simultaneously when the ESD pulse is applied on the V_{DD} power rail. Therefore, some ESD voltage is conducted from V_{DD} to the node n2, which is used to bias the base of the lateral n–p–n BJT in the STLB device in Fig. 4(a). The forward biased base–emitter junction of the STLB device limits the voltage level around ~1 V at the node n2, as the V(n2) curve shown in Fig. 8(a). With a base bias of ~1 V, the lateral n–p–n BJT in the STLB device can be strongly turned on to generate the desired discharging Path_2 in Fig. 2 to bypass the ESD current from V_{DD} to V_{SS}. Thus, the internal circuits can be effectively protected by such a power-rail ESD clamp circuit.

In Fig. 8(b), the V(n2) waveform is almost the same as that of V_{DD}, because the turned-on Mp1 of the first inverter charges up the node n2 (the input node of the second inverter) to the voltage level of V_{DD} in the ESD-detection circuit of Fig. 7(a). Therefore, the NMOS Mn2 of the second inverter is turned on to bias the node n3 at a voltage level of V_{SS}, as the V(n3) curve shown in Fig. 8(b). Because the node n3 is kept at voltage level of V_{SS} by the ESD-detection circuit, the n-well (base of the p–n–p BJT) in the DTDB device is biased at a low-voltage level in the ESD stress condition. The emitter of the p–n–p BJT in the DTDB device is directly connected to V_{DD} in Fig. 7(b), which is biased at a high-voltage level by the ESD energy. Therefore, the emitter–base junction of the p–n–p BJT is strongly forward biased to turn on the DTDB device for discharging the ESD current from V_{DD} to V_{SS}. From the simulated curves in Fig. 8(a) and (b), the proposed substrate-triggered devices can be quickly turned on by the ESD-detection circuits in Figs. 4(a) and 7(a), rather than by the junction breakdown. Thus, the internal circuits can be safely protected by such power-rail ESD clamp circuits.

3.2. V_{DD} power-on condition

A voltage ramp with a pulse height of 5 V and a rise time of 0.1 ms is used to simulate the rising edge of the normal V_{DD} power-on voltage waveform. The rise time of V_{DD} power-on transition is generally in the range of several milli-second (ms). The rise time of 0.1 ms used in this simulation is to verify that the substrate-triggered devices are not turned on in the power-on condition, even if the V_{DD} has a fast power-on transition. The simulated results on the power-rail ESD clamp circuits with the STLB and DTDB devices are shown in Fig. 9(a) and (b), respectively.

Because the time constant of 1 μs in the RC-based ESD-detection circuit, the voltage at node n1 can follow up the voltage increase with a rise time of ms on V_{DD} power rail. The simulated voltage waveform V(n1) in Fig. 9(a) is therefore the same as that of the applied V_{DD} power-on voltage waveform. The PMOS Mp1 in Fig. 4(a) is always off, because its V_{gs} is kept at 0 V during the V_{DD} power-on transition. With an increasing voltage level at node n1, the NMOS Mn1 is turned on to keep the V(n2) curve always at 0 V during the V_{DD} power-on transition. Therefore, the base of the n–p–n BJT, which is biased by the node n2, in the STLB device is biased at 0 V. So, the STLB device kept off during and after the V_{DD} power-on transition.

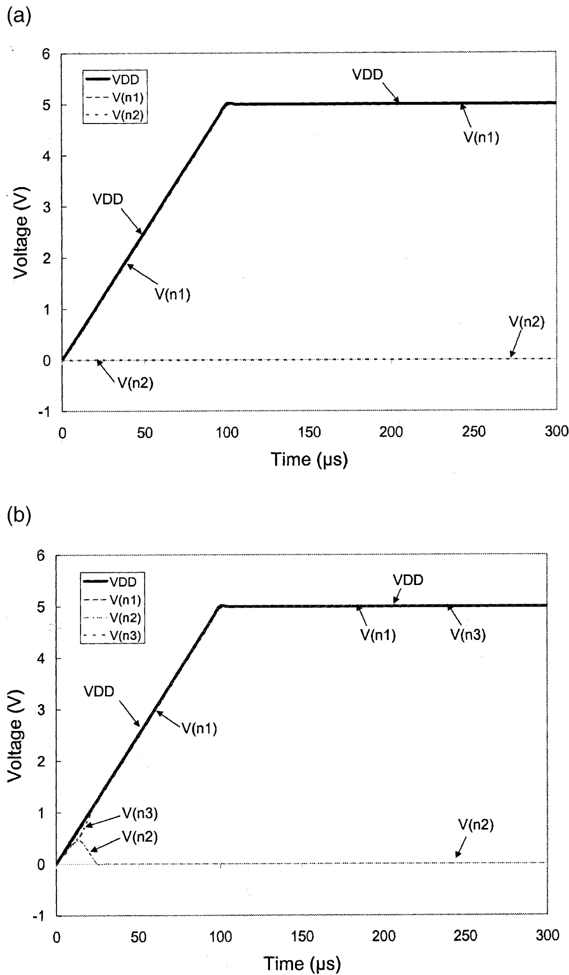

Fig. 9. The HSPICE simulated voltage waveforms for (a) the ESD clamp circuit with the STLB device, and (b) the ESD clamp circuit with the DTDB device, under the triggering of a 5-V ramp voltage with 0.1-ms rise time to simulate the V_{DD} power-on condition.

In Fig. 9(b), the simulated V(n1) has voltage waveform the same as that of V_{DD}. The V(n2) has a little voltage glitch (below 0.5 V) when the V_{DD} starts to increase. But, the V(n3) still has the voltage waveform almost the same as that of V_{DD}. The base voltage of the p–n–p BJT in the DTDB device is in Fig. 7(a) is biased by the node n3. Because the emitter–base junction bias of the p–n–p BJT in the DTDB device is kept at 0 V, the DTDB device is kept off during and after the V_{DD} power-on transition. From this simulation, such power-rail ESD clamp circuits are guaranteed to be kept off, when the IC is in the normal operating condition. This has verified the actual operation of the RC-based ESD-detection circuits, which are used to control the substrate-triggered devices on and off.

4. Experimental results

4.1. Device characteristics

The ESD clamp circuits with the proposed four substrate-triggered devices under different device sizes had been fabricated in a 0.6-µm non-silicided CMOS process. To find the I–V characteristics of these devices, every unit cell of the substrate-triggered devices is fabricated independently. The *Tektronix-370A* curve tracer is used to measure the I–V curves of the four substrate-triggered devices. The measured I–V curves of the STLB, STVB, STDB, and DTDB devices under different base current biases are shown in Fig. 10(a)–(d), respectively. In Fig. 10(a), the STLB device has the lowest snapback holding voltage (~7.6 V) and breakdown voltage (~12 V), as comparing to other three devices. In Fig. 10(b), the STVB device has the largest breakdown voltage (~37 V) among the four devices. The breakdown voltage of the STDB device is 14.4 V in Fig. 10(c), and that of the DTDB device is 14 V in Fig. 10(d). The I–V characteristics of the STDB device and DTDB device are similar, as shown in Fig. 10(c) and (d). But, the collector current of the DTDB device is more than that of the STDB device under the same base current bias. This is due to the contribution of the channel current of the PMOS in the DTDB device.

The beta gains among the four devices are also measured and compared in Fig. 11. In Fig. 11, the X-axis with a logarithm scale is the collector current of the devices, and Y-axis with a linear scale is the beta gain of the devices. The beta gain of STLB device becomes higher than 1, when the collector current is more than 12.7 mA. The beta gain of STVB device drops from 16 to become less than 1, when the collector current is increased more than 14.3 mA. The beta gain of STDB device drops from 18.5 to become less than 1, when the collector current is increased more that 38.4 mA. The beta gain of DTDB device drops from 49 to become less than 1, when the collector current is more than 42.4 mA. The DTDB structure with a collector current of 1 µA has a highest beta gain (~49) among these four devices. In the low-I_C region, the DTDB structure provides a high gain because the PMOS is also turned on. But in the high-I_C region, the beta gains of STVB, STDB, and DTDB devices are degraded to be below one. But, the beta gain of STLB becomes higher than one.

To investigate the leakage current of the proposed substrate-triggering devices when they are kept off, the *HP-4145* is used to measure the total leakage current of the fabricated ESD clamp circuits with proposed substrate-triggered devices. Under the normal V_{DD} bias of 5 V, the leakage currents of the ESD clamp circuits with the STLB (with a silicon area of 25 148 µm^2), the STDB (with a silicon area of 46 757 µm^2), and the DTDB (with a silicon area 46 757 µm^2) devices are all about 12.3 pA.

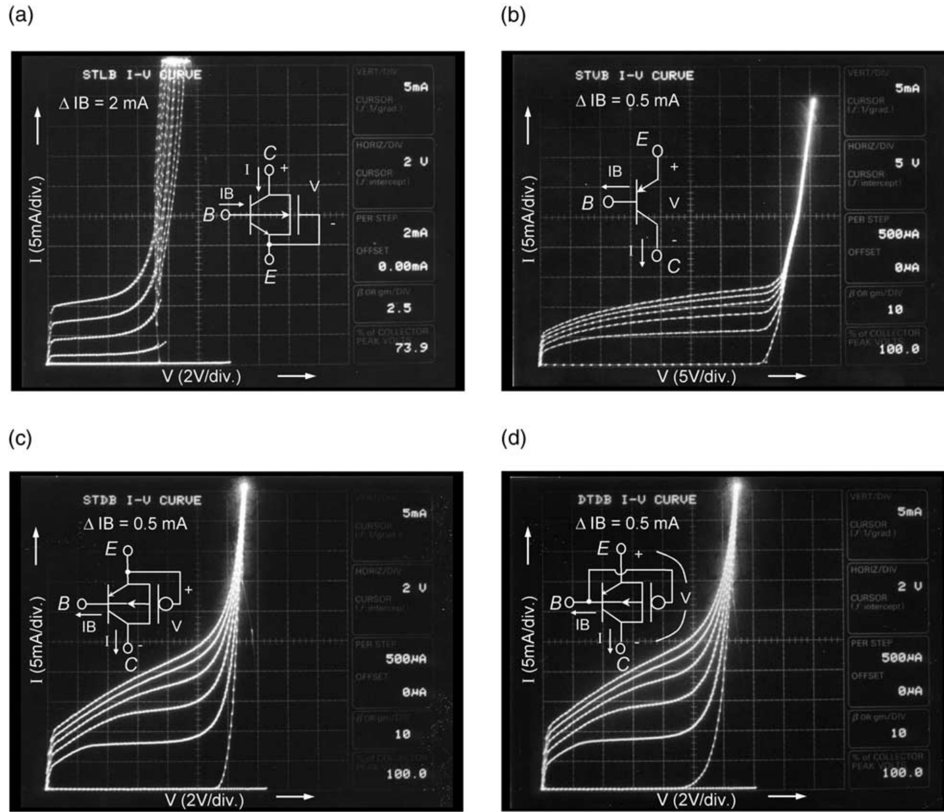

Fig. 10. The measured I–V curves of (a) STLB, (b) STVB, (c) STDB and (d) DTDB devices. (X scale in (a), (c) and (d) is 2 V/div.; X scale in (b) is 5 V/div.; Y scale is 5 mA/div.)

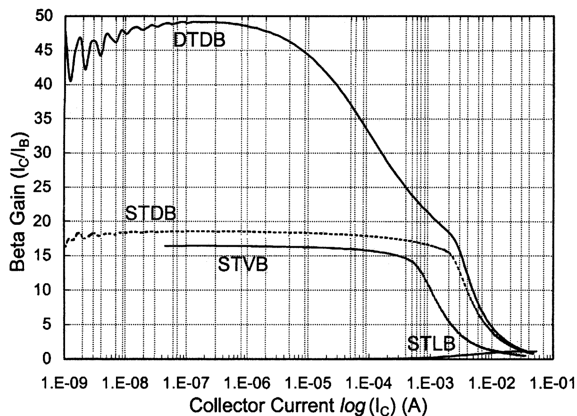

Fig. 11. The dependence of the beta gains on the collector currents among the STLB, STVB, STDB, and DTDB devices.

The leakage current of the ESD clamp circuit with STVB device (with a silicon area of 16 642 μm^2) is only 0.7 pA. With such a small leakage current in the order of several pA, the RC-based ESD detection circuit can indeed keep the substrate-triggered devices off when the IC is under normal V_{DD} bias.

4.2. ESD performance and TLPG I–V curves

The *KeyTek ZapMaster* is used to evaluate the ESD robustness of the fabricated ESD clamp circuits with the proposed substrate-triggered devices under different device dimensions. The applied HBM ESD voltages in the ESD tester are controlled from 200 to 1000 V with a step of 200 V and from 1000 to 8000 V with a step of 500 V. Every fabricated ESD clamp circuits in the testchip is placed in the stand-alone condition, where every power-rail ESD clamp circuit has its own V_{DD} power pad. The failure criterion to judge ESD level of the power-rail ESD clamp circuit is defined as 1-μA current leakage under a 5-V V_{DD} bias. The HBM ESD test results are summarized in Fig. 12(a) and (b). The relations between ESD robustness and channel width of the proposed ESD clamp devices are shown in Fig. 12(a). The dependence of ESD level on the device silicon area among the four ESD clamp devices is shown in Fig. 12(b). The HBM ESD test results of all STVB devices with different device dimensions can pass the stress of 1000 V, but they all fail when the HBM ESD voltage is over 1000 V. The breakdown of the vertical p–n–p bipolar transistor in the STVB device causes the ESD current mainly flowing

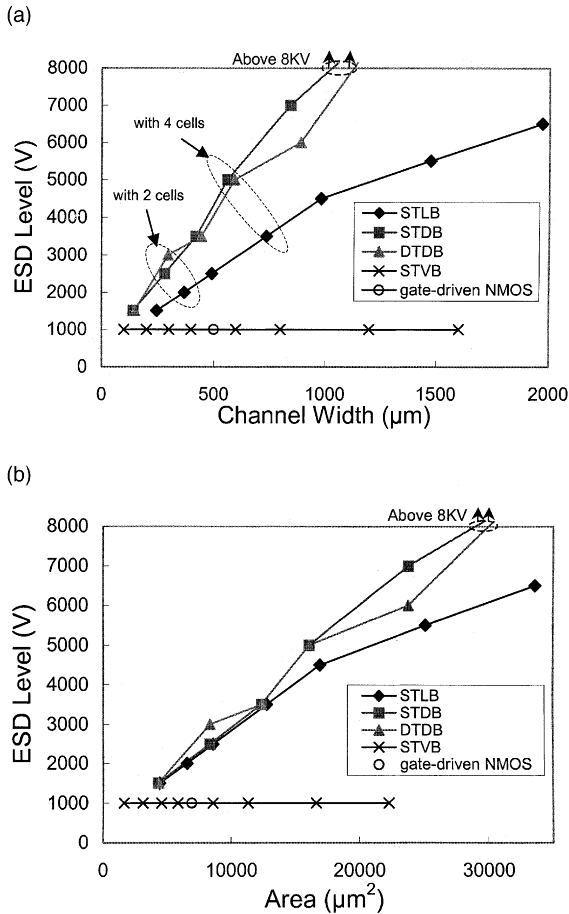

Fig. 12. The dependence of the HBM ESD level on (a) the channel width, and (b) the silicon area, of the power-rail ESD clamp circuits with different protection devices.

form the contact of p^+ diffusion (emitter) into the p-substrate (collector). In this vertical p–n–p bipolar transistor, the base width, between the junction depths of the n-well and p^+ diffusion, is kept the same by the CMOS process. Therefore, even if the STVB has a wide layout area, its base width is still kept the same. Because the ESD current on STVB device is mainly discharged through its base region to the grounded p-substrate, the STVB devices with different layout areas have the same low-ESD level (~1000 V) when the narrow base region is damaged by ESD energy. From Fig. 12(b), the ESD clamp circuits with the STLB, the STDB, or the DTDB structures can sustain higher ESD level in per silicon area. The average ESD robustness in per silicon area of both the STDB and DTDB device is about 0.30 V/μm², and that of the STLB is about 0.26 V/μm². The ESD clamp circuit with the STVB device only sustains a low-ESD level of 1000 V even if it was drawn with a larger device dimension and a large silicon area.

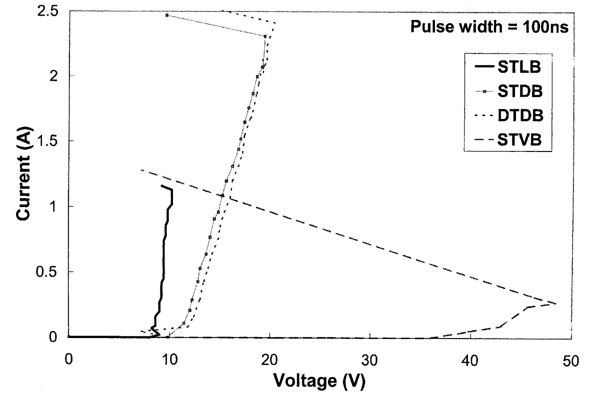

Fig. 13. The TLPG measured I–V curves of the substrate-triggered devices under 0-V substrate bias.

To investigate the snapback characteristics of devices during ESD transition, the transmission line pulsing generator (TLPG) system [34] is used to measure the secondary breakdown currents (I_{t2}) of the four substrate-triggered devices. The TLPG-measured results are shown in Fig. 13. From the experimental results, the STVB device with a silicon area of 4548 μm² has a much smaller I_{t2} of only 0.26 A. The STVB device in the 0.6-μm CMOS process has the lowest ESD roubustness and the largest breakdown voltage, as compared to the other three devices. This means that the STVB device has a lower ESD roubustness, even if the STVB device is triggered by the substrate-triggering design.

From Fig. 13, the STDB and DTDB devices with a silicon area of 12 352 μm² have the I_{t2} of 2.31 and 2.41 A, respectively. The STLB device with a silicon area of 6546 μm² has the I_{t2} of 1.16 A. Then, the I_{t2} in per silicon area of the STLB, STDB, and DTDB devices in the 0.6-μm CMOS technology can be calculated as 177, 187, and 195 μA/μm², respectively. The relation between the HBM ESD level and the secondary breakdown current I_{t2} (which is measured by TPLG with a pulse width of 100 ns) can be written as [35]:

$$\text{HBM ESD level} \approx I_{t2} \times (1500\ \Omega + R_{\text{device}}). \quad (1)$$

The R_{device} is the turn-on resistance of the test device under ESD stress. Generally, the turn-on resistance of an ESD clamp device is much smaller than the HBM resistance of 1500 Ω. The average HBM ESD level of the ESD clamp circuits with the STLB, STDB, and DTDB devices are nearly equal to the product of I_{t2} with the HBM resistance of 1500 Ω in this experimental result.

The traditional power-rail ESD clamp circuit in Fig. 3 with an NMOS by gate-driven design is also fabricated in the same process. With a device dimension (W/L) of 500/1.0 (μm/μm) for the gate-driven NMOS, which occupies a layout area of 6931 μm², this traditional design of Fig. 3 can sustain an HBM ESD level of only 1000 V.

The ESD roubustness in per silicon area of the NMOS is only 0.14 V/μm^2, but that of the STLB is improved to 0.26 V/μm^2. This verifies that the substrate-triggered technique can effectively improve ESD level of the NMOS. With the substrate-triggered technique, the STDB and DTDB devices can provide about two-times greater ESD level in per silicon area than the gate-driven NMOS.

From the measured results on the ESD level and the secondary breakdown current, the STLB, STDB, and DTDB devices with the substrate-triggered design and the cell-based layout method can significantly increase their ESD robustness in a limited silicon area.

4.3. Turn-on verification

To verify the turn-on efficiency of the power-rail ESD clamp circuits, a voltage pulse with a rise time around 5–10 ns and a pulse width of 400 ns applied to the V_{DD} of the ESD clamp circuits with the V_{SS} grounded to simulate the ESD-stress condition. The experimental setup to verify the turn-on efficiency for the ESD clamp circuits with the STLB, STVB, STDB, or DTDB devices is shown in Fig. 14(a). The original waveform of the voltage pulse generated from a pulse generator to investigate the turn-on efficiency of these ESD clamp circuits is shown in Fig. 14(b). The voltage waveform on the V_{DD} node is observed to find the turn-on behavior of the ESD clamp circuits. When the 8-V voltage pulse is applied, the voltage waveforms on the V_{DD} of the ESD clamp circuits with the STLB, STVB, STDB, and DTDB devices are measured and shown in Fig. 14(c)–(f), respectively. The 0–8 V voltage pulse is clamped by the turned-on ESD-clamp device (STLB, STVB, STDB, or DTDB), therefore the voltage pulse is degraded to a certain voltage level. When the capacitor C (node n1) in the RC-based ESD-detection circuit is charged up, the ESD-detection circuit will turn off the ESD-clamp device. Then, the voltage waveform is restored to the original voltage level. Therefore, the period of the degraded voltage waveform can be defined as the turn-on time of the ESD-clamp devices in the power-rail ESD clamp circuits, which is marked as t_{on} in Fig. 14(c)–(f).

The turn-on time in Fig. 14(f) for the power-rail ESD clamp circuit with the DTDB device is about 140 ns. The turn-on time of the power-rail ESD clamp circuit is varying if the applied voltage pulse has different pulse heights. The relations between the turn-on time and the pulse height of the applied voltage pulse among the ESD clamp circuits with the four substrate-triggered devices are measured and summarized in Fig. 15. From the experimental results, the turn-on times of these ESD clamp circuits are around 150–210 ns when the pulse height has a voltage of 10 V. The turn-on time of the ESD clamp circuit is almost linearly increased while the pulse height of the applied voltage pulse increases. This is due to the longer delay time to charge up the capacitor C in the RC-based ESD-detection circuit to a voltage level that causes the inverter changing its output state, when the applied voltage pulse has a higher voltage level.

A 5-V ramp voltage with a rise time of 0.1 ms is also applied to the V_{DD} (with the V_{SS} grounded) to verify whether the ESD clamp circuits are kept off in the normal V_{DD} power-on condition. When the 0–5 V ramp voltage waveform is applied to the V_{DD} of the ESD clamp circuits with the STLB, STVB, STDB, or DTDB devices, no degradation is found on the applied voltage waveform during this V_{DD} power-on condition. Therefore, the ESD clamp circuits with the proposed four substrate-triggered devices are really kept off in the normal V_{DD} power-on condition.

4.4. Power-rail noise clamping

When the IC is in the normal operation condition with 5-V V_{DD} and 0-V V_{SS} power supplies, there are some system-level or board-level noise pulses coupled to the power lines to generate the overshooting noise pulse across the power lines. Such an overshooting noise pulse may initiate the occurrence of latchup in the CMOS ICs to burn out the ICs [21,22]. The ESD clamp circuits with proposed substrate-triggered devices can be also triggered on to clamp such an overshooting noise pulse on the V_{DD} power line. Therefore, the IC protected by such power-rail ESD clamp circuits has a high immunity to the transient-induced latchup. To verify this noise-clamping efficiency of the power-rail ESD clamp circuits with the proposed substrate-triggered devices, a 5–12 V overshooting voltage pulse is added to the 5-V V_{DD} power line of the power-rail ESD clamp circuits. The experimental setup to investigate the noise-clamping efficiency of the power-rail ESD clamp circuits is shown in Fig. 16(a). The original overshooting noise pulse with a rise time of $\sim$10 ns and a pulse width of 200 ns generated from a pulse generator is shown in Fig. 16(b). The overshooting voltage waveforms clamped by the power-rail ESD clamp circuits with the STLB and DTDB devices are shown in Fig. 16(c) and (d), respectively.

In Fig. 16(c), the 5–12 V overshooting voltage pulse is clamped by the STLB to the voltage level of 9.2 V, which is near to its snapback holding voltage. But after the triggering of the 5–12 V overshooting voltage pulse, the V_{DD} voltage level is restored to the original 5 V. In Fig. 16(d), the 5–12 V overshooting voltage pulse is initially clamped by the DTDB device to the voltage level around 10 V, which is dependent on the device dimension of the DTDB device. A larger device dimension causes a lower clamped voltage level on the overshooting noise pulse. A larger RC time constant in the control circuit causes a longer turn-on time on the DTDB device to clamp the overshooting noise pulse. After the triggering of the 5–12 V overshooting voltage

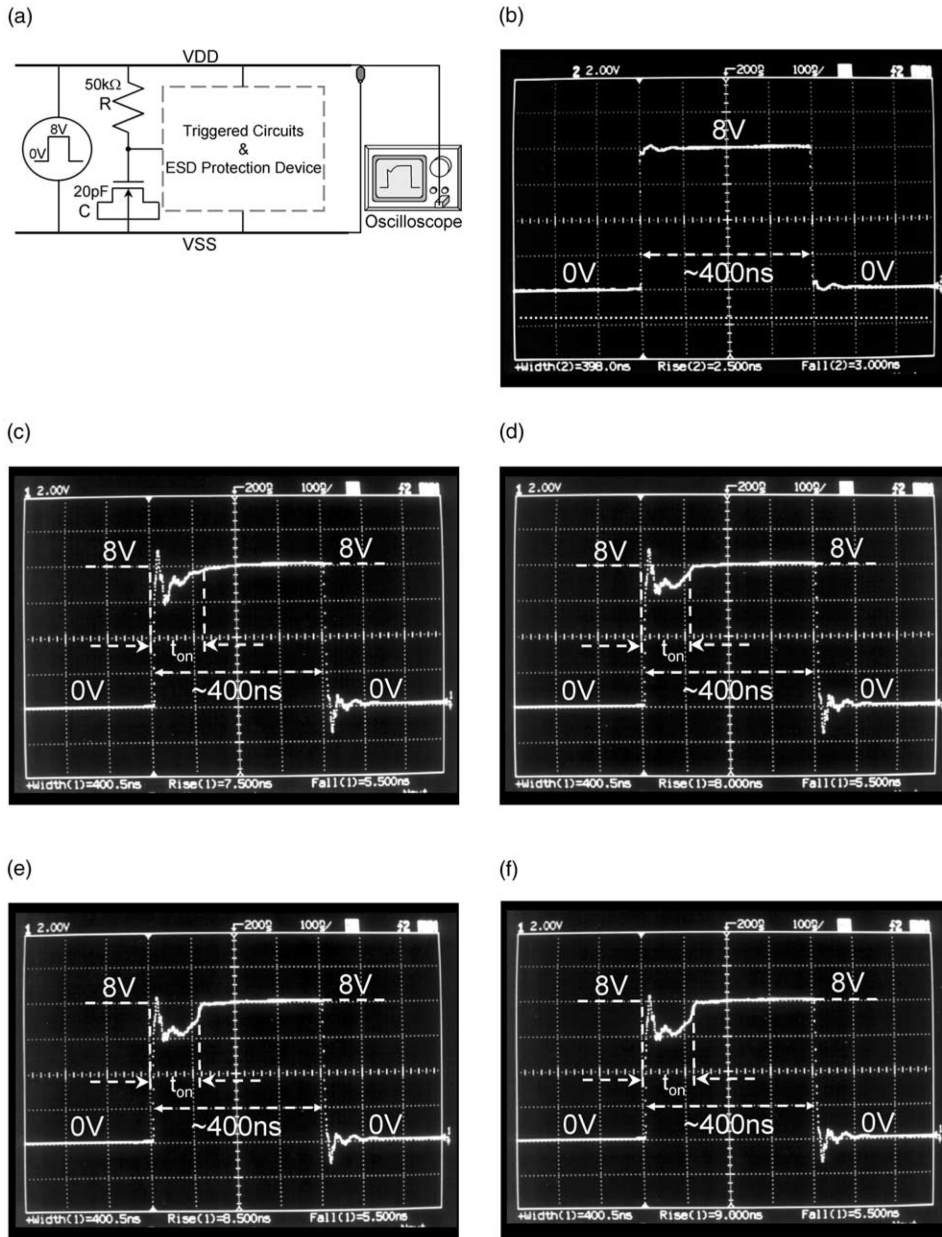

Fig. 14. (a) The experimental setup to verify the turn-on behavior of the power-rail ESD clamp circuits under ESD-stress condition. (b) The original 8-V voltage pulse generated from a pulse generator. The degraded voltage waveforms clamped by the power-rail ESD clamp circuits with the (c) STLB, (d) STVB, (e) STDB, and (f) DTDB devices. (X scale: 100 ns/div.; Y scale: 2 V/div.)

pulse, the V_{DD} voltage levels are restored to the original 5 V. The 5–12 V overshooting voltage pulse clamped by the STVB or STDB devices is almost the same as that clamped by the DTDB device. This verifies that the power-rail ESD clamp circuits with the substrate-triggered devices have the benefit to clamp the overshooting noise pulse on the V_{DD} power line. After the noise transition, the power-rail ESD clamp circuits can turn-off automatically to avoid current leaking from V_{DD} to V_{SS} through the power-rail clamp circuits.

5. Conclusion

Area-efficient power-rail ESD clamp circuits with four different substrate-triggered devices have been prac-

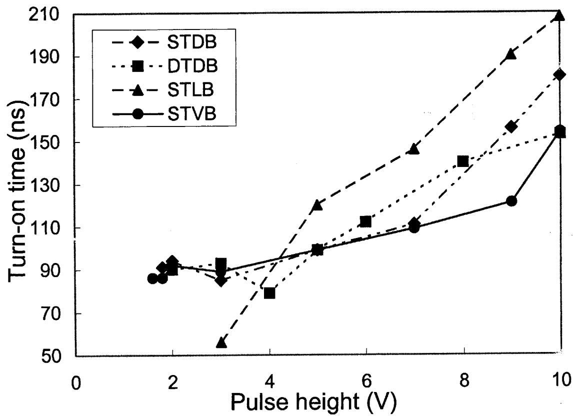

Fig. 15. The relations between the turn-on time and the pulse height of the applied voltage pulses on the power-rail ESD clamp circuits with different protection devices.

tically investigated in a 0.6-μm CMOS process. By using the substrate-triggered technique, the DTDB, STDB, and STLB devices can provide much higher ESD robustness within a smaller layout area, as compared to the traditional design with the gate-driven NMOS device. The STDB and DTDB devices with the parasitic vertical BJT have higher ESD robustness. But, a pure vertical p–n–p BJT in the 0.6-μm CMOS process even with a large device size still sustains a low-HBM ESD level, due to higher breakdown voltage and the lower secondary breakdown current of the STVB device. To improve ESD robustness of an on-chip ESD protection circuit in a limited silicon area, the DTDB device has the best performance among these four substrate-triggered devices. With suitable design on both the bipolar structure in the ESD-clamp device and the substrate-triggered technique, the layout area of the ESD clamp circuit to achieve whole-chip ESD protection can be efficiently reduced to save the silicon cost of CMOS ICs.

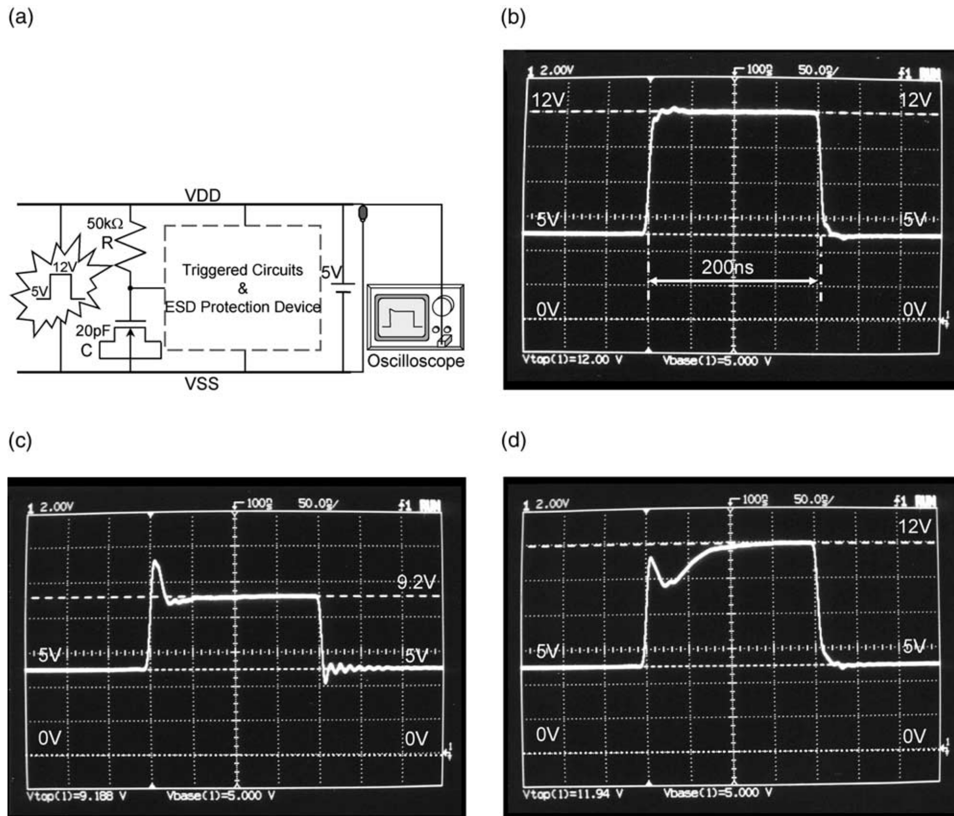

Fig. 16. (a) The experimental setup to verify the noise-clamping efficiency of the power-rail ESD clamp circuits when the IC is in the normal operating condition with 5-V V_{DD} power supply and an overshooting noise pulse. (b) The original voltage waveform of a 5–12 V overshooting noise pulse. The degraded voltage waveforms of the 5–12 V overshooting noise pulse clamped by the power-rail ESD clamp circuits with the (c) STLB and (d) DTDB devices. (*X* scale: 50 ns/div.; *Y* scale: 2 V/div.)

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