Anomalous Variations of OFF-State Leakage Current in Poly-Si TFT Under Static Stress

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***Abstract*—In this letter, we study the anomalous variations of the OFF-state leakage current ($I_{\rm OFF}$) in n-channel poly-Si thin-film transistors (TFTs) under static stress. The dominant mechanisms for the anomalous $I_{\rm OFF}$ can be attributed to 1) $I_{\rm OFF}$ increases due to channel hot electrons trapping at the gate oxide/channel interface and silicon grain boundaries and 2) $I_{\rm OFF}$ decreases due to hot holes accumulated/trapped near the channel/bottom oxide interface near the source region. Under the stress of high drain bias, serious impact ionization effect will occur to generate hot electrons and hot holes near the drain region. Some of holes will be injected into the gate oxide due to the vertical field ($\sim$(V_Gstress$-$V_Dstress)$/T_{\rm OX}$) near the drain and the others will be migrated from drain to source along the channel due to lateral electric field ($\sim$V_Dstress$/L_{\rm CH}$).**

***Index Terms*—OFF-state leakage current ($I_{\rm OFF}$), impact ionization, poly-Si TFT.**

I. Introduction

POLY-Si TFTs have been greatly studied for applications in static random access memories (SRAMs) and active matrix liquid crystal displays (AMLCDs). Although the mobility of poly-Si TFTs is much higher than that of amorphous TFTs, the high OFF-state leakage currents in poly-Si TFTs are also unavoidable [1]. It has been reported that the OFF-state leakage currents can be attributed to the thermal generation effect at low gate-drain electric field and to the electric field effect at high gate-drain electric field in the channel [2], [3]. Several investigations have been already carried out to study the ON-state degradation under static stress in poly-Si TFTs [4], [5]. However, to our knowledge, the variations of the OFF-state leakage currents under static stress are not yet well defined. The object of this work is to study the anomalous variations of the OFF-state leakage currents in poly-Si TFTs under static stress. Forward and reverse mode measurements are used for the OFF-state leakage currents in drain and source regions, respectively.

II. Experiment

Low-temperature processed (<600 °C) n-channel poly-Si TFTs are used in this work. The physical device parameters are 56 nm-thick PECVD gate oxide deposited at 350 °C, 100 nm-thick active channel, channel width $W_{\rm CH} = 5$ μm, and channel length $L_{\rm CH} = 10$ μm. The active channel was deposited from the decomposition of Si_2H_6 in LPCVD system at 460 °C and then crystallized at 600 °C for 24 h. The measured average grain size is 1.1 μm. After completing the device fabrication, no hydrogenation step was performed.

In this letter, the static stress is used to degrade the poly-Si TFTs. The gate potential $V_{\rm GS}$ fixed at 20 V ($V_Gstress = 20$ V) and the drain potential $V_{\rm DS}$ ranged from 20 V to 32 V ($V_Dstress = 20$ V–32 V). $I_{\rm OFF}$ was measured at $V_{\rm GS} = -15$ V and $V_{\rm DS} = 2$ V. Forward mode and reverse mode measurements are used to characterize $I_{\rm OFF}$ variations at the drain side and at the source side, respectively. In the forward mode, the source and drain connections are the same as during stress, while in the reverse mode, they are swapped.

III. Results and Discussion

Figs. 1 and 2 show the $I_{\rm OFF}$ variations under forward mode and reverse mode measurements for $V_Dstress$ ranging from 20 V to 32 V, respectively. Insert plots are the $I_{\rm DS}$–$V_{\rm GS}$ characteristics of poly-Si TFTs before and after static stress for forward mode and reverse mode measurements, respectively. Less $I_{\rm OFF}$ variations can be observed at -7 V $< V_{\rm GS} < -1$ V, while anomalous $I_{\rm OFF}$ variations can be observed at $V_{\rm GS} < -7$ V. For forward mode measurements at $V_Dstress = 20$ V, $I_{\rm OFF}$ is almost unchanged initially and then increased after 100 s. This implied that the device was less degraded at the initial stage, while the increase of $I_{\rm OFF}$ was due to the channel hot electrons trapped in the pre-existed traps (acceptor-like trap states) at the gate oxide/channel interface and silicon grain boundaries or due to the weak bonds (Si-H, distorted Si-Si, and distorted Si-O) broken caused by the channel hot electrons near drain. The trapped electrons at the interface increase the vertical electric field near drain to increase $I_{\rm OFF}$ [6]. However, for $V_Dstress = 22$ V in forward mode measurements, $I_{\rm OFF}$ increases at the initial stage and finally reaches saturation after 1000 s. The saturated $I_{\rm OFF}$ is due to the increase of injection efficiency for hot holes injection into the gate-oxide near drain. Under the stress conditions of high drain bias, serious impact ionization effect will occur to generate hot electrons and hot holes near the drain region. Some of holes will be injected into the gate oxide, and the other holes will migrate to the minimum of potential within the channel. Therefore, some of holes are trapped at the gate oxide/channel interface near drain and the other are accumulated/trapped at the channel/bottom oxide interface near source. Therefore, in reverse mode measurements, $I_{\rm OFF}$ initially increases due to

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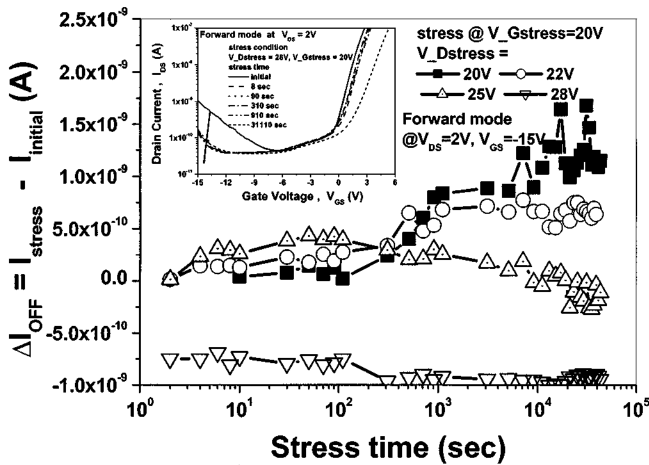


Fig. 1. Variations of OFF-state leakage currents under static stress for forward mode measurements. The insert plots are the $I_{\rm DS}$–$V_{\rm GS}$ characteristics of poly-Si TFT before and after static stress for forward mode measurements.

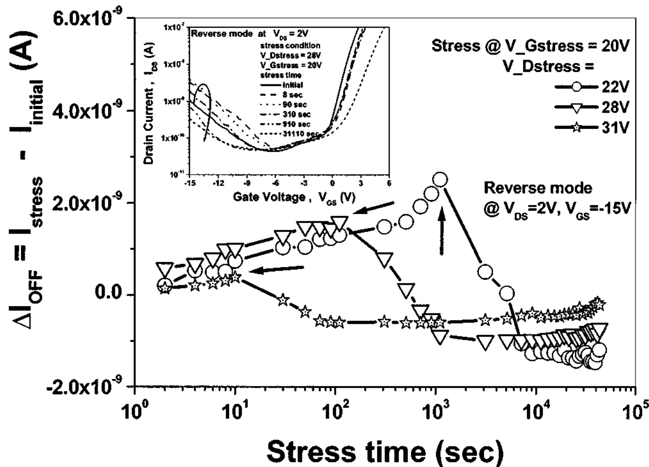


Fig. 2. The variations of OFF-state leakage currents under static stress for reverse mode measurements. The insert plots are the $I_{\rm DS}$–$V_{\rm GS}$ characteristics of poly-Si TFT before and after static stress for reverse mode measurements.

hot electrons injection into the gate oxide near source and then starts to decrease after the turnaround point due to hot holes accumulated/trapped at the channel/bottom oxide interface.

Fig. 3 shows the degradation of the threshold voltage $(\Delta V_{\rm TH})$ as a function of stress time and the insert plots are the variations of the maximum transconductance (ΔG_m). Both $\Delta V_{\rm TH}$ and ΔG_m show that the degradation is proportional to the square root of time. It has been reported that the acceptor-like trap states at gate oxide/channel interface are the dominating factor for $\Delta V_{\rm TH}$ and ΔG_m [7]. Therefore, acceptor-like trap states are generated at the gate oxide/channel interface and silicon grain boundaries.

Fig. 4(a) shows the schematic diagram of the poly-Si TFTs degradation under static stress. The hot holes and electrons are generated from the impact ionization near the drain at high drain bias conditions. The injection efficiency into the gate oxide for hot holes and electrons depends on the vertical electric field near the drain $(\sim(V_Gstress - V_Dstress)/T_{\rm OX})$ and source $(\sim V_Gstress/T_{\rm OX})$ [3]. At $V_Gstress = 20$ V and

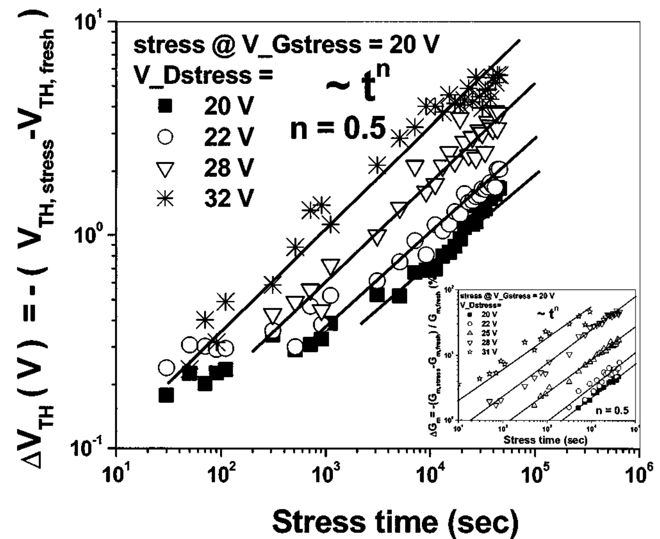
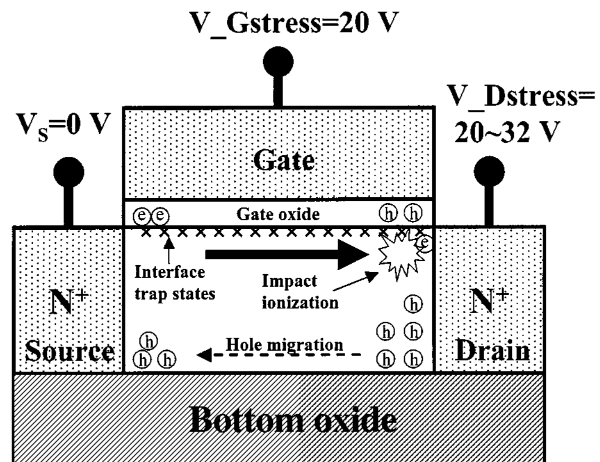


Fig. 3. Variations of the threshold voltage shifts as a function of the stress time. The insert plots are the variations of the maximum transconductance as a function of the stress time.



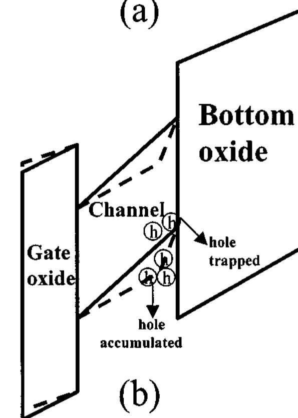


Fig. 4. (a) Schematic diagram of the poly-Si TFTs degradation under the static stress and (b) the schematic energy band diagram for hot holes accumulated/trapped at the channel/bottom oxide interface.

$V_Dstress = 20$ V–25 V, the vertical field near drain is small for holes injection into the gate oxide. Thus, the increased $I_{\rm OFF}$ in forward mode measurements are due to hot electrons trapped by the acceptor-like trap states at the gate oxide/channel

interface and silicon grain boundaries (Fig. 1). On the other hand, the vertical field near source is high and favoring electrons injection into the gate oxide to increase I_{OFF} in reverse mode measurements (Fig. 2). Therefore, I_{OFF} in reverse mode measurements increases initially. Once the number of holes migrated from drain to source are larger than those of electrons trapped in the gate oxide, I_{OFF} starts to decrease and the turnaround points in Fig. 2 can be observed. The path for holes migration is along the channel/bottom oxide interface because of the lowest potential for holes. The holes migrated from drain to source are accumulated and some are trapped at the channel/bottom oxide interface [8]. At $V_Gstress = 20$ V and $V_Dstress = 25$ V–32 V, the vertical electric field near drain is moderate and favoring holes injection into the gate oxide to lower I_{OFF} in forward measurements. Under higher drain bias conditions, a greater number of holes will be generated by the impact ionization [9] and the lateral electric field along channel $(\sim V_Dstress/L_{\mathrm{CH}})$ is also enhanced. Therefore, more number of holes with higher migration speed from drain to source will be accumulated/trapped at channel/bottom oxide interface near the source. Moreover, the time required for turnaround points are decreased as can be expected and seen in Fig. 2. Fig. 4(b) shows the schematic energy band diagram for the hot holes accumulated/trapped at the channel/bottom oxide interface. Because the electric field near the gate oxide/channel interface can be reduced, the I_{OFF} induced by the high electric field can be also reduced.

IV. Conclusion

The anomalous I_{OFF} variations in poly-Si TFTs under static stress are studied. Under low $V_Dstress$, the increased I_{OFF} in forward mode measurements are due to hot electrons trapped by the acceptor-like trap states at the gate oxide/channel interface and silicon grain boundaries. Under high $V_Dstress$, the lower I_{OFF} in forward measurements can be attributed to the fact that the vertical electric field near drain is moderate and favoring holes injection into the gate oxide. Moreover, the holes accumulated/trapped at the channel/bottom oxide interface near the source are the dominating factors for lowering I_{OFF} in reverse mode measurements.

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