Bi 3.25 La 0.75 Ti 3 O 12 thin films on ultrathin Al 2 O 3 buffered Si for ferroelectric memory application

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Citation: Applied Physics Letters **80**, 3168 (2002); doi: 10.1063/1.1471937
View online: http://dx.doi.org/10.1063/1.1471937
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/80/17?ver=pdfcov
Published by the AIP Publishing

$Bi_{3.25}La_{0.75}Ti_3O_{12}$ thin films on ultrathin Al_2O_3 buffered Si for ferroelectric memory application

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(Received 4 June 2001; accepted for publication 20 February 2002)

We have investigated the physical and electrical properties of $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) thin films on $Pt/Ti/SiO_2/Si$ and on $Al_2O_3(6\,nm)/Si$, which are used for one-transistor-one-capacitor and one-transistor ferroelectric memory, respectively. The BLT thin films on both substrates show good capacitance–voltage characteristics and the same threshold voltage shift of 1.6 V at applied ± 10 V bias. However, the leakage current of BLT on Al_2O_3/Si at -100 kV/cm is two orders of magnitude lower than that on Pt. The comparable memory characteristics and much reduced leakage current of BLT on Al_2O_3/Si are the strong advantages as compared with BLT on Pt because it is directly related to switching energy and device scaling down. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1471937]

Ferroelectric random access memory (FRAM) has attracted much attention recently because of better speed performance than Flash memory and smaller size than static RAM.[1] The current cell structure of FRAM is one transistor and one capacitor (1T-1C) type where the data are memorized in the metal/ferroelectric/metal (MFM) capacitor.[2–6] To utilize the full advantage of FRAM, one transistor (1T) ferroelectric metal-oxide-semiconductor field effect transistor (FeMOSFET)-type memory is desirable because of the same small 1T cell structure as Flash memory. Further, the ferroelectric effect induced voltage can be amplified by the transistor in 1T MOSFET cell that gives higher sensitivity than 1T-1C cell. Unfortunately, the progress of 1T FeMOSFET memory is obstructed by the strong interface reaction between most ferroelectric materials and Si that greatly degrades the device characteristics.[7,8] Recently, we have developed 1T FeMOSFET memory using Al_2O_3[9,10] as both gate dielectric for MOSFET and interface reaction barrier between ferroelectric $Pb(Zr,Ti)O_3$ (PZT) and Si. Good transistor and memory characteristics are obtained simultaneously because of good gate dielectric integrity and interface property of Al_2O_3.[9,10] In this letter, we have investigated the stacked gate dielectric of $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT)/Al_2O_3 on Si because BLT is another promising ferroelectric material with excellent nonfatigue behavior on Pt electrode.[11]

Four-inch, *p*-type (100) Si wafers with $\sim 10\ \Omega$ cm resistivity were used in this study. For the MFM structure, a 150-nm-thick Pt was first deposited on $Ti(20\,nm)/SiO_2(200\,nm)/Si$ as the bottom electrode. For the FeMOS structure, a 6-nm-thick Al_2O_3 gate dielectric was first formed on Si and the detailed formation procedure was reported previously.[9,10] Then BLT was deposited on both $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si by chemical solution deposition using spin coating at 4000 rpm for 30 s.[5,6] For the chemical solution synthesis, bismuth acetate, lanthanum acetate hydrate, and titanium n-butoxide were used as precursors and dissolved in the solvents composed of acetic acid, 2-methoxythanol, and glycerol in sequence. Excess 10% Bi precursor was added to compensate for the Bi loss during annealing. After each coating, the wet films were pyrolyzed for several minutes and the formed multilayer films were annealed at 650 °C for 1 h. Au was used as upper electrode for both capacitor structures and Al bottom electrode was used for FeMOS capacitor at the bake side of Si substrates. The total thickness of BLT is about 420 nm as measured by cross-sectional scanning electron microscopy (SEM) images and the capacitor area is 9×10^{-4} cm^2. The phase and surface microstructure of BLT films were observed by x-ray diffraction (XRD) and SEM. Transmission electron microscopy (TEM) was used to investigate the interface characteristics of BLT film grown on Al_2O_3/Si. The electrical properties were characterized by capacitance–voltage ($C-V$) and current density–voltage ($J-V$) by using Hewlett Packard 4284 and 4155B, respectively.

Figures 1(a) and 1(b) show the XRD patterns of BLT thin films deposited on $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si, respectively. As shown in Fig. 1(a), BLT on Pt is polycrystalline without preferred orientation,[12] even though the bottom Pt has preferred (111) orientation. In the case of BLT deposited on amorphous Al_2O_3 shown in Fig. 1(b), the structure is also polycrystalline and the XRD pattern is almost the same as that on Pt. Thus, high quality ferroelectric BLT can be formed on both polycrystalline Pt and amorphous Al_2O_3.

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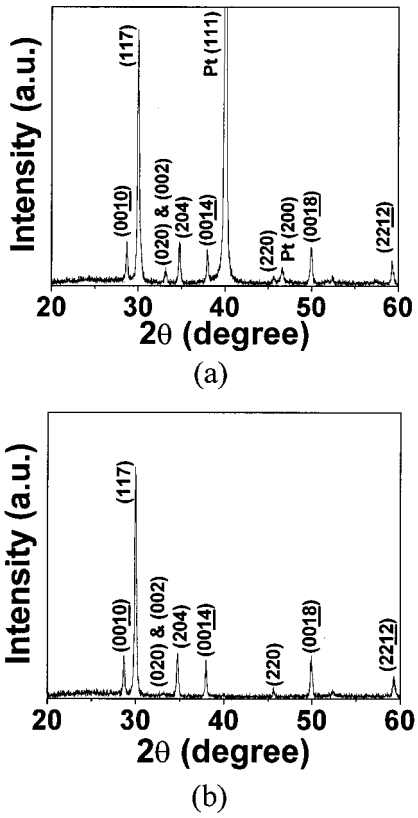

FIG. 1. XRD patterns of BLT on (a) $Pt/Ti/SiO_2/Si$ and (b) Al_2O_3(6 nm)/Si.

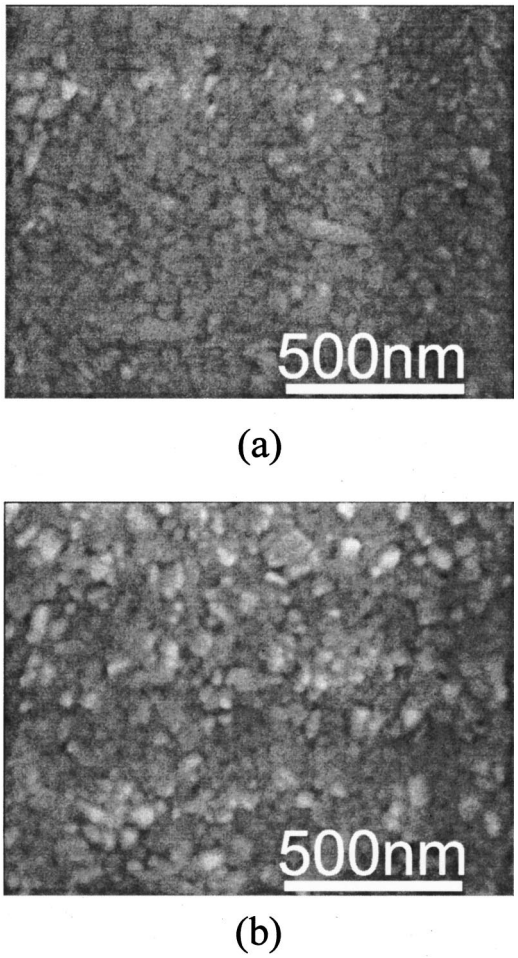

FIG. 2. SEM images of BLT on (a) $Pt/Ti/SiO_2/Si$ and (b) Al_2O_3(6 nm)/Si.

We have also examined the microstructures of BLT thin films deposited on $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si by SEM, and the images are shown in Figs. 2(a) and 2(b), respectively. The grain sizes of BLT on $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si are almost the same, about 50 nm, even though the structure of Pt substrate is polycrystalline that is quite different from amorphous Al_2O_3. The near same grain size of BLT on $Pt/Ti/SiO_2/Si$ or Al_2O_3/Si observed by SEM is consistent with the XRD analysis shown in Fig. 1, which suggests that BLT on both substrates may have close material quality.

Figure 3 shows the cross-sectional TEM picture of the $BLT/Al_2O_3/Si$ structure and reveals only a slight interface layer on the top of Al_2O_3. One possible reason may be due to the fact that the atoms in BLT diffuse to Al_2O_3 gate dielectric. This result is in sharp contrast to the obvious thick intermediate amorphous layer reported by Choi *et al.*,[13] which may be due to the difference in substrate temperature between pulsed ablation deposition and chemical solution deposition. Without the appearance of thick amorphous layer, the ferroelectric BLT film could directly come in contact with the buffer layer this indicates the better interface between them since the memory performance of capacitors may be improved.

We have further studied the memory properties using high frequency (1 MHz) $C-V$ measurement, and Figs. 4(a) and 4(b) show the $C-V$ characteristics of BLT on $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si, respectively. As shown in Fig. 4(a) the $C-V$ characteristics of BLT on Pt have the typical butterfly pattern, which is similar to that of other ferroelectric materials.[14] After ± 10 V applied voltages, a peak voltage difference of 1.6 V is obtained that is due to the polarization effect of BLT. For BLT on Al_2O_3/Si, the hysteresis $C-V$ curves shown in Fig. 4(b) are related to the ferroelectric properties of BLT because Al_2O_3 gate dielectric has negligible hysteresis.[9,10] The decrease of capacitance value at positive gate bias in the FeMOS structure is due to the small series capacitance in Si depletion region. The phenomenon is different from that in the MFM structure because of the negligible depletion width in metal. A threshold voltage shift of 1.6 V is measured for BLT on Al_2O_3/Si that is the same as that in MFM capacitor. The same voltage shift suggests that the electric memory property of BLT on Al_2O_3/Si is at least the same or even better than that on Pt because of the additional voltage drop in Al_2O_3 gate dielectric and reduced electric field in BLT.

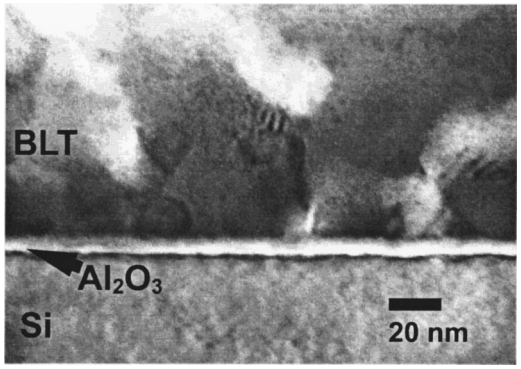

FIG. 3. Cross-sectional TEM image of BLT on Al_2O_3(6 nm)/Si.

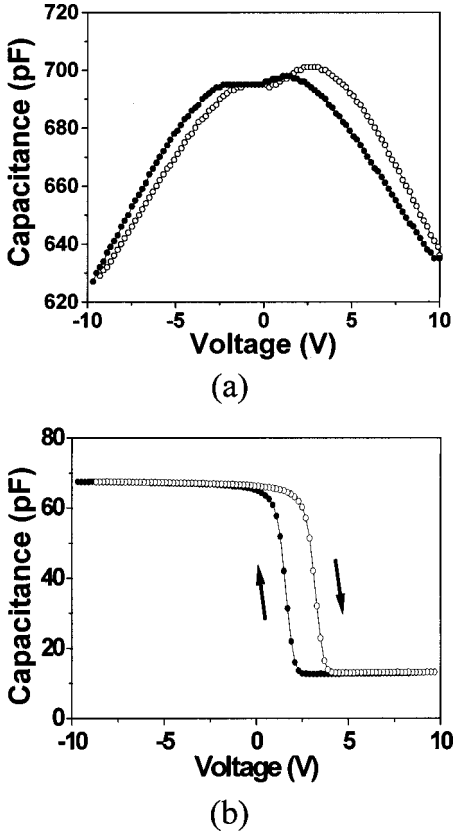

FIG. 4. $C-V$ characteristics of BLT on (a) $Pt/Ti/SiO_2/Si$ and (b) $Al_2O_3(6\ nm)/Si$.

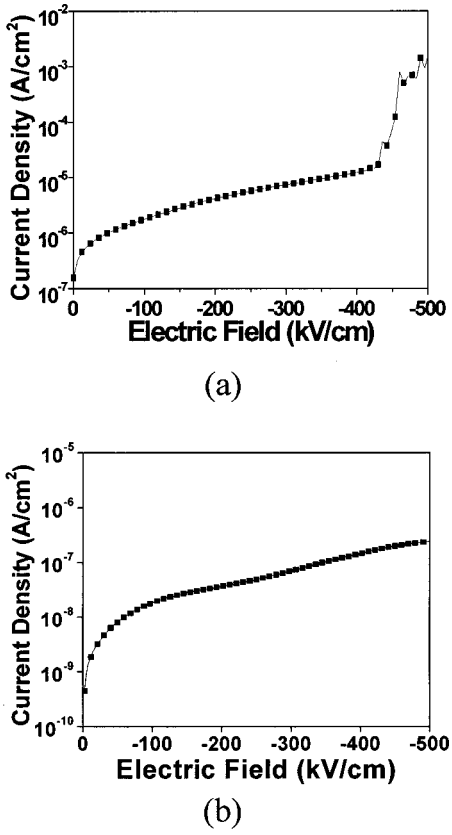

FIG. 5. $J-V$ characteristics of BLT on (a) $Pt/Ti/SiO_2/Si$ and (b) $Al_2O_3(6\ nm)/Si$.

We have also investigated the capacitor leakage current because it is one of the most important properties for a memory capacitor. Figures 5(a) and 5(b) show $J-V$ characteristics of BLT on $Pt/Ti/SiO_2/Si$ and on Al_2O_3/Si, respectively. The leakage current density of BLT on Pt is 1.8×10^{-6} A/cm^2 at -100 kV/cm that is comparable to that of (118)-oriented $Bi_4Ti_3O_{12}$,[15] and the high dielectric breakdown field of -450 kV/cm is also comparable to that of (001)-oriented $Bi_4Ti_3O_{12}$. These results indicate the good quality of BLT on Pt.[15] On the other hand, the leakage current density of BLT on Al_2O_3/Si at -100 kV/cm is 1.8×10^{-8} A/cm^2 that is almost two orders of magnitude lower than BLT on Pt. This low leakage current is comparable with that of vanadium-doped $Bi_4Ti_3O_{12}$[16] and smaller than our previous data of $PZT/Al_2O_3/Si$ FeMOS.[16–17] In addition, no dielectric breakdown up to -500 kV/cm also implies that BLT on Al_2O_3/Si has better dielectric integrity than that on $Pt/Ti/SiO_2/Si$. This smaller leakage current and the larger breakdown field may be due to the additional large energy barrier of Al_2O_3 dielectric[9,10] and no intermediate phase in the interface. The much reduced leakage current of BLT on Al_2O_3/Si is the strong advantage as compared with BLT on Pt because it is directly related to the applied switching energy and technology scaling down.

In conclusion, BLT films on $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si substrates were investigated in this work. Both MFM and FeMOS capacitors show good $C-V$ characteristics and have the same threshold voltage shift of 1.6 V at ±10 V applied voltages. The leakage current density of BLT FeMOS capacitors is about 1.8×10^{-8} A/cm^2 at -100 kV/cm that is two orders of magnitude lower than that of MFM capacitors. The excellent memory characteristics and very low leakage current of BLT on Al_2O_3/Si are the merits for 1T ferroelectric memory as compared with 1T-1C cell.

This work has been supported by the National Science Council Contract Nos. NSC90-2215-E-009-061 and NSC89-2215-E-009-100 of Taiwan.

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