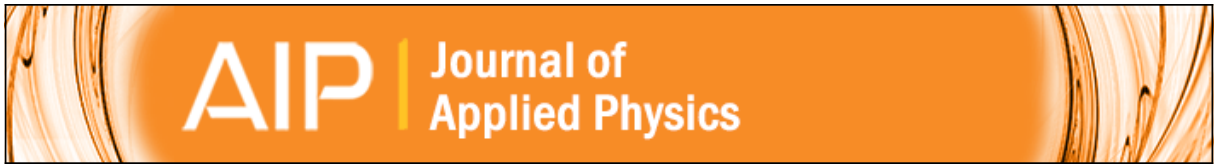

A method to characterize the dielectric and interfacial properties of metal–insulator-semiconductor structures by microwave measurement

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A method to characterize the dielectric and interfacial properties of metal–insulator-semiconductor structures by microwave measurement

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We have developed a method to investigate the dielectric and interfacial properties of gate dielectric thin films by microwave measurement. $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) thin films were deposited on 10 Ω cm (normal) and 10 k Ω cm [high-resistivity, (HR)] silicon substrates at the same time by rf magnetron sputtering. For the BST/HR-silicon, coplanar waveguides (CPW) were fabricated and measured at microwave frequencies with thru-reflect-line calibration while capacitance ($C-V$) measurements were carried out for BST/normal silicon. From the phase change of CPW transmission line and the maximum capacitance in $C-V$ measurement, the dielectric constants of both the BST thin film and interface layer can be determined. Furthermore, the behaviors of insertion loss versus bias voltage were investigated. The results indicate that our method can provide useful information to study the dielectric and interfacial properties of metal–insulator–semiconductor structures. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1459603]

I. INTRODUCTION

With the rapid developments of high-k gate dielectrics[1] and ferroelectric random access memory,[2] the dielectric and interfacial properties of many gate dielectrics deposited on silicon substrate have gained intensive attraction in recent years. Although those metal–insulator–semiconductor (MIS) structures have incorporated many high dielectric constant thin films such as $ZrTiO_4$,[3] Ta_2O_5,[4] TiO_2,[5] $SrTiO_3$,[6] $Ba_xSr_{1-x}TiO_3$ (BST),[7,8] and $SrBi_2Ta_2O_9$,[9] the average dielectric constants of the gate dielectrics obtained by C_{max} (maximum capacitance or accumulation capacitance) in the capacitance–voltage ($C-V$) measurements are often much lower than measured by metal–insulator–metal capacitors due to the low dielectric constant interface layers. In most cases the oxide dielectrics at the interface diffuse into silicon and form a thin SiO_2 layer which lowers down the overall average dielectric constant. Another possible reason is due to the lattice mismatch of dielectrics and silicon surface, which results in lattice strain and subsequently cause the formation of a thin amorphous layer. Although the interface layer is much thinner than the gate dielectric, the overall capacitance is significantly reduced because the total capacitance is the series combination of the multilayers and will be dominated by the low-capacitance layer. In addition, these interface layers often cause increasing interface trap density and then degrade the performance of the gate dielectrics. Therefore, characterization of the interface layers is the important issue in MIS structure. However, these interface layers are often very thin (<10 nm) and their dielectric constants cannot be determined by conventional $C-V$ measurements. Several works[10] used multithickness gate dielectrics to estimate the dielectric constants of the interface layers, assuming both the dielectric constant and thickness of the interface layers were the same for different thickness of the gate dielectrics. However, this assumption is clearly incorrect and only provides a rough estimate. Therefore, additional measurement method for the MIS structure is necessary for exploring its dielectric and interfacial properties.

In our previous work,[11] we have developed a technique to measure the dielectric properties of ferroelectric layer deposited on sapphire by using coplanar waveguide (CPW) with thru-reflect-line (TRL) calibration. In this measurement, the propagation constant (or the velocity) of the multilayered CPW transmission line is perturbed by the high-dielectric-constant layer and the phase of transmission coefficient, $\Delta\Phi_{S_{21}}$, is changed and can be measured to determine the dielectric constant of the ferroelectric layer. This phase change is caused by the high dielectric constant layer, that is, thicker film with larger dielectric constant will give the dominant contribution while the thin interface layer with low dielectric constant gives negligible contribution. Contrary to the $C-V$ measurement, this microwave measurement would therefore provide us direct measurement of the dielectric constant of the gate dielectric, ε_d. After ε_d is measured, the dielectric constant of the interface layer ε_i can be determined based on the average dielectric constant $\varepsilon_{average}$ obtained in the $C-V$ measurement. Therefore, the dielectric constants of both the gate dielectric thin film and interface layer can be solved. This approach is therefore a useful technique for extracting the dielectric constant of gate dielectric and interface layer accurately.

The microwave properties of BST have been studied by some previous works.[12–14] Their studies were focused on the applications on the tunable devices in microwave circuits

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TABLE I. Sample descriptions and the measurement results.

	Sample name	HR (bare substrate)	S1 (BST)	S2 (BST)	S3 (BST)	S4 (BST)	S5 (BST)	S6 (BST)	S7 (BST)
Samples descriptions and the deposition conditions	OMR: $O_2/(O_2+Ar)$	···	0%	10%	20%	10%	10%	10%	10%
	Deposition temperature (°C)	···	600	600	600	600	600	400	500
	t_d (Å)	···	1100	1200	1150	550	2350	1000	1100
	t_i (Å)	···	50	40	50	50	60	110	50
Microwave measurement	q_2	···	7.5×10^{-3}	8.1×10^{-3}	7.8×10^{-3}	3.9×10^{-3}	1.6×10^{-2}	7.2×10^{-3}	7.5×10^{-3}
	q_3	···	7.2×10^{-3}	7.8×10^{-3}	7.5×10^{-3}	3.6×10^{-3}	1.5×10^{-2}	6.5×10^{-3}	7.2×10^{-3}
	$\Delta\Phi(S_{21})$	···	32.3°	31.9°	33.8°	18.7°	55.9°	9.3°	24.1°
	ε_{eff}	6.291	7.691	7.675	7.759	7.078	8.831	6.925	7.324
$C-V$ measurements	$C_{\max}$ (pF)	···	765	567	609	690	537	348	626
	$\varepsilon_{\text{average}}$	···	103	83	86	49	152	45	85
Calculated results	ε_d	···	185	169	187	187	167	85	134
	ε_i	···	10	5	6	5	31	9	9

[a]Sample P: SiO_2 (1000 Å)/polysilicon/HR–Si, deposited by PEVCD in continuous sequence.
[b]Sample X1: SiO_2 (1000 Å)/HR–Si, deposited by thermal growth at 1000 °C.
[c]Sample X2: SiO_2 (1000 Å)/HR–Si, deposited by thermal growth at 1000 °C with SiO_2 in the gap (W) removed.
[d]For the MIS capacitors, the areas are defined to be 9.6×10^{-4} cm^2.

because BST possessed low-loss and high tunability properties. In this article, we are interested in the dielectric and interfacial properties of $(Ba_{0.5}Sr_{0.5})TiO_3$ (BST) thin films deposited on silicon substrate. The dielectric constants of both the BST thin film and thin interface layer were measured by the phase response of the CPW transmission lines. The relationships between insertion losses and bias voltages are also investigated and the results clearly imply the correlation with the trap states. For more illustration, polysilicon with high trap densities and thermally grown SiO_2 were also measured for comparison. These results imply that CPW transmission lines can be used to investigate the dielectric and interfacial properties of MIS structures.

II. SAMPLE PREPARATION

BST thin films were deposited on (100) *n*-type silicon substrates with resistivity of $\rho=10\ \Omega\,\text{cm}$ (normal) and $\rho=10\ \text{k}\ \Omega\,\text{cm}$ [high resistivity (HR)] by rf magnetron sputtering. The deposition conditions of these samples denoted as S1–S7 are listed in Table I. The $Ba_{0.5}S_{0.5}rTiO_3$ target with a diameter of 3 in. was synthesized using standard solid-state reaction process. Since the microwave loss of the conventional silicon substrate (normal) with low resistivity is rather high, we employ high-resistivity silicon substrate to carry out this microwave measurement. For consistency, the normal silicon substrate and the high-resistivity silicon substrates were deposited with BST thin films simultaneously on a spin substrate holder in the vacuum chamber. Before the deposition, standard Radio Corporation of America processes were carried out on silicon substrates to remove the native oxide and surface contamination. The deposition temperatures were ranged from 400 to 600 °C. The constant deposition pressure of 5 mTorr which was maintained by a mixture of oxygen and argon mixing ratio [OMR: $O_2/(O_2+Ar)$] ranged from 0% toward 20%. The x-ray diffraction results as shown in Fig. 1 indicate that all the samples except S6 are well-crystallized films. The thicknesses of BST films were ranged from 500 toward 2000 Å. After deposition, the backside of the normal substrates were deposited with aluminum for ohmic contact after etching off SiO_2 in hydrofluoric solution. Platinum was used as the top electrodes for probe pads. The $C-V$ curves of these MIS capacitors were measured by HP 4284 at 1 MHz.

For the BST/HR-silicon, 1-μm-thick aluminum was deposited on the BST films by thermal evaporator. The photolithography and wet etching were then carried out to form the CPW transmission line patterns as indicated in Fig. 2. The center conductor width (S) was designed to be 20 μm and the gap width (W) 10 μm. Because the characteristic impedance of the CPW transmission line can be changed by the dielectric layer, impedance mismatch may happen. In addition, the transition between the pads and the narrow CPW

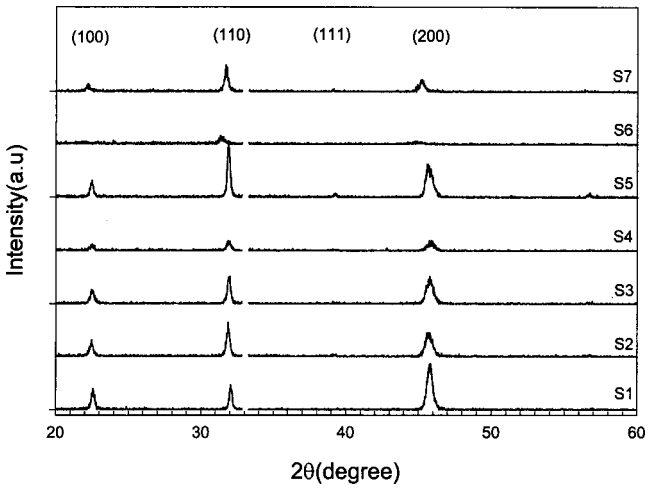

FIG. 1. X-ray diffraction patterns of BST films indicated.

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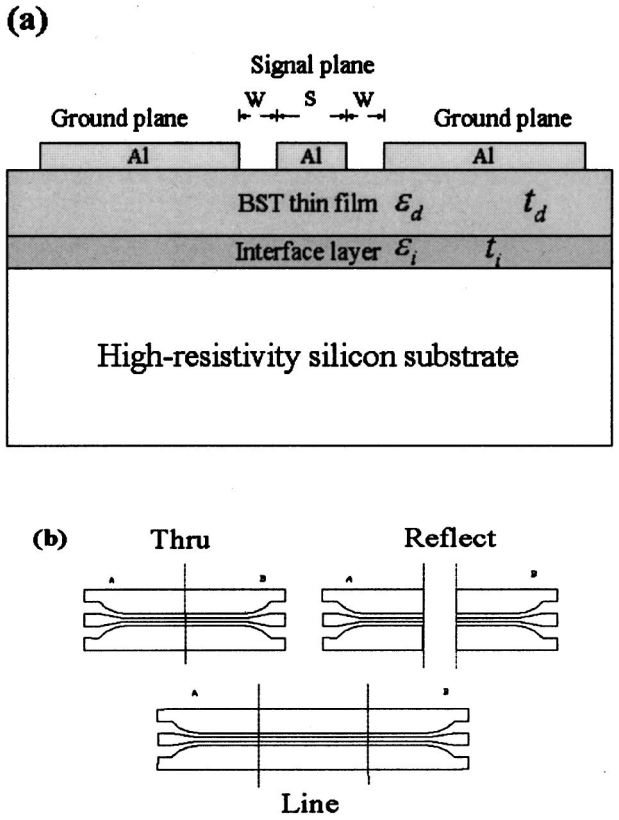

FIG. 2. (a) Cross-section view of CPW transmission lines structures. (b) Layouts of thru, reflect, and line.

transmission lines (tapers) also causes parasitic effect. The TRL calibration was employed to de-embed the microwave response accurately. Details of TRL calibration have been described previously.[11,15] After TRL calibration, the effects of parasitic reflection and impedance mismatch are removed. We designed and measured the ''thru,'' ''reflect,'' and ''line'' CPW patterns at the same wafer, as shown in Fig. 2, and then calculated the TRL calibration by a self-made program. The line pattern was 5 mm longer than the thru, hence, the *S*-parameter de-embedded by the TRL calibration is equivalent to 5 mm long CPW transmission line. These CPW devices were measured at Cascade microwave probe station with HPC GSG probes, and the *S* parameters were measured by the network analyzer HP 8510C with frequency ranging from 200 MHz to 20 GHz. Before measurements, full-two port calibrations were conducted with standard kits to remove external systematic errors.

In order to investigate the behavior of charge carriers in the MIS structures, dc voltage bias was applied at the center conductor through a bias tee. The two ports were applied with the same voltage synchronously to prevent current flow. The measurement frequency was fixed at 20 GHz and the voltage is swept from $+5$ to -5 V. For each CPW device the sweep-frequency measurement at zero bias was first performed, and then the sweep-bias measurement at 20 GHz was then carried out without lifting the probes. The sweep-bias measurement also incorporated TRL calibration for consistency.

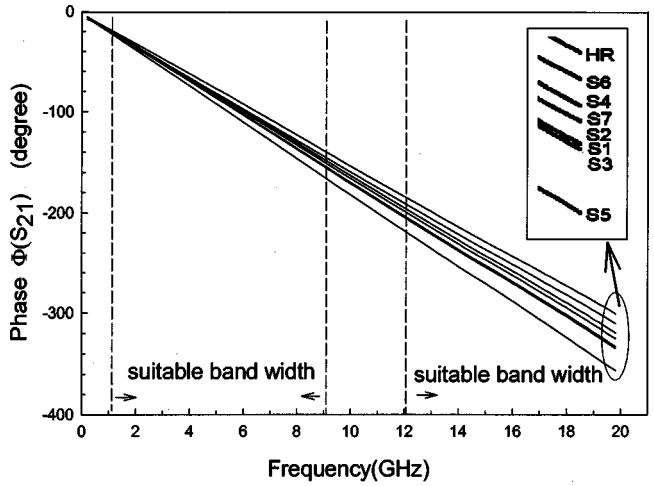

FIG. 3. The phase of S_{21} of BST/HR–Si CPW transmission lines (5 mm long) measured at zero gate bias after TRL calibration.

The film thickness of the gate dielectrics was obtained by the spectrophotometer (n&k analyzer 1200, Nikon). The n&k analyzer incorporates the Forouhi–Bloomer[16] formulation for optical constants along with a parameterized model for multilayer configuration. The thickness of the thin interface layers were observed by transmission electron microscope (TEM) with Philips Tecnai 20 microscope that was operating at an accelerating voltage of 200 keV.

The samples P, X1, and X2 were prepared for comparison. For sample P, 3000-Å-thick poly-silicon was deposited directly on HR-silicon substrate, after that 1000-Å-thick SiO_2 layer was deposited. The processes were done in a continuous sequence by plasma enhanced chemical vapor deposition (PECVD). For samples X1 and X2, 1000-Å-thick SiO_2 was thermally grown at 1000 °C in O_2 ambient. For the sample X2, SiO_2 in the gap (W) was removed by dipping the sample in the buffer oxide etcher (BOE, NH_4F: HF=6:1) with photoresist covered on the aluminum conductors. CPW patterns were also fabricated on these samples to compare with the BST gate dielectrics.

III. MICROWAVE AND *C–V* MEASUREMENTS OF THE DIELECTRIC CONSTANT

The plots of phase of transmission coefficients, S_{21}, measured at zero gate bias versus frequency are shown in Fig. 3. We can observe that the phase of CPW transmission lines is changed after deposition of BST thin film on silicon substrate. These phase changes with respect to the bare HR-silicon substrate, denoted by $\Delta\Phi_{S_{21}}$ are listed in Table I, which are around 10° to 60° at 20 GHz. It is indicated that the phase change is a function of deposition condition and thickness of the BST thin film. For each sample, the effective dielectric constant ε_{eff} is extracted by the phase of transmission coefficient S_{21}:

$$|\Phi_{S_{21}}| = \frac{360\sqrt{\varepsilon_{\text{eff}}} f \ell}{c} \quad \text{(degree)}, \tag{1}$$

where f is the frequency, c is the velocity of light, and ℓ is the length of transmission line, and is equal to 5 mm. The

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TRL calibration is not suitable for frequencies near $n\lambda/2$ (or equivalent 0° and 180° phase shifts). Therefore, the suitable bandwidths without these points are shown in Fig. 3. It is indicated that the phases of all CPW transmission lines are straight lines implying that the dielectric constants of BST films are constant over this frequency range. The effective dielectric constants ε_{eff} are extracted by the slopes of those lines in Fig. 3.

The effective dielectric constant ε_{eff} is a measure of the microwave propagation velocity. We have developed the calculation procedure in our previous work[11] for the two-layer structure, and we can simply extend the formula to three-layer structure with the same conformal mapping method[11,17,18] as the following:

$$\varepsilon_{\text{eff}}=1+q_1(\varepsilon_{\text{Si}}-1)+q_2(\varepsilon_i-\varepsilon_{\text{Si}})+q_3(\varepsilon_d-\varepsilon_i), \tag{2}$$

and

$$k_0=\frac{S}{S+2W}, \tag{3}$$

$$k_1=\frac{\sinh(\pi S/4h)}{\sinh[\pi(S+2W)/4h]}, \tag{4}$$

$$k_2=\frac{\sinh[\pi S/4(t_d+t_i)]}{\sinh[\pi(S+2W)/4(t_d+t_i)]}, \tag{5}$$

$$k_3=\frac{\sinh[\pi S/4t_d)}{\sinh[\pi(S+2W)/4t_d]}, \tag{6}$$

$$q_i=\frac{1}{2}\frac{K(k_i)}{K'(k_i)}\frac{K'(k_0)}{K(k_0)}, \quad i=1,2,3, \tag{7}$$

where h, t_d, and t_i are defined to be the thickness of substrate, gate dielectric, and interface layer, respectively. ε_{Si}, ε_d, and ε_i are the dielectric constants of the Si substrate, gate dielectric, and interface layer, respectively. $K(x)$ is the elliptical integral of the first kind, and $K'(x)\equiv K(\sqrt{1-x^2})$ q_i are the filling factors. The parameters are clearly defined in Fig. 2. Equation (2) can be rewritten as

$$\varepsilon_{\text{eff}}=(1-q_1)+(q_1-q_2)\varepsilon_{\text{Si}}+(q_2-q_3)\varepsilon_i+q_3\varepsilon_d. \tag{8}$$

Equation (8) indicates that the total effective dielectric constant is the sum of the dielectric constant of each layer multiplied by the filling factor. In other words, the filling factor is a measure of the proportionality of electromagnetic energy inside each layer. The filling factor of the substrate, q_1, is almost a constant and approaches 0.5. For our CPW devices with $S=20$ μm, $W=10$ μm, the filling factors. q_2 and q_3 are calculated versus various film thicknesses and plotted in Fig. 4. For comparison, filling factors for different linewidths CPW are also shown. Note that the filling factor is almost proportional to the film thickness and increases with shorter linewidths. The effective dielectric constants were measured for each sample and the corresponding q_2 and q_3 are listed in Table I.

Note that the thin interface layers are less than 100 Å, and the corresponding filling factors, (q_2-q_3), are less than 7×10^{-4}. Furthermore, the dielectric constant of the interface layer is much lower than that of the gate dielectric, therefore the contribution of interface layer is estimated to be less than 1% and can be neglected for convenience. We can simplify the Eq. (2) to

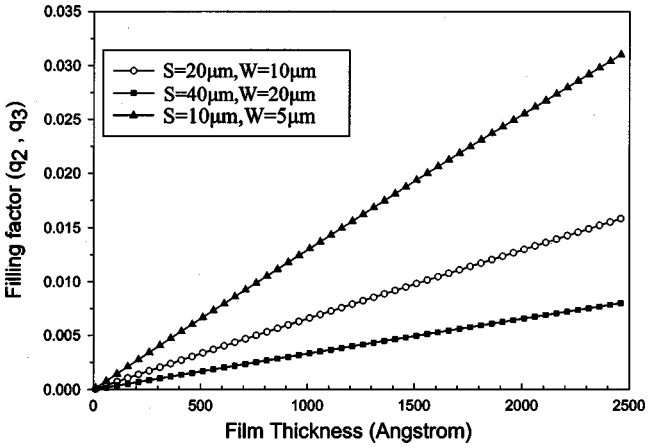

FIG. 4. Calculated filling factors vs BST film thickness for various CPW linewidths indicated.

$$\varepsilon_{\text{eff}}=1+q_1(\varepsilon_{\text{Si}}-1)+q_2(\varepsilon_d-\varepsilon_{\text{Si}}). \tag{9}$$

This equation is consisted of only one unknown value, ε_d, and hence the gate dielectric constant can be extracted directly by the microwave measurements. If Eq. (2) rather than Eq. (9) is used, the two unknown values ε_d and ε_i should be determined if combined with Eq. (10), which will be discussed next.

For a 1000-Å-thick thin film, its filling factor q_3 is around 0.007, therefore high dielectric constant thin film is required to give sensitive phase change of CPW transmission line. That is the reason why we use BST with high dielectric constant ($\varepsilon_d>200$) to demonstrate this technique. However, for thinner gate dielectrics with lower dielectric constants, the phase changes can be too small to be measured. In this case, it can be solved by reducing the linewidths of CPW transmission lines. As indicated in Fig. 4, we can find that the filling factor increases significantly with reducing linewidth. The measurement sensitivity can be enhanced by reducing the linewidth. Another possible way to enhance the phase change is to increase the length of transmission line. However, in these cases the insertion losses increase correspondingly, and the etching process becomes more difficult. Therefore, certain trade-off between the linewidth and phase change should be made to ensure good-sensitivity measurement.

The measurement of insertion loss versus frequency for several samples was carried out and shown in Fig. 5. It shows that the loss of passivated polysilicon is the lowest while that of the thermal oxide is the largest. The reason for this phenomenon will be discussed in Sec. V.

The results of $C-V$ measurements of several samples are shown in Fig. 6. The average dielectric constant is equal to the series combination of the capacitances of BST and interface layer, and can be calculated by

$$\varepsilon_{\text{average}}=\frac{C_{\max}(t_d+t_i)}{A\varepsilon_0}=\left(\frac{t_d}{\varepsilon_d}+\frac{t_i}{\varepsilon_i}\right)^{-1}(t_d+t_i), \tag{10}$$

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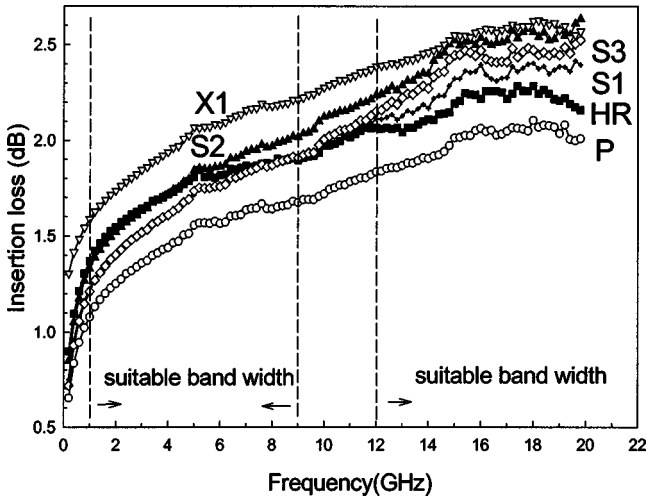

FIG. 5. The insertion loss vs frequency for various samples indicated, which was measured at zero bias after TRL calibration.

where $C_{\max}$ is the maximum capacitance (or the accumulation capacitance). A is the capacitor area, which is equal to 9.6×10^{-4} cm^2 in our measurement. ε_0 is the free space dielectric permittivity. This average dielectric constant is often much lower ($\varepsilon_{\text{average}}<100$) than the dielectric constant ε_d measured by microwave CPW transmission lines. Combining Eqs. (10) and (2), we can calculate ε_d and ε_i, and the results are listed in Table I. For simplicity, Eq. (9) instead of Eq. (2) can be used and the results provide less than 1% deviation, indicating that the contribution of interface layer to the microwave measurements is negligibly small

IV. DISCUSSION OF THE DIELECTRIC PROPERTIES OF BST/SI

As indicated in Table I, the ε_i range from 5 toward 31, which are much lower than ε_d, but larger than 3.9 (dielectric constant of SiO_2). The lattice constant of cubic BST can be calculated by x-ray spectrum shown in Fig. 1 and the results show that the lattice constant of BST is 3.97 Å, which is much lower than that of the silicon, 5.40 Å. This lattice mismatch between BST and silicon wafer may lead to thin interface layer formed to compensate the lattice strain. The interface layer of sample S1 is clearly viewed by TEM pictures shown in Fig. 7, from which the thickness of the interface layer of sample S1 is obtained to be 5 nm. Typical depth profile analyzed by the secondary ion mass spectroscopy of sample S1 (Fig. 8) indicates uniform concentration distribution for all species in the film, but atoms accumulate at the interface of BST/silicon. Although it is common to assume the interface layer of gate dielectric is pure SiO_2, this assumption is incorrect because Ba, Sr, and Ti ions can diffuse into SiO_2 interface layer. Small ions such as Ti^{+4} (0.6 Å) show a large accumulation at the interface, indicating that

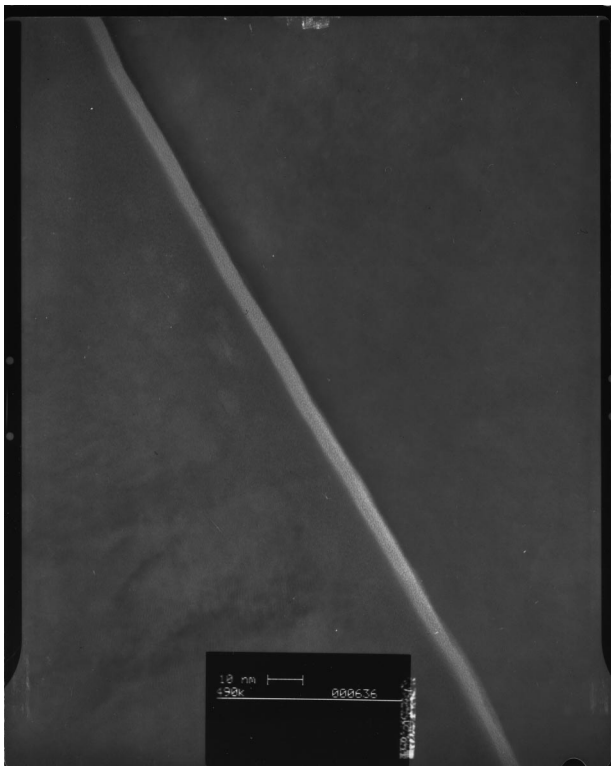

FIG. 7. Transmission electron microscope picture of sample S1. The upper side is silicon, while the lower side is BST thin film.

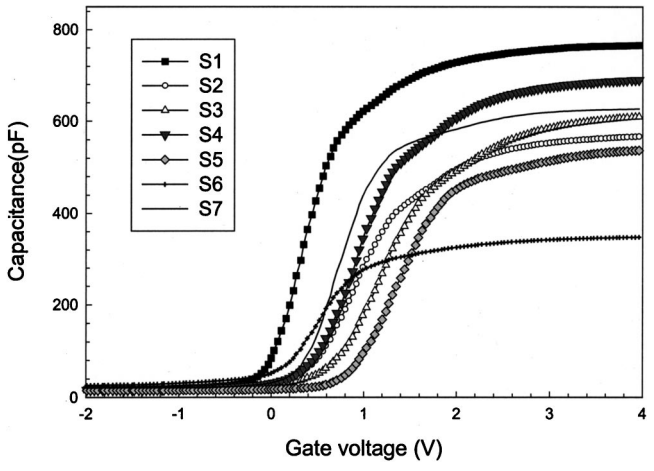

FIG. 6. $C-V$ characteristics of Pt/BST/Si(normal) MIS structures.

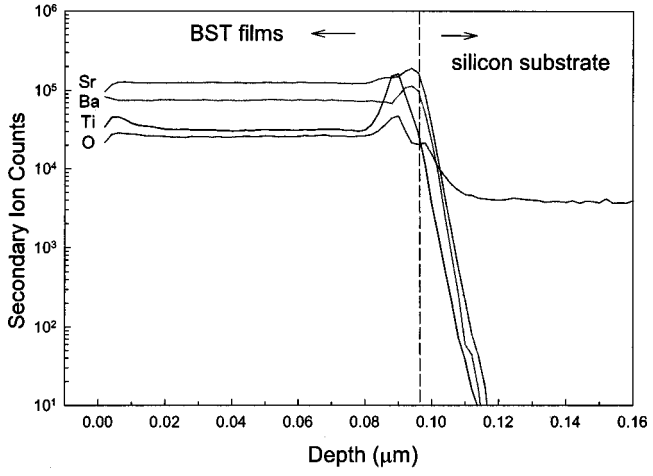

FIG. 8. Secondary ion mass spectroscopy depth profile for S1.

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Ti^{+4} ions easily diffuse into the interfacial SiO_2 layers compared to Ba and Sr. This BST diffused SiO_2 layer has dielectric constant larger than that of SiO_2, 3.9.

One important result of our method is that we can obtain the dielectric constants of both the BST film and interfacial layer. The dielectric constant ε_d of 600 °C deposited BST film is around 200 and decreases for lower deposition temperature (samples S2, S6, and S7). ε_d is only 85 for 400 °C deposition temperature (S6), this is because that the BST layer is amorphous at low temperature growth, as confirmed by the weak peak intensity in the x-ray spectrum (Fig. 1). The average dielectric constants $\varepsilon_{\text{average}}$ decrease with decreasing film thickness (samples S2, S4, and S5), which is common result in the high-*k* gate dielectrics. On the other hand, we can observe the dielectric constant ε_d of BST layer and the interface layer thickness t_i do not change much for different BST film thickness and the average dielectric constants are lowered down much more for thinner BST films. Therefore, it may conclude that the decreasing average dielectric constant with decreasing thickness is mainly due to the interface layer rather than the crystallinity of BST layer in this case. In addition, the interface layer dielectric constant ε_i increases with increasing BST film thickness. This may be attributed to the better crystallized interface layer for thicker BST film.

So far we are the first to measure the dielectric constants of both the gate dielectrics and interface layers directly by employing conventional $C-V$ and microwave measurements together. This measurement technique would provide very useful information for the MIS structure studies.

V. THE MICROWAVE RESPONSE OF MULTILAYERED CPW TRANSMISSION LINES UNDER BIAS

The phase of S_{21} is related to the dielectric constant of the thin film. On the other hand, the magnitude of S_{21} (or insertion loss) is able to give us the information about the charge carrier. We can apply dc bias on the center conductor in the CPW transmission line to attract charge carriers into the interface and monitor the change of insertion loss. For *n*-type substrate, there is electron accumulation at the surface for positive gate bias while there is hole inversion for negative bias. In both cases, we may expect that the charge accumulation in the interface of BST/Si will cause dissipation of electromagnetic energy. The results of the measurements of insertion loss versus bias at 20 GHz for various samples are shown in Figs. 9–12. On the basis of these results, we can find that the insertion loss does not always change rapidly with the bias but instead there are voltage ranges existed with small variations of insertion loss in some samples. In this region the insertion losses vary slowly and beyond this region the insertion losses increase rapidly. We believe that this interesting phenomenon is related to the interface traps. If the charge carrier density Q $(1/\text{cm}^2)$ attracted by the bias is less than the trap density, Q_t, the charge carriers will be bound in the trap states. The trap states are the localized electronic energy states or in other words, the carriers in the trap states are immobile. Therefore, those charge carriers will contribute much less microwave dissipation. In this way, the

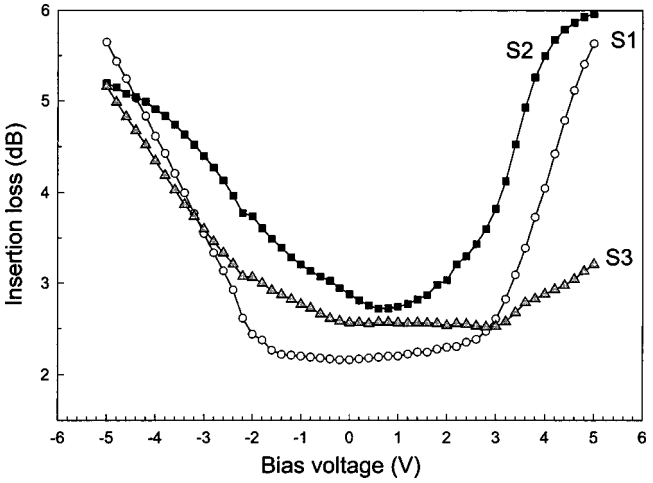

FIG. 9. Comparison of the insertion losses vs bias at 20 GHz for samples deposited at various oxygen mixing ratio.

trap states effectively ''pin'' the Fermi level and the microwave dissipation shows low variation in this voltage range. However, if the applied bias is larger such that $Q>Q_t$, the additional carriers will go to the conduction bands or valence bands and consequently contribute larger microwave dissipations. Since the energy of the trap states is often continuously distributed in the band gap, the trap densities are often characterized by energy density of states, $D_{\text{it}}(1/\text{cm}^2\,\text{eV})$. The D_{it} then causes less band bending than ideal, and the slope of the insertion loss versus bias is reduced.

Based on the earlier argument, we can qualitatively explain the characteristics of the behavior of insertion loss versus bias voltage. As shown in Fig. 9, 10% OMR BST (S2) has the fastest variation implying that lower trap density existed in this sample compared to those of S1 and S3. In Fig. 10, the low temperature grown BST (S6) has smaller variation implying larger trap densities existed in this sample. In Fig. 11, thinner BST gate dielectrics (S4 and S2) have faster variations because their capacitances are larger such that the charge densities attracted per unit voltage are larger. For more illustration, characteristics of passivated polysilicon

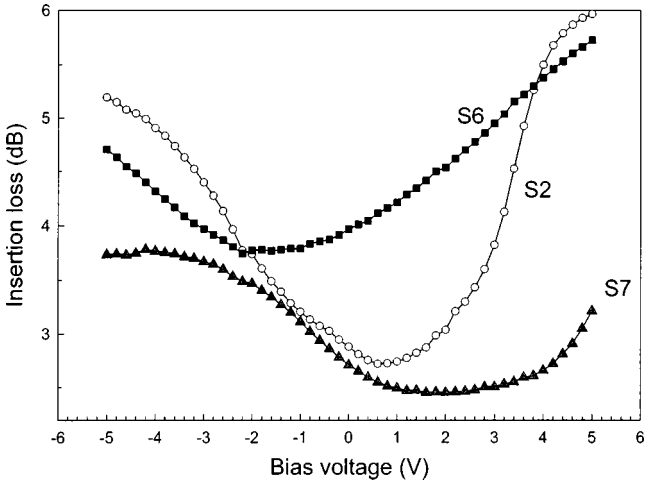

FIG. 10. Comparison of the insertion losses vs bias at 20 GHz for samples deposited at various temperatures.

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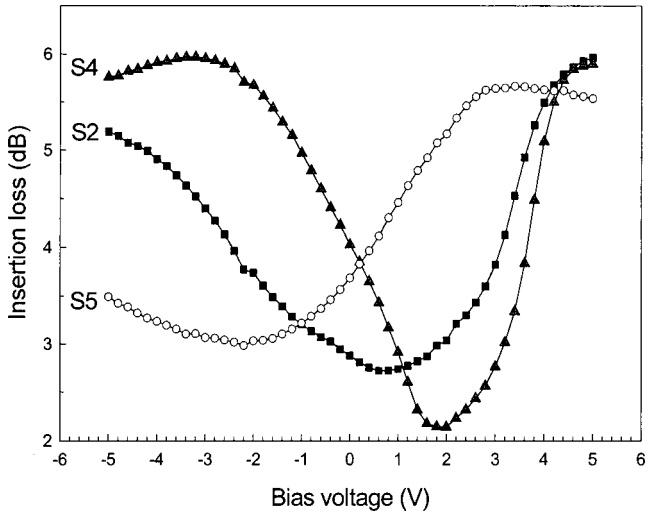

FIG. 11. Comparison of the insertion losses vs bias at 20 GHz for samples with various film thicknesses.

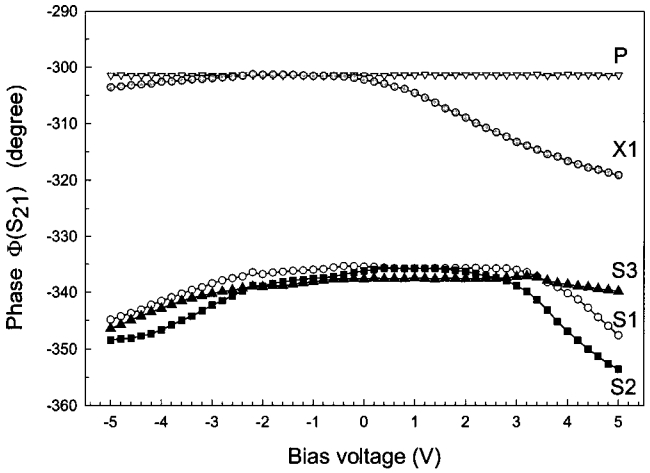

FIG. 13. Comparison of the phase changes vs bias at 20 GHz for several samples indicated.

were also measured (sample P). The 3000-Å-thick polysilicon film was used to provide trap states while the 1000-Å-thick SiO_2 was used for isolation and passivation. Gamble *et al.*[19] have pointed out the incorporation of polysilicon on the surface of HR silicon will reduce the microwave loss through trap states; We are now verifying this assumption by applying bias. In Fig. 12, the insertion loss of sample P remains almost constant for various biases, indicating that all the carriers induced by the applied bias were accommodated in the trap states. This result strongly suggests the correlation of the behavior of insertion loss with trap states. For the 1000-Å-thick thermal-oxide (sample X1) the insertion loss is larger than sample P, and shows a larger variation over bias. The reason for that the incorporation of insulating oxide would cause large microwave loss was explained by Wu *et al.*[20] That is, there is surface band bending existed at the interface of silicon substrate due to the oxide fixed charge. This band bending causes a conducting channel between the signal and ground lines and contributes a large microwave loss. The insertion loss of sample X2 in which the SiO_2 in the gap of CPW was removed is reduced (Fig. 12) because the conducting channel in the gap was removed. The insertion loss of sample X2 also shows a small variation over bias. This is due to the accumulated carriers below the conductors.

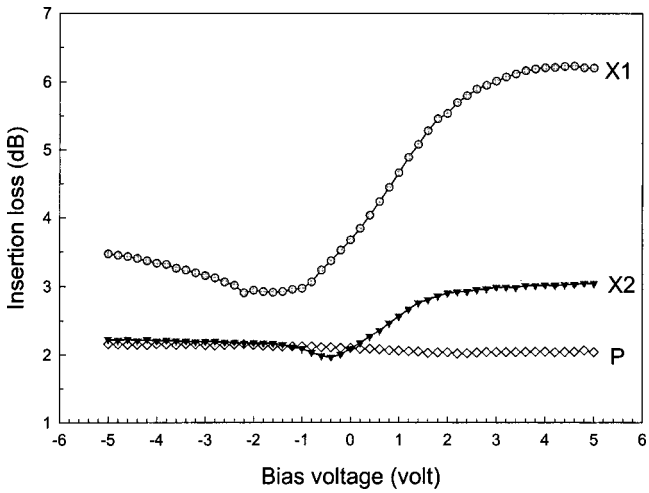

FIG. 12. Comparison of the insertion losses vs bias at 20 GHz for several samples indicated.

Another interesting behavior is the phase changes, as shown in Fig. 13, indicating the phases $\Phi_{S_{21}}$ remain constant for small bias voltages, as the results in the measurement of insertion loss (Fig. 9). Beyond this region, the phase changes increase indicating a slower microwave velocity. This behavior is due to the ''slow wave'' phenomenon.[21–23] The accumulated free carriers not only increase the loss but also effectively slow down the microwave velocity. At low bias voltages, the carriers are trapped in the trap states and are immobile. Therefore, the slow-wave property does not occur. For accurate measurement of the dielectric constant, the phase should be chosen in the range with low variation to prevent the effect of slow wave.

Although we can qualitatively explain the behavior of insertion loss over bias, the accurate modeling of the MIS CPW transmission lines is complex and requires more rigorous analysis of the distribution of charge carriers. It needs further study to quantitatively characterize these phenomena.

By the earlier-mentioned result of this article, the application of passivated polysilicon is a good choice to keep the HR silicon low-loss, even for high bias voltage. We also suggest deep-level traps introduced by ion implantation into the HR-silicon surface will result in the similar behavior due to the pinning of the deep level. All these trap states can be monitored by the relationships of insertion loss versus bias voltage.

High-resistivity silicon is thought to be a possible candidate for rf-complementary metal–oxide–semiconductor (CMOS) substrate. Recent developments of silicon-based rf–CMOS meet difficulty[24] due to the loss of silicon substrate. Conventional CMOS silicon substrate ($\rho \approx \tilde{10}\Omega\text{-}cm$) is high loss, which causes serious parasitic effects both in the active (CMOS, BJT, etc.) and passive devices (inductors, transmission lines, etc.). To overcome such high loss, developments such as microelectromechanical technology[25] and thick

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polymides[26] have been incorporated. However, those technologies are not fully compatible with standard CMOS process and there are also problems in the process yield. These drawbacks are expected to be overcome by employing HR-silicon substrate. If epilayer with doping can be grown on the HR-silicon wafer or by ion implantation, then active devices can be fabricated. For the passive devices such as inductors, one can incorporate HR-silicon substrate with passivated polysilicon or deep level implanted, and the quality factor (Q value) of the devices can be increased. These fabrication processes are all under the standard CMOS process without changing too much. Therefore HR silicon may be used as the rf–CMOS substrate to reduce the substrate parasitic effects and increase the performance of microwave devices.

VI. CONCLUSIONS

In conclusion, we present an attempt to measure both the dielectric and interfacial properties of MIS structures by CPW transmission lines. According to the phase changes and $C-V$ measurements, the dielectric constants of both the gate dielectrics and thin interface layers can be determined accurately with TRL calibration. This method provides a useful technique for material characterization.

The behavior of insertion loss versus bias shows obvious correlations with the trap states. We have demonstrated several phenomena and given qualitative analysis. Although there remain some problems for accurate modeling, we believe this technique provide some information about the MIS structures.

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[1] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[2] E. Tokumitsu, R. I. Nakamura, and H. Ishiwara, IEEE Electron Device Lett. **18**, 160 (1997).
[3] D. A. Chang, P. Lin, and T. Y. Tseng, J. Appl. Phys. **78**, 7103 (1995).
[4] H. F. Luan, S. J. Lee, C. H. Lee, S. C. Song, Y. L. Mao, Y. Senzaki, D. Roberts, and D. L. Kwong, Tech. Dig. - Int. Electron Devices Meet. **1999**, 141 (1999).
[5] X. Guo, X. Wang, Z. Luo, T. P. Ma, and T. Tamagawa, Tech. Dig. - Int. Electron Devices Meet. **1999**, 137 (1999).
[6] K. Eisenberg *et al.*, Appl. Phys. Lett. **76**, 1324 (2000).
[7] A. Srivastava, V. Craciun, J. M. Howard, and R. K. Singh, Appl. Phys. Lett. **75**, 3002 (1999).
[8] S. Jun, Y. S. Kim, J. Lee, and Y. W. Kim, Appl. Phys. Lett. **78**, 2542 (2001).
[9] E. Tokumitsu, G. Fujii, and H. Ishiwara, Jpn. J. Appl. Phys., Part 1 **39**, 2125 (2000).
[10] S. Otani, M. Kimura, and N. Sasaki, Appl. Phys. Lett. **63**, 1889 (1993).
[11] H. T. Lue and T. Y. Tseng, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **48**, 1640 (2001).
[12] J. F. Scott, D. Galt, J. C. Price, J. A. Beall, R. H. Ono, C. A. P. Dearaujo, and L. D. Mcmillan, Integr. Ferroelectr. **6**, 189 (1995).
[13] J. F. Scott, *Ferroelectric Memories* (Springer, Berlin, 2000), Chap. 13.
[14] F. A. Miranda, F. W. Van Keuls, R. R. Romanofsky, C. H. Mueller, and J. D. Warner, Integr. Ferroelectr. **34**, 247 (2001).
[15] G. F. Engen and C. A. Hoer, IEEE Trans. Microwave Theory Tech. **27**, 897 (1979).
[16] A. R. Forouhi and I. Bloomer, Phys. Rev. B **38**, 1865 (1988).
[17] E. Carlsson and S. Gevorgian, IEEE Trans. Microwave Theory Tech. **47**, 1544 (1999).
[18] C. M. Jackson, T. Pham, Z. Zhang, A. Lee, and C. Pettiete-Hall, IEEE MTT-S Int. Microwave Symp. Dig. **3**, 1439 (1995).
[19] H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, and J. A. C. Stewart, IEEE Microwave Guid. Wave Lett. **9**, 395 (1999).
[20] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, IEEE Microwave Guid. Wave Lett. **9**, 10 (1999).
[21] J. P. K. Glib and C. A. Balanis, IEEE Trans. Microwave Theory Tech. **40**, 2148 (1992).
[22] E. S. Tong and S. K. Chaudhuri, IEEE Trans. Microwave Theory Tech. **47**, 1760 (1999).
[23] S. Chen, R. Vahldieck, and J. Huang, IEEE Trans. Microwave Theory Tech. **44**, 2487 (1996).
[24] T. H. Lee and S. S. Wong, Proc. IEEE **88**, 1560 (2000).
[25] V. Milanovic, M. Gaitan, E. D. Bowen, and M. E. Zaghloul, IEEE Microwave Guid. Wave Lett. **6**, 380 (1996).
[26] G. E. Ponchak, A. Margomenos, and L. P. B. Katehi, IEEE Trans. Microwave Theory Tech. **49**, 866 (2001).

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