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Impacts of SiN deposition parameters on n-channel metal-oxide-semiconductor field-effect-transistors

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ABSTRACT

Although the incorporation of a SiN capping layer could dramatically enhance device performance, the accompanying hydrogen species contained in the capping layer may aggravate hot-carrier reliability. In order to alleviate this shortcoming, we vary the precursor flow conditions and deposition temperature of SiN film during plasma-enhanced chemical vapor deposition (PECVD) and study their impacts on the device performance and reliability. We found that SiN film with higher nitrogen content depicts larger tensile stress and therefore better mobility. More importantly, the resistance to hot-carrier degradation is also improved by increasing N_2 gas flow rate and deposition temperature because of less hydrogen diffusion from the capping layer.

1. Introduction

Channel strain engineering such as embedded SiC source/drain (S/D) [1,2] and highly tensile SiN capping layer [1–9] for *n*-channel metal-oxide-semiconductor field-effect-transistors (NMOSFETs) mobility enhancement has been pursued aggressively in scaled complementary metal-oxide-semiconductor (CMOS) devices. Among these methods, SiN capping technique has received much attention because it is easily implemented in modern ULSI technology. In addition, depending on the SiN deposition conditions, stress level ranging from highly tensile to highly compressive is adjustable, enabling the dual-SiN stressor technology for CMOS manufacturing [5].

Although SiN capping can dramatically enhance the device performance, the abundant hydrogen species generated during the SiN deposition process may diffuse into the channel region, resulting in serious hot-carrier reliability issue [6]. Recently, the insertion of an ultra-thin buffer layer between the SiN capping layer and the underlying poly-Si gate electrode was demonstrated to effectively suppress the hydrogen diffusion and restore the reliability without compromising the device performance [7,8]. In this work, another effective approach to directly adjust the composition of SiN film by varying the precursor gas flow rate and deposition temperature is explored. Our results indicate that it is indeed possible to optimize the SiN deposition so the device reliability aggravation is alleviated without compromising the device performance enhancement by the channel strain.

2. Device fabrication

NMOSFETs characterized in this study were with 3 nm-thick thermal oxide grown in a vertical furnace, and 150 nm-thick polycrystalline–silicon (poly–Si) layer as the gate electrode. After S/D doping and self-aligned spacer formation step, a 300 nm-thick SiN capping layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), as shown in Fig. 1. In this work, we evaluated devices with five different types of SiN film using SiH_4/NH_3/N_2 gas mixtures at 300 °C and 400 °C (denoted as SiN-1, SiN-2, SiN-3, SiN-1(400 °C), and SiN-3(400 °C)). The detailed gas flow rates are listed in Table 1, and the major parameter adjusted is the N_2 gas flow rate. Deposition pressure and radio frequency (rf) power were fixed at 1 Torr and 100 W, respectively. In addition to SiN-capped samples, the control devices with 300 nm-thick PECVD oxide capping were also fabricated as the control (denoted as SiO_2 split). After contact hole formation and metallization processes, the processing steps were completed with a forming gas anneal at 400 °C and 30 min.

Current–voltage characteristics of devices with channel width (W) of 10 μm and channel length (L) ranging from 0.4 μm to 10 μm were measured using an Agilent 4156 system. Capaci-

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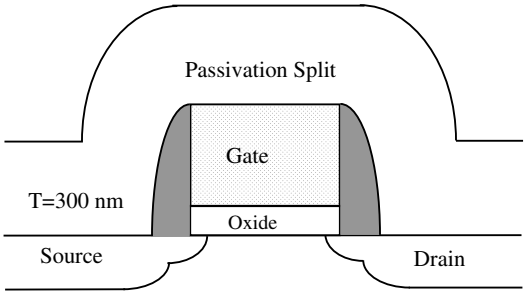

Fig. 1. Schematic structure of fabricated devices with different types of passivation. The passivation thickness is fixed at 300 nm.

tance–Voltage (C–V) characteristics for devices with $W/L = 50/50$ μm were performed using Agilent 4284 system.

3. Material analysis

X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared spectrometer (FTIR) were employed to investigate the material properties of the deposited SiN films, and the major results are given in Figs. 2 and 3, respectively. From XPS analysis (Fig. 2), we confirmed that SiN-3 and SiN-3(400 °C) samples have similar N content that is higher than the other samples. Obviously the use of higher N_2 flow rate in the deposition process is responsible for the phenomenon. In addition, from the analysis of FTIR measurement, an increase in N_2 flow rate [10] and deposition temperature [11] tends to weaken the signal of Si–H bonds, as shown in Fig. 3. Later we will show that this finding has important implication for increasing the immunity of devices to hot-carrier degradation.

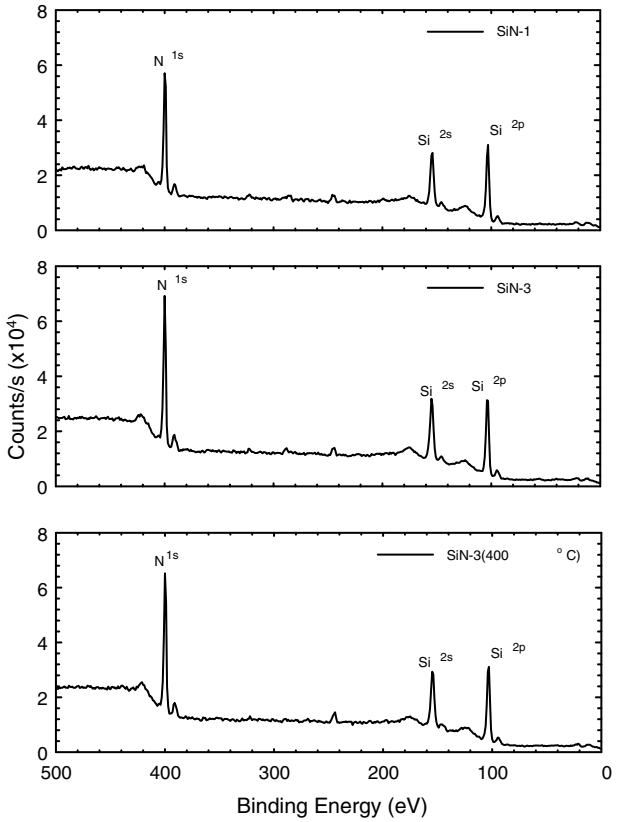

Fig. 2. Results of XPS analysis: SiN-3 and SiN-3(400 °C) samples depict similar N content which is higher than the other samples, owing to the use of higher N_2 flow rate during the deposition.

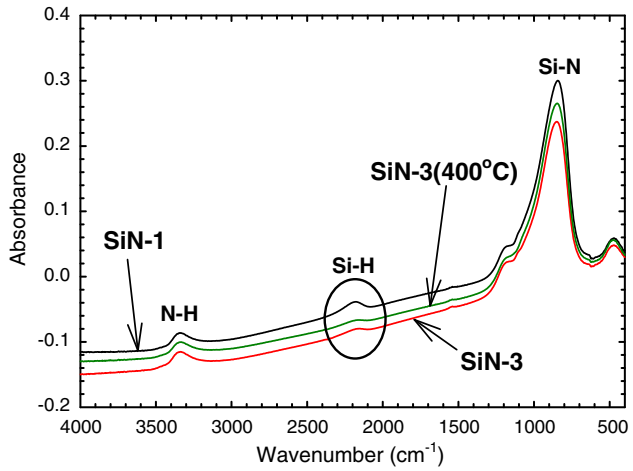

Fig. 3. Results of FTIR analysis: SiN-1 sample contains more Si–H bonds than the other samples. Increase in N_2 flow rate and deposition temperature tends to weaken the signal of Si–H bonds.

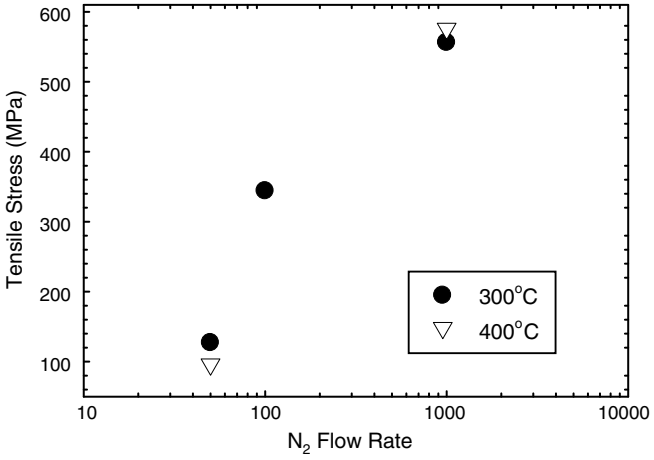

Fig. 4. Stress level of the deposited films as a function of the N_2 flow rate during deposition.

The stress measurements were performed using a Tencor FLX-2320 system. This system evaluates the stress by measuring the change in curvature of the silicon substrate before and after the deposition of a blanket SiN layer with a thickness of 300 nm. We confirmed that the stress is tensile in nature with a magnitude of around 127, 344, 556, 96, and 576 MPa for SiN-1, SiN-2, SiN-3, SiN-1(400 °C), and SiN-3(400 °C) splits, respectively, as listed in Table 1. It can be seen that the tensile stress increases with increasing N_2 flow rate, as shown in Fig. 4, while only mildly affected by the two deposition temperatures studied in this work.

4. Device characteristics

Next, the electrical characteristics were performed using an Agilent 4156 system. Fig. 5 compares transconductance (Gm) enhancement for all splits with $W/L = 10/0.4$ μm. It can be seen that SiN-3 and SiN-3(400 °C) splits depict identical Gm that is the largest among all samples, while the SiN-1 and SiN-1(400 °C) splits show comparable Gm to the SiO_2 split. Similar enhancement trend in drive current is also observed, as shown in Fig. 6. These

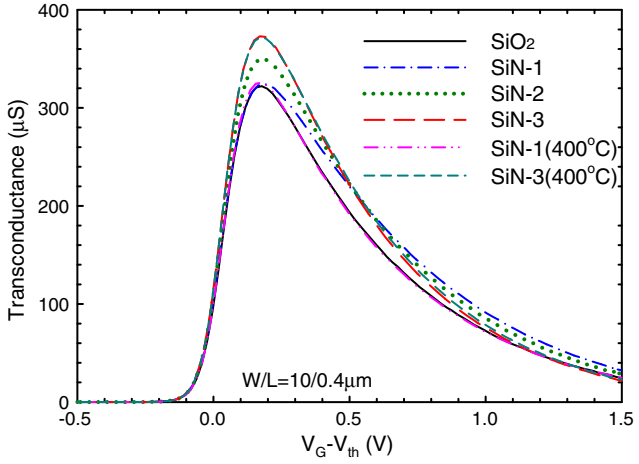

Fig. 5. Transconductance (Gm) versus (V_G–V_{th}) for all splits with W/L = 10/0.4 μm. The SiN-3 and SiN-3(400 °C) splits depict identical Gm which is the largest among all samples, owing to the largest tensile stress level.

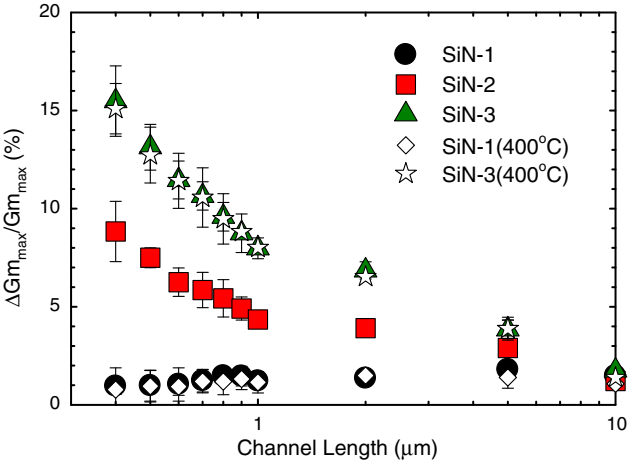

Fig. 7. The percentage increase of Gm for all SiN-capping samples, compared with the SiO_2 controls, as a function of channel length. Each datum point represents the mean measurement value from six devices.

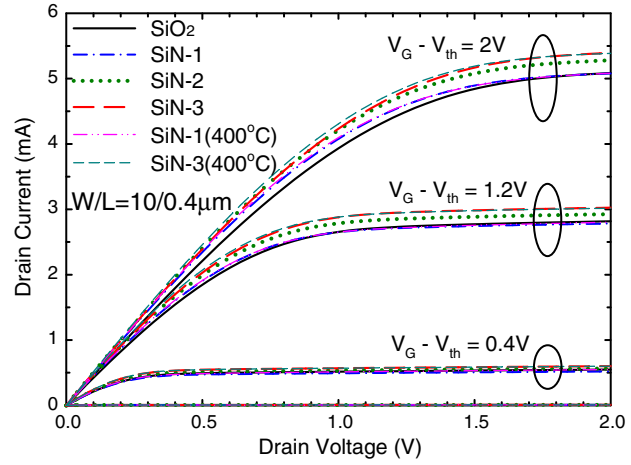

Fig. 6. Output characteristics of NMOSFETs for all splits. The enhancement trend in driving current is similar to Gm increase.

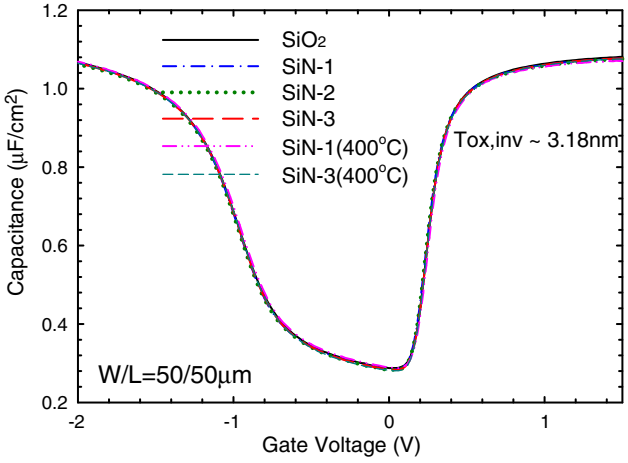

Fig. 8. Capacitance–Voltage (C–V) characteristics for all splits. The C–V curves coincide altogether, indicating that the above-mentioned results are indeed not caused by the difference in oxide thickness.

electrical results are consistent with the results of film stress measurement listed in Table 1.

Fig. 7 shows the percentage increase of Gm for all SiN-capping samples compared with the controls as a function of channel length. Each datum point represents the mean measurement value from six devices. We can see that Gm enhancement ratio increases with decreasing channel length, a feature of uniaxial strain caused by SiN capping [9]. The C–V characteristics of these samples are shown in Fig. 8. It can be observed that the C–V curves coincide altogether, indicating that the above-mentioned results are indeed not caused by the difference in gate-oxide thickness.

Table 1
Precursor flow rates, deposition temperature, and measured tensile stress level for SiN films

	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Temp. (°C)	Stress (MPa)
SiN-1	50	6	50	300	127
SiN-2	50	6	100	300	344
SiN-3	50	6	1000	300	556
SiN-1(400 °C)	50	6	50	400	96
SiN-3(400 °C)	50	6	1000	400	576

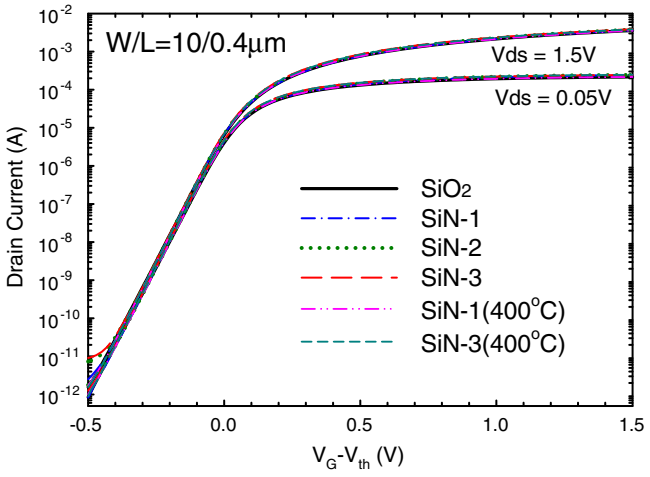

Fig. 9. Subthreshold characteristics of NMOSFETs for all splits with W/L = 10/0.4 μm.

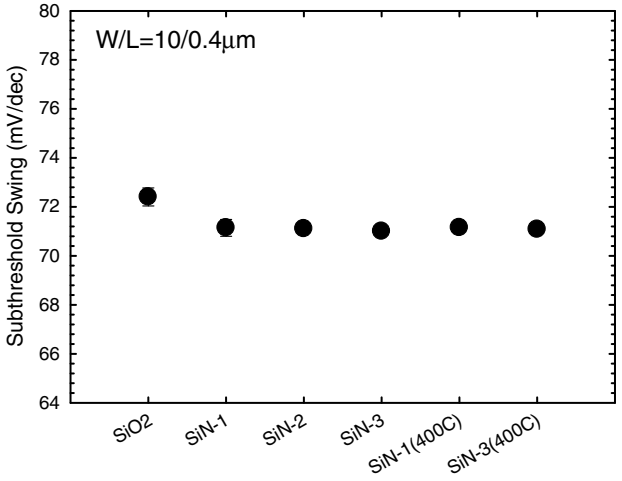

Fig. 10. Subthreshold swing of NMOSFETs for all splits with W/L = 10/0.4 μm.

The subthreshold characteristics and extracted subthreshold swing (S.S.) are shown in Figs. 9 and 10, respectively. We can see that subthreshold swing of all SiN-capping splits depicts similar value and is slightly lower than that of SiO_2 control. Subthreshold swing of an MOSFET at room temperature can be expressed as [12]

$$S.S. = 60\left[1 + \frac{C_d + C_{it}}{C_{ox}}\right](\mathrm{mV/dec}),$$

where C_{ox} is the gate capacitance, C_d is the depletion capacitance, and C_{it} is interface state capacitance. The PECVD SiN film contains a large amount of hydrogen due to the use of hydrogen-containing precursors (SiH_4 and NH_3) [10,13]. These hydrogen species may diffuse into the SiO_2/Si interface and passivate the dangling bonds, resulting in a decrease in C_{it} [10,14] and a reduction in S.S.

5. Hot-carrier stress

Finally, we turn our attention on hot-carrier characteristics. Devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.6 V and V_G at maximum substrate current. Threshold voltage shift (ΔV_{th}) and interface state generation (ΔN_{it}) as a function of stress time for all splits are shown in Fig. 11a and b, respectively. It can be seen that SiN-1 split depicts the worst degradation in terms of the largest ΔV_{th} and ΔN_{it}, while SiN-1(400 °C) split apparently fares much better. By contrast, SiN-3 and SiN-3(400 °C) splits show much improvement in the immunity to hot-carrier damage as compared with the other SiN samples. Note that the difference between SiN-3 and SiN-3(400 °C) is much smaller than that between SiN-1 and SiN-2. Since the SiN-3 split has the least hydrogen content, this implies that the effect of deposition temperature becomes weaker as the SiN contains less hydrogen.

From the FTIR results shown in Fig. 3, we speculate that the amount of Si–H bonds contained in the SiN film is mainly responsible for the hot-carrier immunity of the SiN samples. Note that the bond strength of nominal Si–H bonds (i.e., 314 kJ/mole) is much weaker than that of N–H bonds (i.e., 389 kJ/mol) [15,16]. It is thus reasonable to assume that the hydrogen pertaining to the former bonds is much easier to dissociate and release from the SiN film. As a consequence, the high amount of Si–H bonds in the SiN-1 split (Fig. 3) would release extra H species to the device and form new Si–H bonds at the Si/channel interface [10,14]. The breaking of Si–H bonds at the Si/channel interface during stressing is believed to be one of the major root causes responsible for the hot-carrier degradation [6–8,17]. These passivated Si–H bonds act as precursors to hot-carrier degradation [18,19] and are more easily broken during subsequent stressing [17]. Therefore, SiN film containing abundant hydrogen species would aggravate hot-carrier reliability. Since SiN-1 film contains the highest amount of Si–H bonds, the worsening of hot-carrier reliability occurs most significantly in the SiN-1 split, even though its strain level is not high. Increase in both N_2 flow rate [10] and deposition temperature [11] could reduce the amount of Si–H bonds, as evidenced in FTIR analysis. Therefore, SiN-3(400 °C) shows the best hot-carrier reliability among all SiN capping samples, even though its stress level and the resultant device performance enhancement is the highest (Figs. 5–7). However, the difference between SiN-3(400 °C) and SiN-3 is small. This indicates that, as the amount of Si–H bonds contained in the SiN layer is reduced, the deposition temperature plays a less important role on affecting the device performance as well as the hot-carrier degradation.

Channel strain engineering using highly tensile SiN capping has been popularly applied to modern technology to enhance the driving current of NMOS [1–9]. Based on the results presented in the present study, the N content and the Si–H bonds contained in the capping layer must be carefully controlled. Special attention should be paid to the NMOS devices in the input/output (I/O) regions which have more concerns on hot-carrier reliability, since

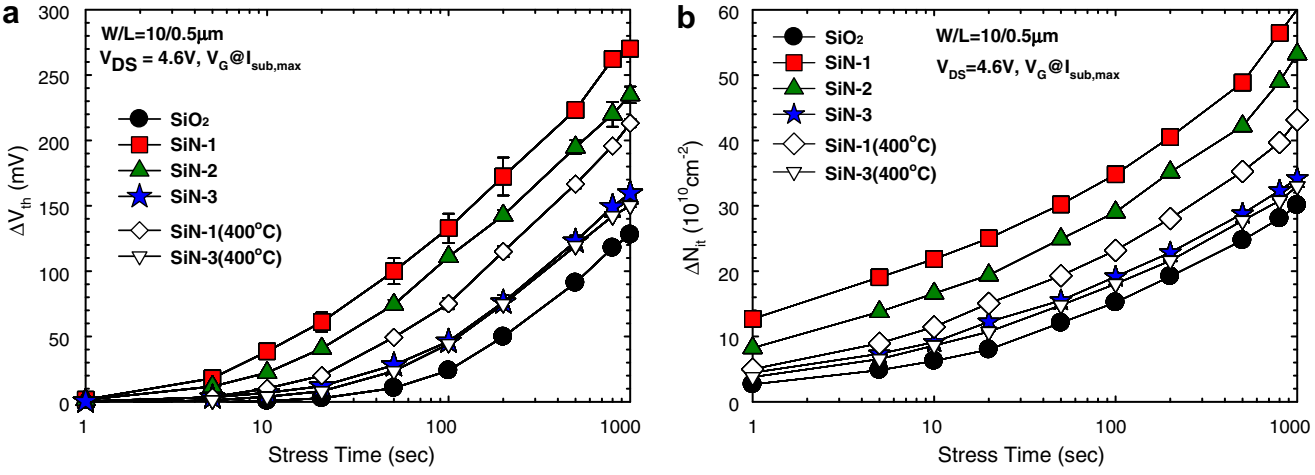

Fig. 11. (a) Threshold voltage shift (ΔV_{th}), and (b) interface state generation (ΔN_{it}) as a function of stress time for all splits. Devices are stressed at V_{DS} = 4.6 V, and V_G at maximum substrate current. ΔV_{th} is defined as $V_{th}(t)$–$V_{th}(0)$ for transistors with W/L = 10/0.5 μm.

they typically are subjecting to a working voltage higher than the core devices.

6. Conclusions

In this work, we have fabricated strained channel NMOSFETs with five types of SiN capping layer by varying the N_2 flow rate and temperature during deposition. Both the tensile stress level and the device performance enhancement are found to increase with increasing N_2 flow rate, especially in short-channel devices. On the other hand, we found that the device immunity to hot-carrier degradation is mainly affected by the hydrogen content, rather than the stress level. Therefore, SiN film with high tensile stress but low hydrogen content is ideally suitable for NMOSFETs, and nitrogen-rich film can fulfill the requirement.

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