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Microelectronics Reliability 42 (2002) 721–733

MICROELECTRONICS RELIABILITY

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RF CMOS technology for MMIC

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Received 6 December 2001

Abstract

This paper presents a high performance RF CMOS technology with a complete portfolio of RF and base band components for single-chip systems. Using an optimized 0.13 μm CMOS topology, f_T of 86 GHz and f_{max} of 73 GHz are obtained, in addition to a NF_{min} of 1.5 dB without ground-shielded signal pad. The high-Q accumulation-mode and diode varactors are optimized to perform a high tuning range of 47% and 25%, respectively. Inductors with a quality factor of 18 at 1.7 nH are obtained using copper interconnect, while capacitors with high unit capacitance and quality factor are fabricated with metal-insulator-metal structures. Finally, a deep n-well isolation is adopted to suppress the interblock coupling noise penetrating through substrate by 40 and 25 dB at 0.1 and 2.4 GHz, respectively. These results clearly demonstrate that CMOS technology can provide a complete solution for single-chip wireless systems.

1. Introduction

Successful implementation of the entire circuit blocks in a single-chip requires the integration of precise and high performance passive as well as active components [1]. In recent years CMOS technologies have become quite attractive for RF circuit implementation due to aggressive scaling, high-speed performance, and cost reduction. In the development of short-range wireless communications, CMOS has received tremendous interest by integration with high performance digital circuits and high-speed analog circuits [2]. Nonetheless, several major issues need to be addressed for adopting CMOS to RF products. First of all, the RF performance of MOS transistor itself represents a bottleneck due to limited cut-off frequency (f_T), maximum oscillation frequency (f_{max}), and high-frequency noise performance (NF_{min}) [3]. Secondly, the fabrication of RF passive components with high quality factor (Q) is in direct conflict with the fine-pitch and thin-line metallization used in advanced CMOS technologies. Thirdly, the coupling noise propagation through the substrate, due to noise generated during CMOS digital switching, complicates the integration of digital, analog and RF blocks on the same chip [4,5]. Isolation among each individual RF blocks become crucial in implementing high precision and high quality RF circuits.

In this paper, optimization of device design using an existing logic CMOS baseline for RF circuit applications is discussed [3,6–11]. This approach is quite promising because of its compatibility with existing logic CMOS technology and inherent reliability. Various high-Q varactors are investigated. The resultant integrated varactors can be successfully implemented as the capacitive tuning elements for monolithic microwave ICs (MMIC). The on-chip inductors, which often are a performance limiting component in many important RF circuits, such as voltage-controlled oscillators (VCO) phase noise [12], low-noise amplifiers (LNA) bandwidth [13], and passive filters loss, are also presented. Additionally, the metal-insulator-metal (MiM) capacitors with their highly linearity, are discussed by observing their RF characteristics. Finally, the use of a deep n-well isolation for integrating RF blocks with low coupling noise is also discussed.

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0026-2714/02/$ - see front matter
PII: S0026-2714(02)00006-9

This paper is organized as follows. After a brief introduction in Section 1, RF performance of MOSFET is described in Section 2. Section 3 describes the varactors, while Section 4 discusses the on-chip inductors. The MiM capacitors are discussed in Section 5, and the substrate coupling is discussed in Section 6. Finally, a brief conclusion is given in Section 7.

2. RF performance of MOSFET

2.1. Small-signal model analysis of MOSFET

To investigate the RF figure of merit (FOM) for MOSFET, we first concentrate on the small-signal model of MOSFET. The cross-section of a MOSFET is shown in Fig. 1. The intrinsic parts of the MOSFET, enclosed in the box with broken lines in Fig. 1, are responsible for the transistor action, and consist of the gate, gate oxide, inversion layer and the depletion region between source and drain. The extrinsic parts of MOSFET, which are located outside the box, consist of all the parasitics. The complete small-signal equivalent circuit for RF application is as shown in Fig. 2(a). The gate transconductance g_m, source-drain conductance g_{ds} and body transconductance g_{mb} describe the channel transport current [14] with the following relation:

$$i_T = g_m v_{gsi} + g_{ds} v_{dsi} + g_{mb} v_{bsi}, \tag{1}$$

where v_{gsi}, v_{dsi} and v_{bsi} represent the voltage changes of the intrinsic parts. In addition to the transport current, charge storage effects are governed by the intrinsic capacitance C_{gsi}, C_{gdi}, C_{sbi}, C_{dbi} and C_{gbi}.

The gate resistance R_g is composed of the resistance of polygate and contact, while the source/drain resistance R_s/R_d includes the spreading resistance, diffusion resistance, and contact resistance of source/drain. The p-well resistance is modeled by R_{sb}, R_{db} and R_{dsb} which is the proximity resistance between source and drain [15,16]. Finally, capacitance C_{gse} and C_{gde} comprise the overlap capacitance and the outer fringing capacitance between gate and source/drain, which is in parallel with C_{gsi} and C_{gdi}. Hence, the whole gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} can be represented as

$$\begin{aligned} C_{gs} &= C_{gsi} + C_{gse}, \\ C_{gd} &= C_{gdi} + C_{gde}. \end{aligned} \tag{2}$$

In addition, source and drain junction capacitance C_{jsb} and C_{jdb} are in parallel with C_{sbi} and C_{dbi}, respectively. Hence, the whole source-to-body capacitance C_{sb} and drain-to-body capacitance C_{db} can be represented as

$$\begin{aligned} C_{sb} &= C_{sbi} + C_{jsb}, \\ C_{db} &= C_{dbi} + C_{jdb}. \end{aligned} \tag{3}$$

Lastly, the extrinsic gate-to-body capacitance C_{gbe} and intrinsic capacitance C_{gbi} can be incorporated into the whole gate-to-body capacitance C_{gb}, as shown below:

$$C_{gb} = C_{gbi} + C_{gbe}. \tag{4}$$

Hence, the small-signal equivalent circuit can be further constructed as shown in Fig. 2(b) by taking into account (2)–(4). For two-port common-source S-parameter measurements, the source and body are tied to the ground, while the gate and drain are connected to the input and output ports respectively. So to obtain Y-parameters that reflect the configuration of measurement, source and body nodes in Fig. 2(b) should be grounded. The Y-parameters can be derived according to Fig. 2(b), and is shown below [15,16]:

$$\begin{aligned} y_{11} &\cong \frac{j\omega C_{gg}}{1 + j\omega R_g C_{gg}} \cong \omega^2 \left(R_g C_{gg}^2 \right) + j\omega C_{gg}, \\ y_{12} &\cong \frac{-j\omega C_{gd}}{1 + j\omega R_g C_{gg}} \cong -\omega^2 R_g C_{gg} C_{gd} - j\omega C_{gd}, \\ y_{21} &\cong \frac{g_m - j\omega \left(C_m + C_{gd} \right)}{1 + j\omega R_g C_{gg}} \\ &\cong g_m - \omega^2 R_g C_{gg} \left(C_m + C_{gd} \right) \\ &\quad - j\omega \left(C_m + C_{gd} + g_m R_g C_{gg} \right), \\ y_{22} &\cong \frac{g_{ds} + j\omega \left(C_{bd} + C_{gd} \right)}{1 + j\omega R_g C_{gg}} \\ &\cong g_{ds} + \omega^2 R_g C_{gg} \left(C_{bd} + C_{gd} \right) \\ &\quad + j\omega \left(C_{bd} + C_{gd} - g_{ds} R_g C_{gg} \right), \end{aligned} \tag{5}$$

where $C_{gg} = C_{gs} + C_{gd} + C_{gb}$, and C_m is the transcapacitance that equals to the difference between intrinsic drain-to-gate capacitance and gate-to-drain capacitance (i.e., $C_{dgi} - C_{gdi}$). The derivation of (5) neglects the source/drain resistance and the p-well resistance, and assumes $R_g C_{gg} \ll 1$. The Y-parameters are very useful for analyzing RF FOM of MOSFET.

2.2. Layout of MOSFET cell

The schematic top-view of MOSFET with finger-type gate and p-well contacts, which will be called "MOSFET cell" in this paper, is shown in Fig. 3(a). All fingers have the same gate length L_g. The total gate width W_t thus equals to the unit finger length (W_f) multiplied by the total finger number (m). A wide gate width is often used to improve the transconductance of the MOSFET cell, however, gate resistance increases because of the wide gate width. To alleviate this undesirable effect, multi-finger gate structure is generally employed to effectively reduce the gate resistance. For MOSFET cell with multi-finger gate structure, the gate resistance is reduced by the square of the finger number. Further, since gate contacts are designed on both sides of each finger, the gate resistance is reduced by a factor of 12 due to the distri-

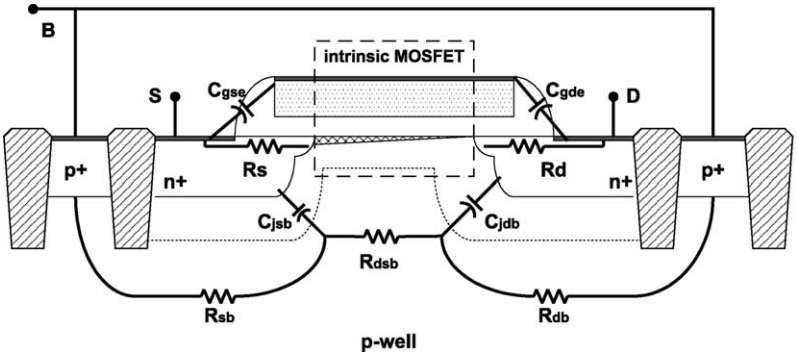


Fig. 1. The cross-section of MOSFET including the parasitics for small-signal equivalent circuit.

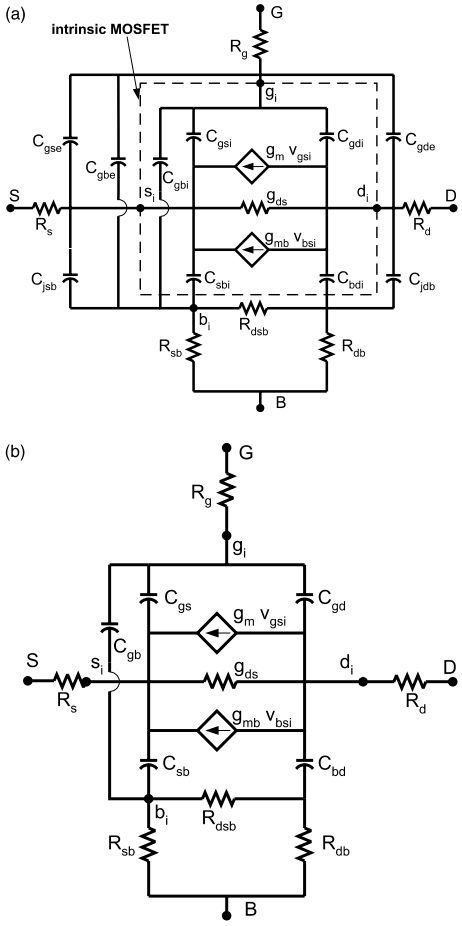


Fig. 2. Quasi-static small-signal model of MOSFET for RF applications: (a) incorporating all parasitics, and (b) a simplified version.

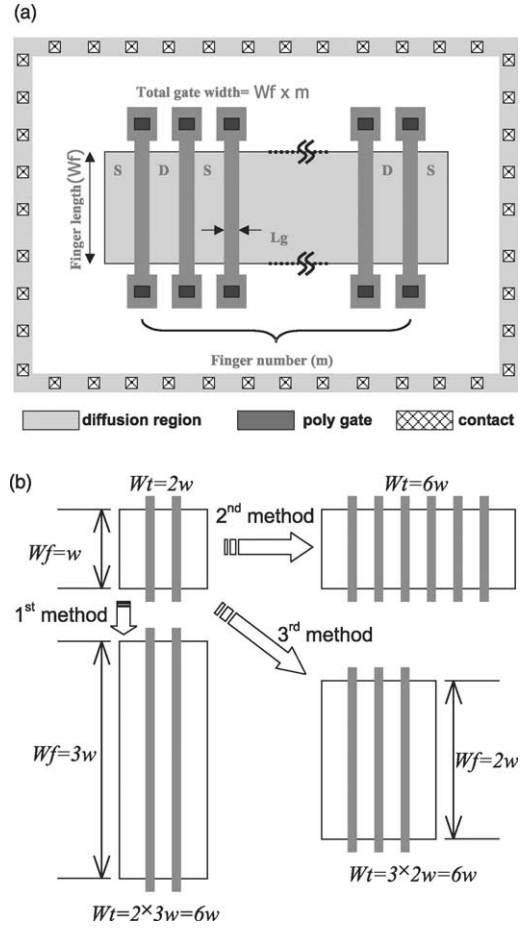


Fig. 3. (a) Top-view of MOSFET cell with multi-finger gates for RF applications. The gate contacts are located at the two ends of polygate. W_f and m represent unit finger length and finger number, respectively. (b) Three methods to scale up W_t.

bution nature in high-frequency range [17]. In this study, multiple ohmic contacts to p-well substrate are formed to surround the active region, as shown in Fig. 3(a). These contacts serve as guard-ring to further reduce the substrate resistance and coupling noise [18,19]. It should be noted that ohmic contacts to p-well substrate can also be designed on only the two sides of the active region.

The latter layout has the advantages of easy characterization and modeling of the substrate resistance [20,21]. However, substrate resistance increases due to increased physical distance of the current path in the MOSFET cell. An increase in substrate resistance raises the intrinsic p-well bias level, causing an undesirable kink effect that is different from the kink effect in SOI technology. The output resistance of MOS transistors is also degraded. To alleviate this undesirable effect, the "guard-ring type" p-well contacts are adopted for all MOS cells used in this work.

In order to scale up the total gate width W_t, e.g., to scale up MOSFET cell with $W_t = 2w$ to $W_t = 6w$, three methods can be used as described in Fig. 3(b). The first method is to scale up the unit finger length W_f while maintaining the original finger number. The second method is to scale up the finger number m while maintaining the original unit finger length. Finally, the third method is to scale up both the finger number and unit finger length. However, secondary effects due to finger-type structure affect not only the static but also the RF behaviors of MOSFET cells. The dependence of unit finger length and the finger number on RF parameters should therefore be investigated separately in order to exactly analyze the impact of finger-type layout on the transistors' RF performance. In general, MOSFET cell with finger-type gates can be regarded as consisting of multiple transistors that are arranged in parallel with respect to each other. Each individual transistor shares its source/drain with its adjacent transistors, therefore its source/drain region is not surrounded by shallow trench isolation.

2.3. Unity-current-gain cut-off frequency, f_T

The f_T of transistor is a common FOM for the speed of a transistor. The f_T is measured in our study by finding the regression line of $|H_{21}|$ and then extrapolated to $|H_{21}| = 1$. This method is more reliable than the gain-bandwidth product method. The f_T can be derived from the Y-parameters of MOSFET by setting $|y_{21}/y_{11}| = 1$ [14,15,22], and is shown as

$$f_T \cong \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}}. \quad (6)$$

The f_T of a 0.13 μm MOSFET cell versus the drain current (I_{ds}) with V_{ds} as a parameter (1.2 and 0.6 V) is shown in Fig. 4. Peak f_T is found to occur at the maximum gate transconductance g_{mx} [3,22]. In addition, no obvious drain bias dependence is found. According to (6), f_T of MOSFET cell should be proportional to $1/L_g^2$, so the dependence on technology scaling can be estimated. The reported f_T as a function of feature size (some in gate length and some in channel length) available from the literature are plotted in Fig. 5(a)

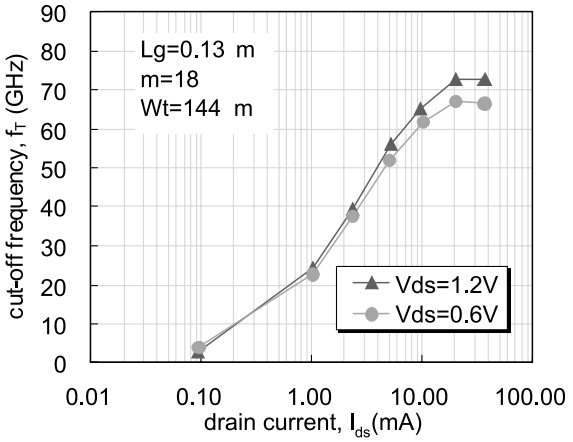


Fig. 4. Cut-off frequency versus drain current with $V_{ds} = 0.6$ V and 1.2 V.

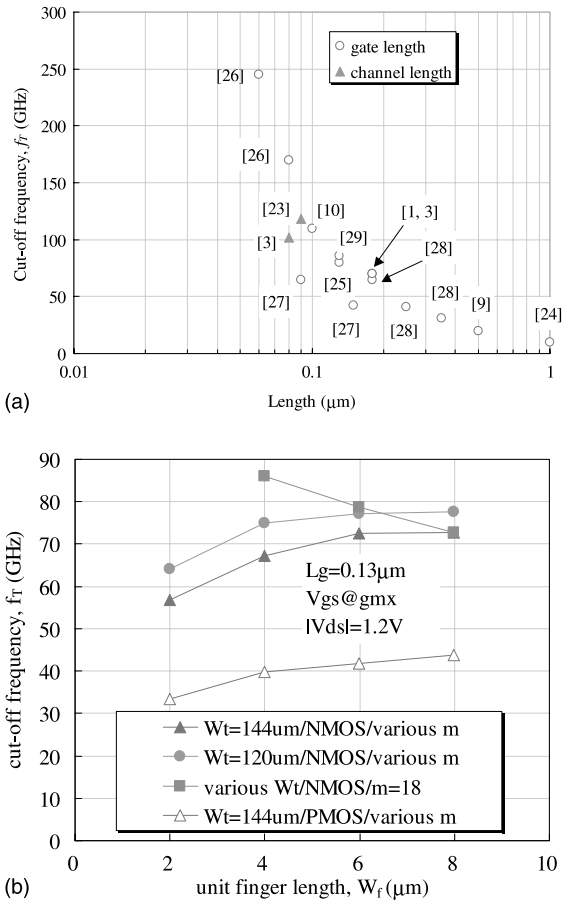


Fig. 5. (a) The reported f_T with respect to technology shrinkage from literature. (b) Cut-off frequency with various geometric parameters. The f_T's in this figure were obtained with V_{gs} biased at g_{mx}.

[1,3,9,10,23–29]. It can be seen that when the gate length is shrunk below 0.1 μm, f_T will exceed 100 GHz.

The dependence of finger number on f_T of MOSFET cells is shown in Fig. 5(b). All f_T's in Fig. 5(b) were obtained with V_{gs} biased at g_{mx}. With a given W_f, f_T is degraded with increasing finger number (i.e., which corresponds to the second method illustrated in Fig. 3(b)). It is found that the peak f_T decreases from 86 to 67 GHz when m increases from 18 to 36 for $W_f = 4$ μm. In addition, increasing W_f with a given m increases f_T (i.e., which corresponds to the first method illustrated in Fig. 3(b)). As shown in Fig. 5(b), the peak f_T can be enhanced from 72.7 to 86 GHz when W_f decreases from 8 to 4 μm for $m = 18$.

2.4. Maximum oscillation frequency, f_{max}

The f_{max} is the bandwidth of a transistor as an active component. In contrast to f_T, f_{max} is very sensitive to the layout due to its strong dependence on parasitic resistance. Two methods can be used to extrapolate f_{max}, i.e., MSG/MAG and Mason's power gain methods [30]. Since the stability factor (i.e., k-factor) of MOSFET is relatively small over a wide frequency range for deep-submicron technology [11,29], the extraction of f_{max} from MSG/MAG is difficult. Rather, Mason's unilateral power gain U is used to find f_{max}. Although U is a popular method to determine f_{max} in recent literatures [3,31], however, it is worthy to note that U could become negative under certain conditions especially in lower frequency range for MOSFET because of the relatively small k-factor. It can be shown that the necessary condition for $U < 0$ is k-factor < 1. Based on the small-signal model of MOSFET, f_{max} can be derived [3,28]

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}}. \quad (7)$$

The f_{max} versus I_{ds} with various W_f is shown in Fig. 6. The bias dependence of f_{max} is mainly due to g_m and g_{ds} as shown in (7). So the peak f_{max} does not occur at the V_{gs} corresponding to the maximum gate transconductance. For I_{ds} larger than 10 mA, f_{max} is degraded because of increased g_{ds}. The reported dependence on gate length from the literature can be found in Fig. 7(a). Although the trend that f_{max} improves with reduced gate length can be found, data are more scattered, when compared to the technology dependence on f_T. This is because some of the reported results were not based on the optimal layouts. In addition, some of the f_{max} was not extracted at the optimal biases. Finally, in some cases the measured frequency was limited to obtain the exact f_{max}. Even though, to design MOSFET cell with optimal f_{max}, geometric parameters W_f and m should be properly chosen. The W_f dependence with a given m can be observed in Fig. 6. It is clearly shown that MOSFET

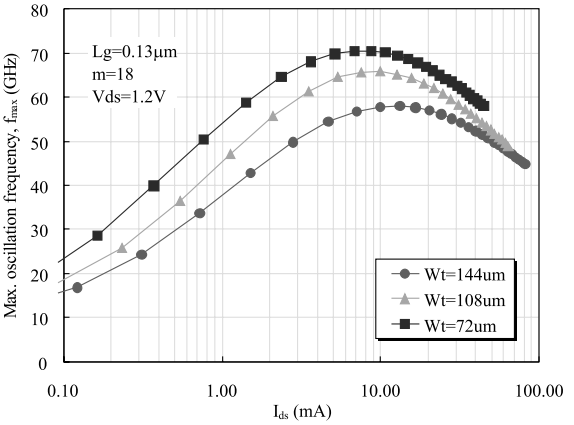


Fig. 6. Bias dependence of f_{max} with various W_t.

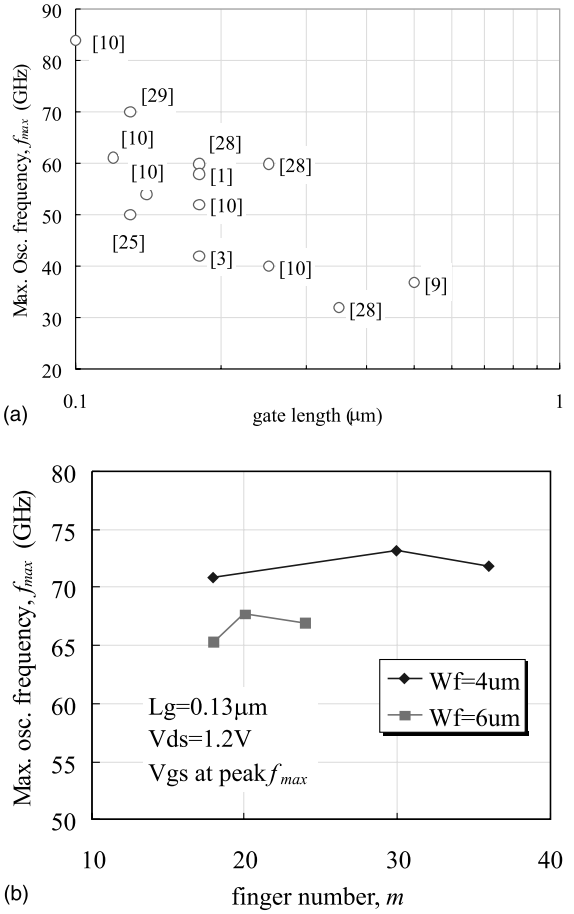


Fig. 7. (a) The reported f_{max} with respect to technology shrinkage from literature, (b) maximum oscillation frequency with various geometric parameters.

cell with larger W_f at a given finger number exhibits higher R_g, C_{gd} and g_{ds} and smaller f_T (i.e., Fig. 5(b)), therefore a lower f_{max}. In addition, the finger number

dependence of f_{max} is shown in Fig. 7(b). The f_{max} exhibits only minor dependence on m at a given W_f. Only 3 GHz variations were found in our experiments. This result can be further confirmed by (7) while normalizing W_t of each terms in (7).

2.5. High-frequency noise of MOSFET cell

The noise sources in MOSFET include terminal resistive noise, channel noise, induced gate noise, $1/f$ noise, and substrate resistive noise. Among them, $1/f$ noise is dominant in lower frequency range (i.e., lower than 100 MHz). The terminal resistive noise is attributed to the parasitic resistance of MOSFET, including the gate resistance and source/drain diffusion resistance. Channel noise is mainly due to the thermal noise generated by the channel carriers [14,16,22,32–36]. Substrate resistive noise is ascribed to the resistive substrate. The fluctuation of V_{bs} due to resistive noise can be coupled by the body transconductance g_{mb} to the drain current [33,37,38]. Lastly, the induced gate noise is attributed to the channel voltage fluctuation and is coupled by the gate capacitance [13,14,22,33]. Contrary to the $1/f$ noise, this noise source increases with frequency.

To investigate the noise in MOSFET cells, a measurable parameter, the minimum noise figure NF_{min} can be used. The NF_{min} of MOSFET can be derived from the small-signal model by incorporating all noise sources, and then transforming the noisy two-port network to the equivalent noise-free network with external noise sources at the input. Detailed derivation can be found in [22]. Hence, NF_{min} of MOSFET is as shown below [3,28]:

$$NF_{min} = 1 + K\frac{f}{f_T}\sqrt{g_m(R_g + R_s)}, \tag{8}$$

where K in (8) is a fitting parameter. It is clearly shown in (8) that NF_{min} improves with the bandwidth. The bias dependence of NF_{min} and associated gain of MOSFET cells can be found in Fig. 8(a). NF_{min} minimum can be obtained at a certain bias. The noise measurements shown in Fig. 8(a) were performed without de-embedding the probing pads. Hence, the thermal noise of resistive p-substrate will be coupled to the pads and increases NF_{min}. The determination of W_f and m dependences of MOSFET cells without pad parasitics is questionable. Therefore, discussions in W_f and m dependence are not included here. However, based on (8) and the reported results in [22], NF_{min} will be degraded with increased W_f, albeit independent with m. Additional discussions in parallel–series configuration and cascade configuration of noise de-embedding can be found in [39] and [40–42], respectively.

Fig. 8(b) shows the reported NF_{min} with respect to the technologies from literature. It can be seen that NF_{min} at 2 GHz for technologies below 0.25 μm is lower than 0.5 dB. For the 0.1 μm technology, NF_{min} smaller than 0.2 dB at 2 GHz can be obtained as expected from (8).

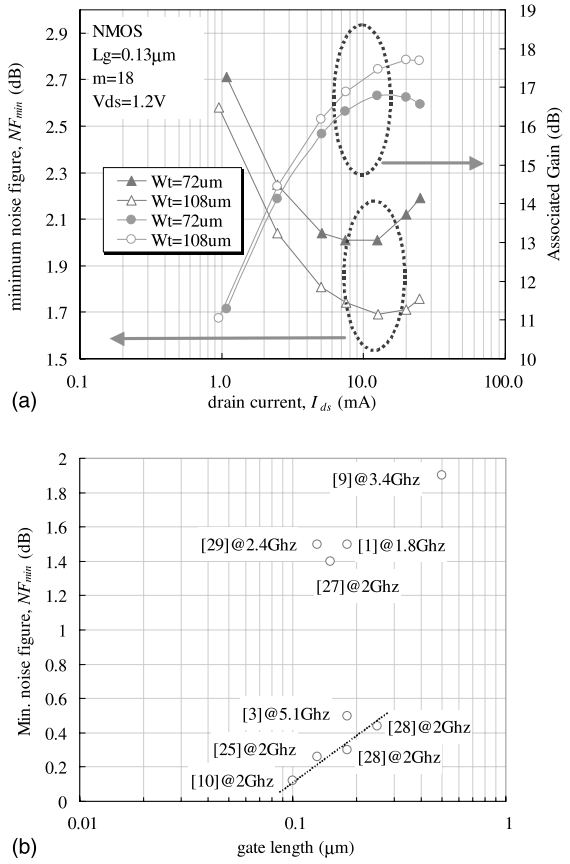


Fig. 8. (a) Bias dependence of NF_{min} various W_t. (b) The reported NF_{min} with respect to technology shrinkage from literature.

3. Varactors

The varactors play an indispensable role in the successful monolithic solutions with RF CMOS technology. Because of their bias-variable capacitance, varactors are widely used in many applications including parametric amplification, harmonic generation, frequency conversion and frequency tuning [43,44]. The key criteria for designing high-performance varactors are high quality factor, high tuning range, voltage compatibility with technology scaling, high self-resonant frequency, and unit high capacitance [45–47].

3.1. Characteristics of varactors

The tuning range of varactors can be determined by performing C–V measurements, and should be as high

as possible to reduce the power consumption. To calculate the tuning range, the bias range should be defined first. Next, the maximum capacitance C_{max} and minimum capacitance C_{min} are determined in this range, the tuning range of a varactor can be calculated as follows [47,48]:

$$\text{tuning\_range} = \pm\frac{\Delta C}{C_{center}}100\%, \tag{9}$$

where $C_{center} = 0.5(C_{max} + C_{min})$, and $\Delta C = C_{max} - C_{min}$. Besides the tuning range, quality factor Q is also an important RF FOM of varactors. Fig. 9 shows a simple equivalent circuit of varactor. R_s is the equivalent in-series resistance, C_j is the equivalent in-series capacitance, R_p is the in-parallel resistance, and L_s is the in-series inductance. Traditionally, Q value can be obtained based on the network theory as shown below:

$$Q = \frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})}. \tag{10}$$

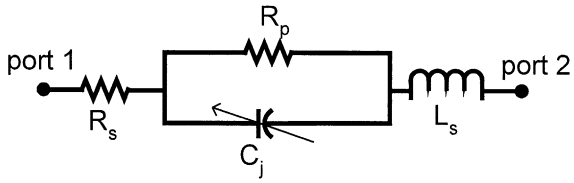


Fig. 9. Small-signal equivalent circuit of varactor.

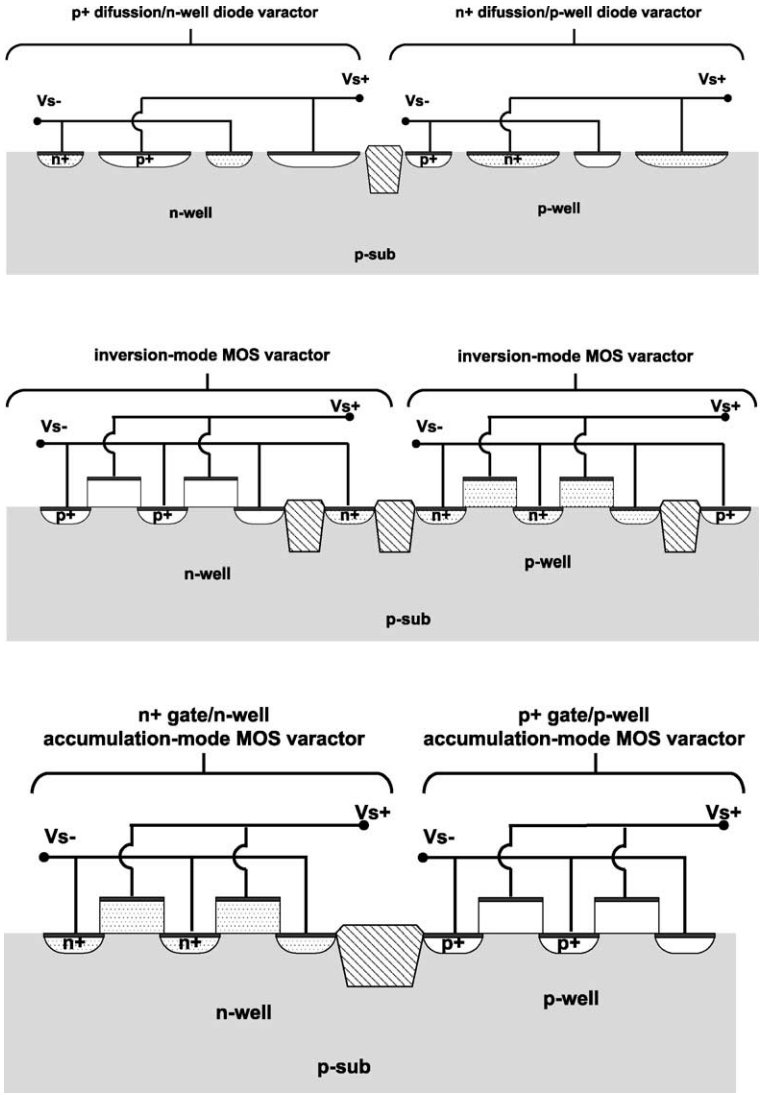


Fig. 10. Types of varactors.

However, definition of Q in this manner is only valid for low-frequency regime. At low frequency, ωL_s can be neglected so Q is roughly estimated as $1/\omega R_s C_j$. At high frequency, however, distribution effect as well as parasitics needs to be incorporated into Y_{11}, and a more precise representation should be used for more accurate estimation of varactor's Q value. Although several methods have been proposed for calculating Q values of passive components, such as phase stability, bandwidth, and the maximum energy methods [49,50], Eq. (10) can still be used to estimate the varactor's Q values in the applied frequency range. In addition, the S-parameter measurements of varactors should be performed extra care in order to extract consistent Q value. This is because the in-series resistance R_s of a varactor is typically only a few ohms, thus the contact resistance between the probe-tips and G–S–G pads will distort the varactor's Q value, and should be taken into account for reliable measurement.

3.2. Types of varactors in RF CMOS technology

In principle, two types of varactors, diode-type and MOS-type varactors, are commonly used for RF applications as illustrated in Fig. 10. The diode-type varactor can be formed in p^+ diffusion/n-well and n^+ diffusion/p-well. The commonly used varactor is the p^+ diffusion/n-well diode due to the smaller well resistance and the isolation between n-well/p-substrate. C–V characteristics of p^+ diffusion/n-well varactors based on 0.18 μm CMOS technology are shown in Fig. 11(a). The usable bias range for diode-type varactor is between the weak forward bias and the reverse bias. The 2-V tuning range (i.e., 0.5 to −1.5 V) of the smallest diode varactors are 25.9%, and 25.7% and 25.5% for the medium and largest diode varactors, respectively. The corresponding Q–V characteristics at 2.4 GHz are shown in Fig. 11(b). The quality factor of varactors decreases with increased bias and p^+ area due to the higher capacitance.

Even the diode varactor exhibits excellent RF performance. The bias range of diode varactor is reduced with the technology scaling [47,48]. For example, diodes can be biased between 0.5 and 1.8 V for 0.18 μm technology, but biased between 0.5 and 1.2 V for 0.13 μm technology. Contrary to the diode varactors, MOS varactors have wider bias range. MOS varactors can be classified as inversion-mode and accumulation-mode MOS varactors, as shown in Fig. 10. The inversion-mode MOS varactor is basically the MOSFET with source, drain and body connected together as one-end. The channel resistance of this type of varactor serves as the main power loss while biased at strong inversion, thus lowering the quality factor [46]. In addition, the gate and well resistance also dissipates power. For the accumulation-mode MOS varactor, as illustrated in Fig. 10, the doping of source, drain, well and gate are of the same type. Advantages of the accumulation-mode MOS varactors are smaller resistive loss, higher capacitance per area and better linearity [1]. In addition, with the trend of technology scaling, the ultrathin gate dielectric and heavy channel doping will increase the unit capacitance. Fig. 12(a) is the C–V characteristics of accumulation-mode MOS varactor with 3.2 nm oxide. All three varactors depict almost the same tuning range of 47.7%. Compared to the diode-type varactor, accumulation-mode MOS varactor depicts better tuning range. The corresponding quality factor at 2.4 GHz is shown in Fig. 12(b). Again, Q value of MOS varactor decreases with increased capacitance, as expected.

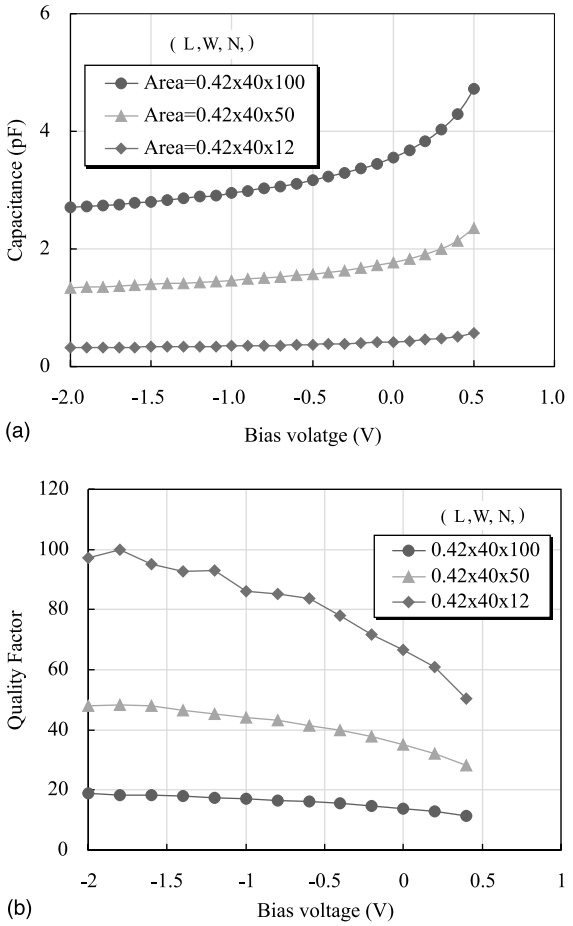
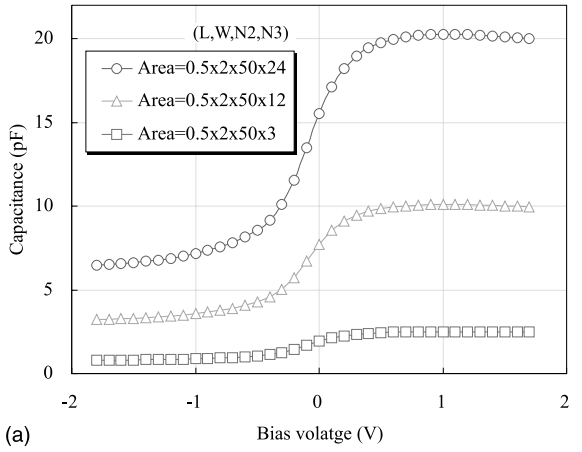


Fig. 11. (a) C–V characteristics of p^+ diffusion/n-well diode varactor. (b) The corresponding quality factor.

4. On-chip inductors

In silicon-based RF technologies, inductor represents an important and potential limitation in RF circuit



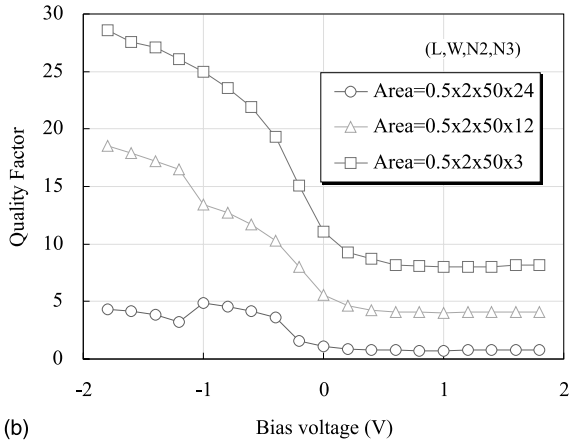


Fig. 12. (a) *C–V* characteristics of accumulation-mode MOS varactor. (b) The corresponding quality factor.

performance for circuits such as VCO, LNA, passive element filters, etc. [12,13,51]. A desirable inductor should possess several features, including high quality-factor for low power loss and high storage energy, high self-resonance frequency for minimum inductance variation with various frequencies, high unit inductance for high integration efficiency [45], and high robustness for minimal process derivation. Considerable efforts have been devoted to meet these goals [52,53].

For silicon-based MMIC, the quality factor degradation of inductor is mainly due to metal loss and substrate eddy current loss. The metal loss includes the ohmic and eddy current loss. To reduce the metal loss in order to enhance the quality factor, there are two approaches. The first approach is to use low resistive metal as the inductor coils. The second approach is to employ taper inductor to reduce eddy current loss of metal line [54–57]. To achieve a low resistive metal, an effective way is to use a low-resistivity metal and/or increase the metal thickness. Fig. 13 shows the Q and inductance of

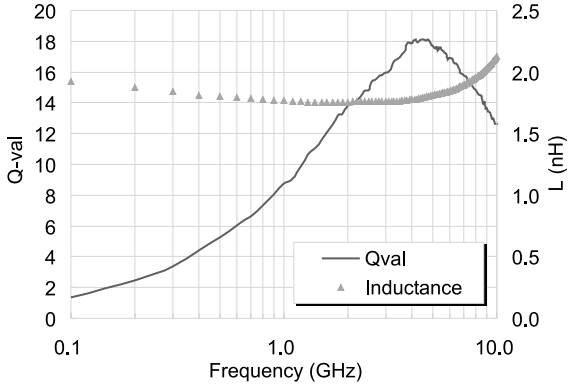
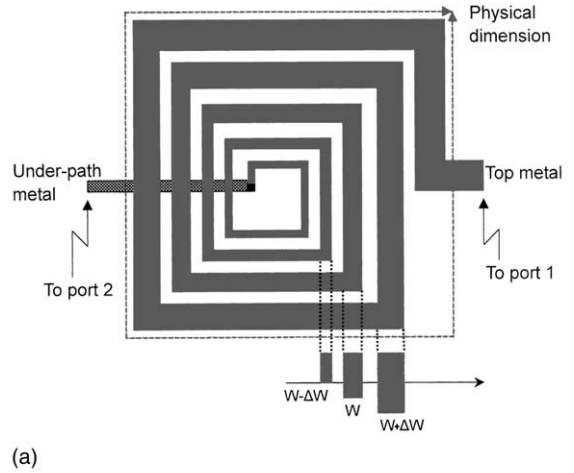


Fig. 13. Quality factor and inductance versus frequency of a 2.8-μm thick copper top-wiring layer.



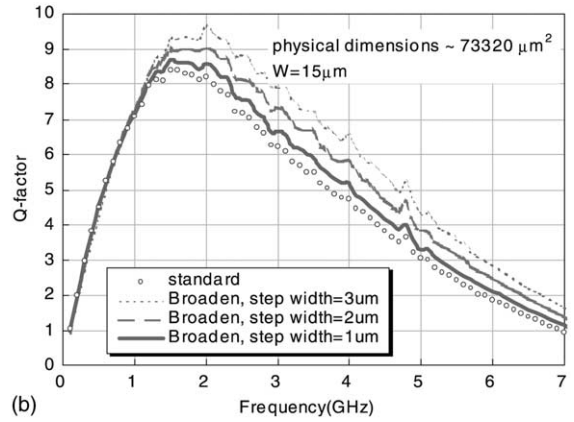


Fig. 14. (a) The spiral inductors with arithmetically progressive width. (b) The quality factor.

copper metal in top-wiring layer with a thickness of 2.8 μm. The Cu inductor gives, for a 1.7 nH inductor, a peak Q of 18 at 4.8 GHz and Q of 14 at 2.4 GHz. It should be

noted that to improve Q value by thickening the metal is limited by the skin depth of the metal, hence, an even thicker Cu would not help improve the Q value obviously. On the other hand, eddy current loss, that shows much stronger frequency dependence [58,59], can be reduced by using arithmetically progressive width pattern as shown in Fig. 14(a). Since the distribution of magnetic field is concentrated in the inner turns of the spiral inductor, rather than in the outer turns, the induced eddy current loss is more significant in inner turns of the spiral inductor. In addition, the eddy current loss is proportional to the metal stripe area in which the magnetic field penetrates. With a larger ΔW, the eddy current loss is more significantly reduced, because of the larger reduction in metal width of the inner turns. The experimental results can be found in Fig. 14(b), the broadening spiral inductor with $\Delta W = 3$ μm exhibits a high Q of 9.68 at 2.0 GHz. Compared to the conventional inductor (with constant W), the Q-factor has improved by 18.8%.

In addition, pattern ground plate underneath the inductor can be used to reduce the substrate loss. Pattern ground shielding using polysilicon has been recognized as a useful method to prevent substrate eddy loss [60]. In our work, three kinds of materials for ground-shield were investigated, i.e., metal, ploysilicon and silicide without polysilicon underneath it. The improvement of Q-factor can be obtained by the polysilicon and silicide pattern ground as shown in Fig. 15, both providing 16% peak Q increase. In contrast, no improvement is found for the metal-1 pattern ground. This is because the silicide and polysilicon provided better eddy current shielding, while metal does not.

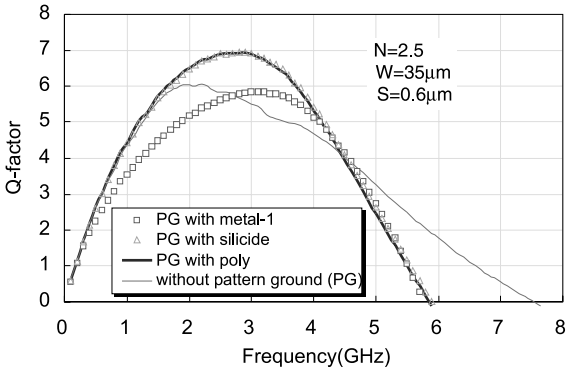


Fig. 15. Quality factor of spiral inductor by using pattern ground plate to reduce the substrate loss.

5. Metal–insulator–metal capacitors

Even the varactors can provide the capacitive characteristics for RF blocks, however, in some specific

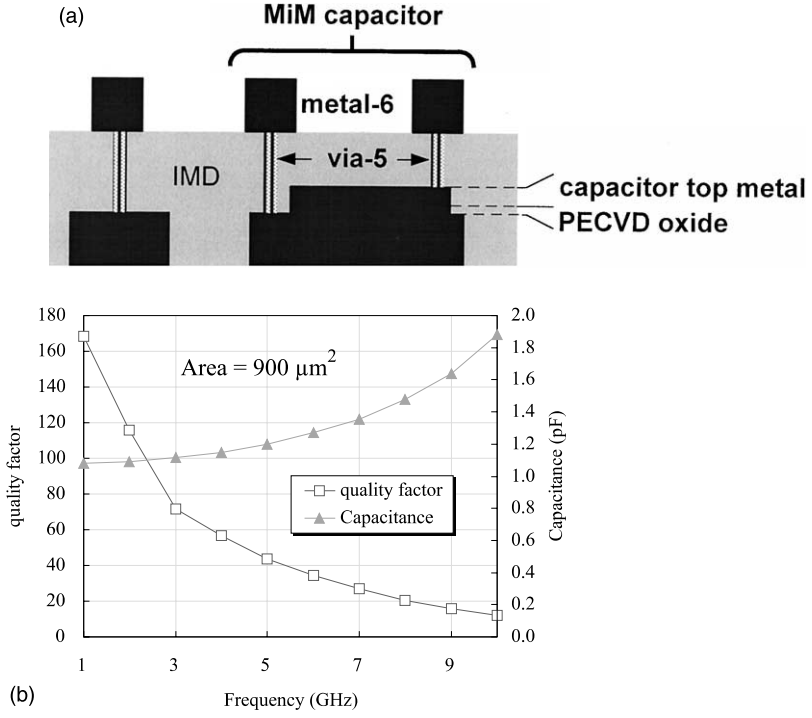


Fig. 16. (a) The cross-section of MiM capacitor, and (b) its capacitance and quality factor characteristics.

cases, varactors cannot satisfy the demand of linear capacitance for matching network. Instead, MiM capacitor can be developed to serve this purpose. Three types of MiM capacitors are commonly developed. The first type is the mesh capacitor, which adopts the interconnect arrays that are arranged as mesh fixture [61]. The second type is the plate capacitor fabricated with existing metal layers [45], for example, metal-4 and metal-5. The third type is the plate capacitor with thin oxide, which can be fabricated by depositing an extra metal layer [1]. The first two types can be fabricated without additional process steps or mask, however, the unit capacitance is relatively small compared to the plate capacitor with thin oxide.

Fig. 16(a) shows the cross-section of a MiM capacitor that exhibits high capacitance per area. The bottom plate of MiM capacitor is made of metal-5, with an additional thin metal layer between metal-5 and metal-6 as the top plate. The dielectric of MiM capacitor is the PECVD oxide with a thickness of 37.2 nm. The quality factor of MiM capacitor is 118 at 2.4 GHz as shown in Fig. 16(b). Capacitance per area of this capacitor is 1 fF/μm^2, which is about 30 times higher than that of the plate capacitor with crude metal layer (i.e., the second type of MiM capacitor as described in Section 5). In addition to the quality factor, the voltage coefficient and the temperature coefficient are 61.6 ppm/V and 52.25 ppm/°C, respectively. These results indicate that MiM capacitor depicts highly linear characteristics. Finally, the leakage current of this MiM capacitor is smaller than 1 fA/μm^2 at a dc bias of 10 V (data not shown).

6. Coupling noise

A critical issue in system integration is the substrate coupling noise [4], which could be induced by digital circuits disturbing small-signal analog circuits, or by a large-signal RF circuit (such as oscillators, power amplifiers) disturbing a small-signal circuit. The noise propagation is aggravated in standard CMOS technology using low-resistivity substrate. High-resistivity substrate, though capable of improving coupling noise as well as reducing component signal loss [62], may induce serious latch-up problems. The coupling noise reduction can be achieved by either reducing the noise source or adding a noise stopper. The latter approach is more popular, and can be accomplished by using p^+ guard-ring or deep n-well isolation [18,19]. As shown in Fig. 17, with p^+ diffusion representing a noise injector, the deep n-well can be placed around the p^+ injector and biased through a surface n-well that is connected to the deep n-well. The proposed deep n-well should be deep enough to minimize disturbing the dc characteristics of MOSFETs, but not so deep so that it can be connected

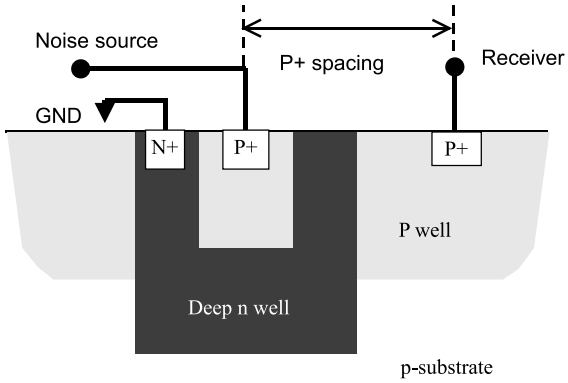


Fig. 17. Illustration of substrate coupling experiment.

to the regular n-well. Consequently, the received noise power is measured from another p^+ diffusion, namely the noise receiver, using a network analyzer to measure its forward power gain S_{21}. As shown in Fig. 18(a), the coupling noise measured from the receiver is improved by 40 and 25 dB at 100 MHz and 2.4 GHz, respectively. Distance between the noise source and the receiver in this experiment is 100 μm. These results demonstrate

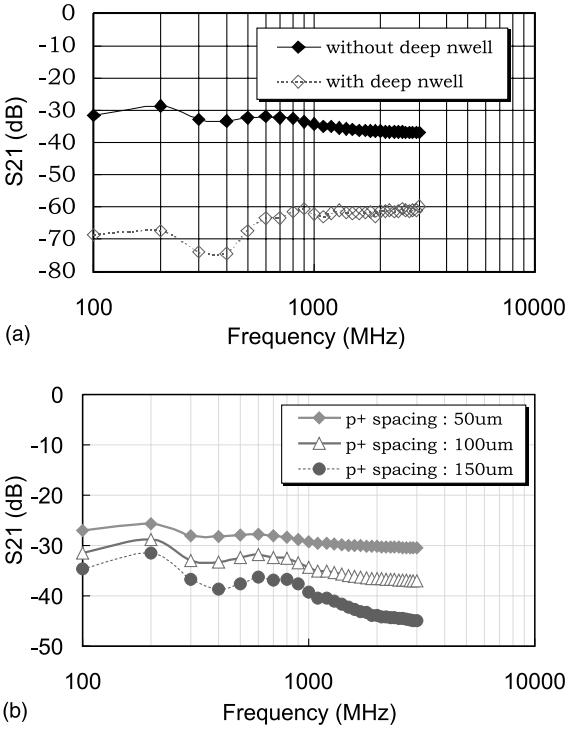


Fig. 18. (a) Comparison between p^+ diffusion with and without deep n-well isolation. (b) Substrate coupling for various p^+ diffusion distances.

that placing a deep n-well around the noisy circuits can successfully eliminate the coupling noise to other sensitive circuits. It should be noted in Fig. 18(b) that, although increasing the inter-p^+ spacing also reduces the injected noise, the amount of noise power reduction is only around 5 dB per 50 μm spacing increase, which is mush less effective than applying a deep n-well.

7. Conclusion

In this paper, the dimensional analysis of RF FOMs of 0.13 μm RF CMOS were characterized and discussed. It is shown that f_T of 86 GHz and f_{max} of 70 GHz can be obtained with nMOSFET cells with $W_t = 72$ μm, $W_f = 4$ μm and $m = 18$. The NF_{min} of 1.5 dB without pads de-embedding was observed in nMOSFET with $W_t = 144$ μm, $W_f = 4$ μm and $m = 36$. In addition, high performance passive components such as varactors, inductors and MiM capacitors can be implemented by adopting CMOS technology for RF networks. Finally, noise due to substrate coupling can be effectively suppressed by adding a deep n-well isolation. The successful implementation of all active and passive components offers a complete solution for single-chip application.

Acknowledgement

This work was supported in part by National Science Council, Taiwan, ROC, under Contract NSC90-2215-E009-072.

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