Active ESD Protection Design for Interface Circuits Between Separated Power Domains Against Cross-Power-Domain ESD Stresses

Shih-Hung Chen, Ming-Dou Ker, *Fellow, IEEE*, and Hsiang-Pin Hung

***Abstract*—Several complex electrostatic discharge (ESD) failure mechanisms have been found in the interface circuits of an IC product with multiple separated power domains. In this case, the machine-model (MM) ESD robustness cannot achieve 150 V in this IC product with separated power domains, although it can pass the 2-kV human-body-model (HBM) ESD test. The negative-to-VDD (ND) mode MM ESD currents were discharged by circuitous current paths through interface circuits to cause the gate oxide damage, the junction filament, and the contact destruction of the internal transistors. The detailed discharging paths of ND-mode ESD failures were analyzed in this paper. In addition, some ESD protection designs have been illustrated and reviewed to further comprehend the protection strategies for cross-power-domain ESD events. Moreover, one new active ESD protection design for the interface circuits between separated power domains has been proposed and successfully verified in a 0.13-μm CMOS technology. The HBM and MM ESD robustness of the separated-power-domain interface circuits with the proposed active ESD protection design can achieve over 4 kV and 400 V, respectively.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, separated power domains.**

I. Introduction

As ultra-large-scale-integrated (ULSI) circuits are being continually developed toward system-on-chip (SoC) applications, more and more multiple separated power domains are used in an SoC IC for specified circuit functions, such as digital/analog circuit blocks, mixed-voltage circuit blocks, and power management considerations. However, the IC products with multiple separated power domains often have more unexpected current paths during electrostatic discharge (ESD) stresses and easily cause damages across interface circuits between different power domains beyond the ESD protection circuits of I/O cells [1]–[5]. Such ESD failures across interface circuits between different power domains are often difficult to be clearly examined and revised, even with a lot of failure analysis procedures. In this paper, a failure study of the internal ESD damage on the interface circuits of a 0.35-μm 3.3/5-V mixed-mode CMOS IC product with two separated power domains is presented [6]. The ESD failure spots were specially observed at the interface circuits of the separated power domains after the negative-to-VDD mode (ND-mode) machine-model (MM) ESD stress [7] of 100 V. However, this IC product has 2-kV human-body-model (HBM) ESD robustness [8] in each ESD test combination of I/O pin to power/ground pins. Therefore, the efficient ESD protection designs should be applied on the interface circuits between the separated power domains against such cross-power-domain ESD stresses.

Several cross-power-domain ESD protection designs had been studied and proposed to avoid ESD damages on the interface circuits between two separated power domains [1]–[6]. The bidirectional diode connection had been generally used to connect the separated power or ground pins in different power domains. The bidirectional diode connection can construct the completely whole-chip ESD current discharging paths under cross-power-domain ESD stresses [9], [10]. According to previous studies [10]–[12], the overstress voltages across the interface circuits between separated power domains easily caused the ESD damages, such as the gate oxide damage, the junction filament, and the contact destroy under cross-power-domain ESD stresses. Therefore, the second ESD clamp designs had been applied to reduce the overstress voltages across the interface circuits. Furthermore, the second ESD clamp with the desired trigger mechanism also had been proposed to rapidly and efficiently clamp the overstress voltages across the interface circuits between separated power domains, particularly in the integrated circuits with a nanoscale CMOS technology [10]–[12].

In this paper, several active cross-power-domain ESD protection designs were reviewed to compare their ESD protection strategies for interface circuits between separated power domains. Furthermore, one new active ESD protection design for the interface circuits between separated power domains has been also proposed to solve the interface circuit damages under cross-power-domain ESD stresses. This ESD protection design has been implemented by PMOS and NMOS transistors with the ESD-transient detection function in a 0.13-μm 1.2-V CMOS technology. It can be rapidly triggered on and efficiently reduce the overstress voltages across the gate oxides of the

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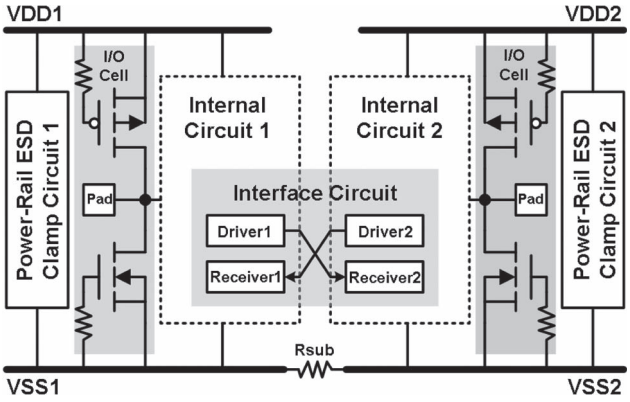

Fig. 1. ESD protection scheme in an IC product with separated power domains. The ESD protection circuits included input, output, and power-rail ESD clamp circuits.

MOS transistors of the receivers in interface circuits between separated power domains under the cross-power-domain ESD stresses. The proposed ESD protection design for the interface circuits between separated power domains has been successfully verified with 4-kV HBM and 400-V MM ESD robustness against cross-power-domain ESD stresses.

II. Failure Study Under Cross-Power-Domain ESD Stresses

A. ESD Protection Cell Designs for the Commercial IC Product With Separated Power Pins

The ESD protection scheme for input, output, and power-rail ESD clamp circuits in this IC product is shown in Fig. 1. Internal circuit 1 is a digital circuit block, and internal circuit 2 is an analog circuit block. Each circuit block has an individual power-rail ESD clamp circuit. The gate-grounded NMOS (GGNMOS) and the gate-VDD PMOS (GDPMOS) with a channel length/width of 0.8/300 μm are used for pad-to-VSS and pad-to-VDD ESD protection at each I/O pad, respectively. The power-rail ESD clamp circuit, which is implemented with the substrate-triggered field-oxide device (STFOD) [13], [14] with an RC-based ESD transient detection circuit [15], is individually installed in each power domain, as illustrated in Fig. 1. The perimeter of the STFOD is equivalent to 216 μm. The STFOD as a power-rail ESD clamp circuit of a VDD (or VSS) cell had been successfully verified with over 4-kV HBM and 400-V MM ESD robustness in this 0.35-μm 3.3/5-V CMOS process. In addition, each I/O cell with GGNMOS and GDPMOS of a 300-μm channel width had been also verified to achieve over 4-kV HBM and 400-V MM ESD robustness in the same process. Due to noise consideration between power domains, the VDD1 was separated from the VDD2. Then, the VSS1 and VSS2 only connected by the parasitic p-substrate resistance (Rsub) without bidirectional diode connection in this chip.

B. Internal ESD Damages on the Interface Circuits Between Separated Power Domains

After HBM ESD tests of all I/O pins to each power/ground pin and power-to-ground ESD test, the HBM ESD robustness achieved 2 kV, which is the basic specification for commercial IC products. However, the MM ESD robustness cannot achieve 200 V in positive-to-VSS mode (PS-mode), positive-to-VDD mode (PD-mode), negative-to-VSS mode (NS-mode), and ND-mode MM ESD stresses. Even the ND-mode MM ESD robustness of Pin-A and Pin-B cannot achieve 200 V by VDD1 and VDD2 shorting together in the test board under the ND-mode ESD stress. The ESD test results for this IC product are shown in Table I.

TABLE I
HBM and MM ESD Robustness of the Pin-A and Pin-B I/O Pins in This IC Product

ESD Test	I/O Pins	PS-Mode	NS-Mode	PD-Mode	ND-Mode
HBM	Pin-A	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
	Pin-B	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
MM	Pin-A	150 V	150 V	150 V	150 V
	Pin-B	150 V	150 V	150 V	100 V

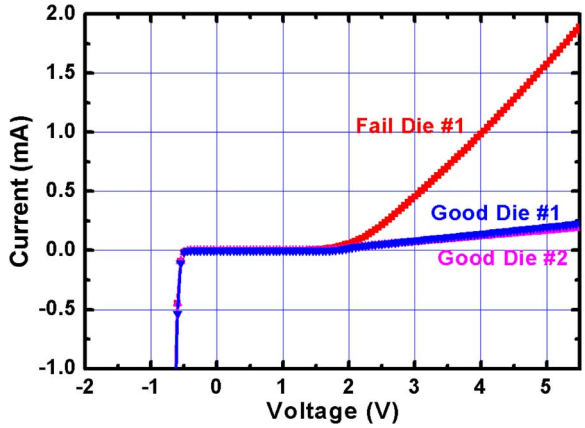

Fig. 2. After the ND-mode MM ESD stress on I/O pins, the I–V characteristics of VDD2-to-VSS2 showed higher leakage currents than those before the ESD stress.

After the ESD tests are finished, a monitor on the leakage current is used to judge whether the I/O pin under the ESD test is passed or failed. The traced I–V characteristics of the investigated IC before and after the ESD stress are shown in Fig. 2. Obviously, after the 200-V MM ESD stress, the leakage current at 3.3 V between VDD2 and VSS2 showed a leakage current about 10 times higher, as compared with that of good dies. From the measured I–V characteristics, there are some ESD damages in the internal circuits between VDD2 and VSS2 after the ESD stress. These internal ESD damages have been also clearly observed by the physical failure analysis, such as an emission microscope (EMMI) and a scanning electron microscope (SEM).

C. Failure Mechanism Under Cross-Power-Domain ESD Stresses

To indicate the failure locations caused by ND-mode MM ESD stresses, the EMMI was used to find abnormal ESD failure

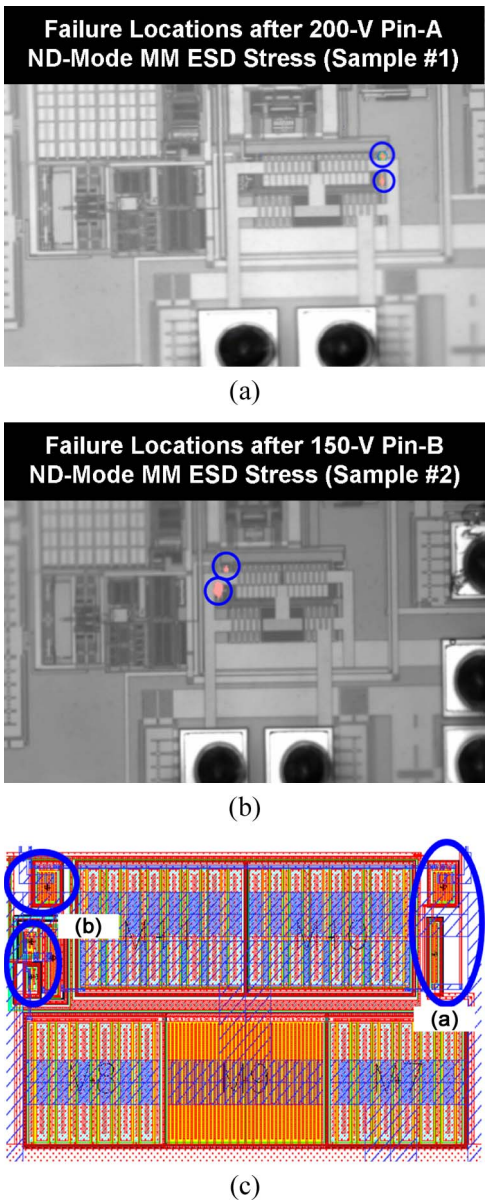

Fig. 3. According to the EMMI failure analysis, abnormal hot spots were found at the interface circuits (see the circled areas) after the ND-mode MM ESD stress on (a) Pin-A and (b) Pin-B. (c) Corresponding layout locations of the interface circuits were indicated as the failure spots in (a) and (b).

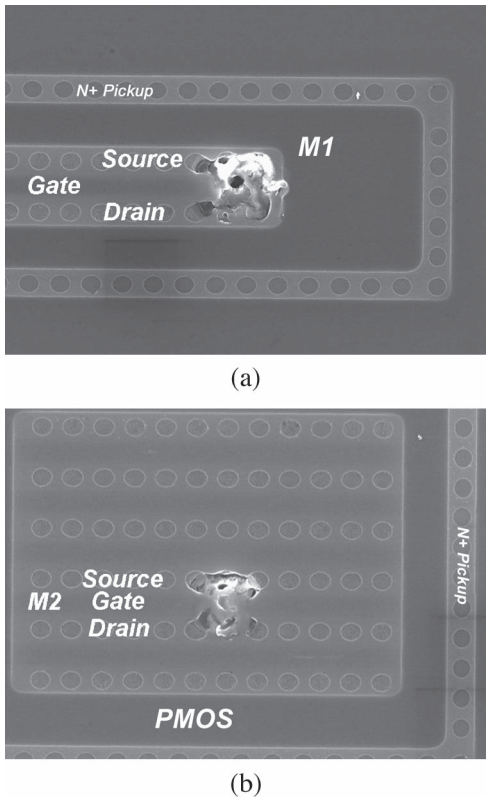

Fig. 4. After the ND-mode MM ESD stress on Pin-A, the failure spots were located at (a) PMOS transistor (M1) and (b) the other PMOS transistor (M2).

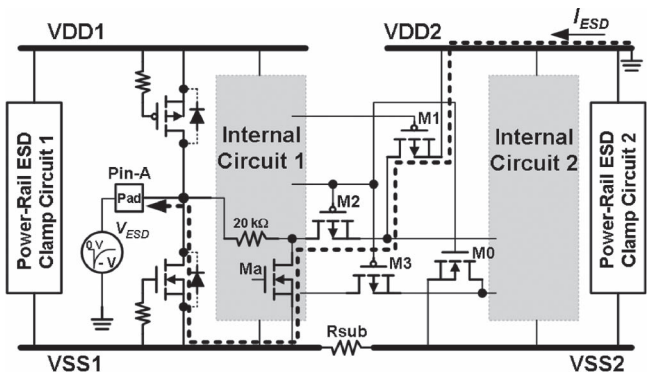

Fig. 5. ESD current could be discharged through the circuitous path to cause ESD damages to M1 and M2 during the ND-mode MM ESD stress on Pin-A.

spots in this IC. The measured EMMI photos are shown in Fig. 3(a) and (b) with the corresponding IC layout patterns of the ND-mode MM ESD failure sample. All the circled areas in Fig. 3(c) are the ESD damage locations indicated by the EMMI around the interface circuits after the ND-mode MM ESD stress. The ESD damages are recognized at the interface circuits by comparison with circuits and layout patterns to the SEM photos of ESD damaged failure spots. After the Pin-A ND-mode MM ESD stress, the SEM photos of failure spots are shown in Fig. 4(a) and (b). The clear failure spots were found in two PMOS transistors (M1 and M2) of the interface circuits. However, Pin-A is connected to internal circuit 1 through a 20-kΩ polyresistor, which can effectively block the ESD currents to damage internal circuits near the I/O cell. Therefore, the ESD current could be discharged by the circuitous path to cause damages on M1 and M2 after the Pin-A ND-mode MM ESD stress, as shown in Fig. 5. Due to the larger device size of Ma in Fig. 5, the ESD current did not destroy it during the ND-mode MM ESD stress. On the other hand, the failure spots were also found in the two transistors of interface circuits after the Pin-B ND-mode MM ESD stress, as shown in Fig. 6(a) and (b). ND-mode MM ESD currents were discharged by two mainly current paths, as shown by the dashed lines in Fig. 7. These two paths provided the current paths to the distributive discharge ESD current. The corresponding failure photos on the interface devices Mb and M3 are shown in Fig. 6(a) and (b), respectively.

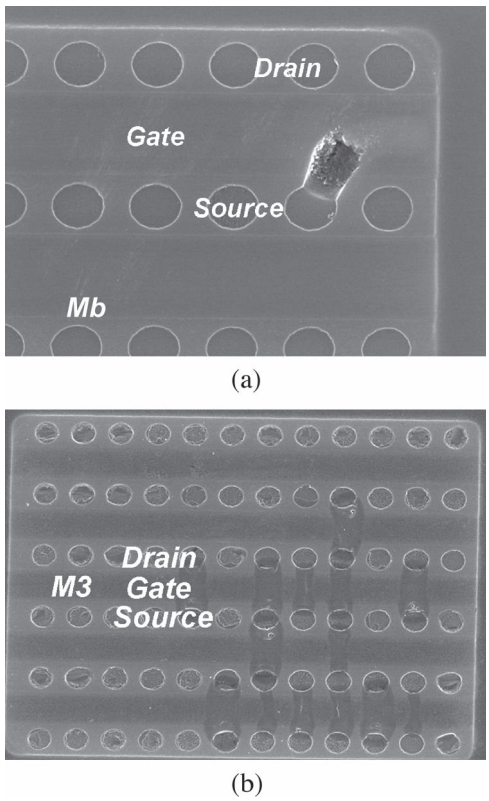

Fig. 6. (a) NMOS transistor (Mb) and (b) PMOS transistor (M3) of the interface circuits were destroyed after the ND-mode MM ESD stress on Pin-B.

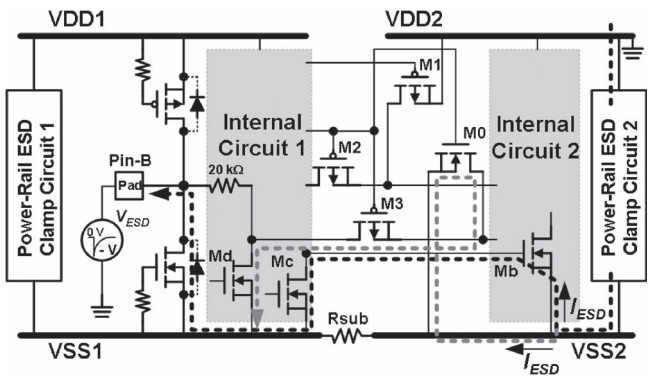

Fig. 7. ESD discharging paths during the ND-mode MM ESD stress on Pin-B. Mb and M3 were damaged after such ESD stress.

D. Proposed Solutions to Rescue Such ESD Failures

To overcome such ESD failures at the interface circuits between separated power domains, adding the suitable blocking resistors (Rblock) to the interface devices and installing the bidirectional diode connection in the original ESD protection scheme were proposed in Fig. 8. Two extra blocking resistors are added at the source terminal of M1 and the gate terminal of Mb, respectively. The bidirectional diode connection was used to connect the separated ground lines (VSS1 and VSS2). The diode numbers of the bidirectional diode connection were optimized to prevent the different ground-line noise coupling issue between the separated ground lines of analog and digital

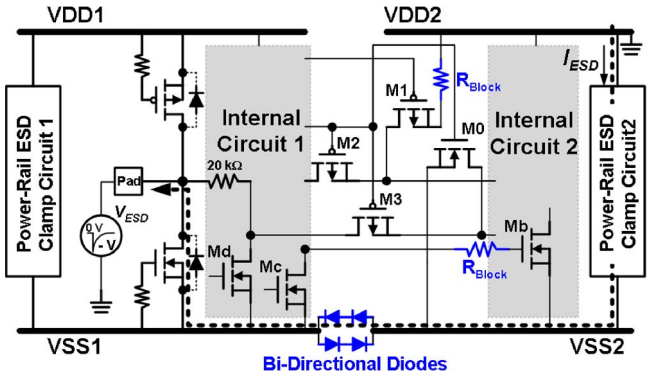

Fig. 8. Proposed ESD protection solution to rescue ESD failures at the interface circuits of this IC product with separated power domains.

circuit blocks. To further provide higher ground-line noise coupling isolation, the bidirectional silicon-controlled rectifier (SCR) [16] with an ESD-detection circuit can be used to replace the bidirectional diode connection between the separated power lines (VDD1 and VDD2). By using the proposed ESD protection solutions, the ESD current will be effectively discharged along the desired connection of ground lines under the ND-mode MM ESD stress. In addition, the blocking resistors can also avoid the ESD currents that are discharging through the undesirable paths. Therefore, the abnormal internal ESD damages can be overcome in this IC product with separated power lines.

III. Active ESD Protection Designs for the Interface Circuits Between Separated Power Domains

A. ESD Threats and Damages of the Interface Circuits Between Separated Power Domains

With more circuit blocks integrated into an IC product to meet different applications, such circuit blocks usually have separated power domains to supply the power and ground signals in each individual circuit block. In addition, the interface circuits were also adopted to communicate with different circuit blocks inside the chip. However, the interface circuits between separated power domains are often damaged under cross-power-domain ESD stresses [1]–[6]. The bidirectional diode connections between the separated power domains are usually applied to construct a completely whole-chip ESD protection design [9], [10], as shown in Fig. 8. In general, the bidirectional diode connections are only used to connect the separated VSS pins due to different VDD1 and VDD2 voltage levels and noise-coupling considerations [9], [10].

When the ESD voltage was applied on VDD1 and grounded VDD2 under the cross-power-domain ESD stresses, the ESD current could be discharged from VDD1 to VSS1 by power-rail ESD clamp circuit 1 in power domain 1, from VSS1 to VSS2 through the inserted bidirectional diode connection, and then from VSS2 to grounded VDD2 through the other power-rail ESD clamp circuit 2 in power domain 2, as shown by the discharged path (dashed lines) in Fig. 9(a). Vh1 and Vh2 are the holding voltages of power-rail ESD clamp

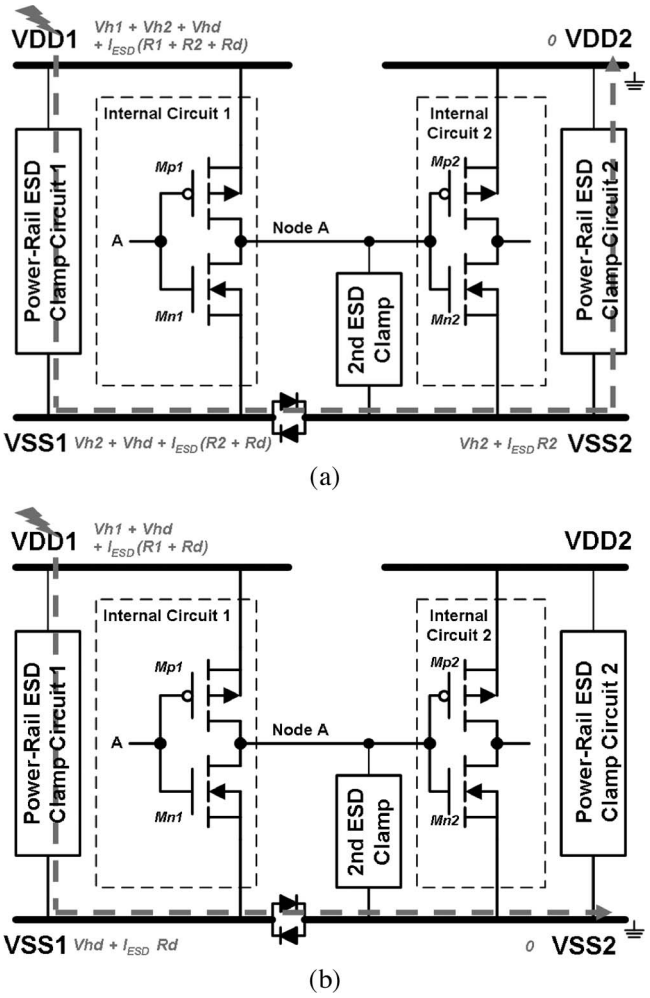

Fig. 9. Estimations of the induced voltage potential under the cross-power-domain (a) VDD1-to-VDD2 and (b) VDD1-to-VSS2 ESD stresses.

circuits 1 and 2, respectively. Then, Vhd is the holding voltage of the bidirectional diode connection between the separated power domains. Among the parameters, R1, R2, and Rd are the turn-on resistances of power-rail ESD clamp circuits 1 and 2, and the bidirectional diode connection, respectively. When the ESD current was conducted by this long discharging path, it induced the overstress voltage across each MOS transistor in the interface circuits between separated power domains [10]–[12]. The induced voltage drops with discharging ESD currents from VDD1 to VDD2 on each node of the interface circuit had been estimated, as shown in Fig. 9(a). The voltage potential at node A could be raised up to VDD1 because the driver's PMOS transistor (Mp1) had an initially floating gate situation. The highest voltage drop was applied across the gate oxide of the receiver's PMOS transistor (Mp2) in the interface circuits under the VDD1 to VDD2 ESD stresses.

On the other hand, the highest voltage drop was also generated across the gate oxide of the receiver's NMOS transistor (Mn2) in interface circuits under the VDD1 to VSS2 ESD stresses. The similar estimation on voltage drops during the ESD stress was presented in Fig. 9(b). Therefore, the second

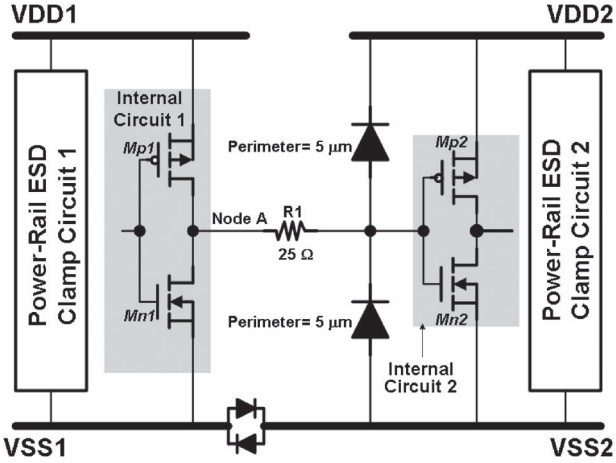

Fig. 10. ESD protection design with a resistor-diode clamp had been proposed to protect the interface circuits between separated power domains [10].

ESD clamp designs were usually installed near the MOS transistors of the receiver to reduce the overstress voltage under the cross-power-domain ESD stresses [10]–[12], as shown in Fig. 9(a) and (b). As CMOS technology is being continually shrunk toward nanometer scales, the breakdown voltages of the ultrathin gate oxide in the MOS transistors were sharply reduced to impact the ESD protection designs. It was important to avoid the gate oxide damages of the MOS transistors in the interface circuits by ESD-current-induced overstress voltages. The overview on some second ESD clamp designs will be presented and compared in Section III-B.

B. Review on ESD Protection Designs for Interface Circuits Between Separated Power Domains

The resistor-diode clamp design [10], which consists of a resistor (R1) and two diodes, was allocated in the interface circuits between separated power domains to restrict the ESD current distribution and to clamp the overstress voltage across the gate oxide of the receiver's MOS transistors, as shown in Fig. 10. These two clamped diodes can be respectively replaced by the GGNMOS transistor and the GDPMOS transistor to further enhance the clamping efficiency. However, such traditional junction-breakdown clamp designs with diodes, GGNMOS, or GDPMOS could not be suitable for interface circuits with the ultrathin oxide against cross-power-domain ESD stresses. Therefore, some second ESD protection designs with special trigger mechanisms, such as the modified interface circuits with special drivers and receivers [11] as well as the ground-current-trigger (GCT) NMOS transistor [12], had been proposed to efficiently reduce the overstress voltages across the ultrathin gate oxides of the MOS transistors in interface circuits between separated power domains.

The special driver and receiver had been implemented for interface circuits between separated power domains, which were collaborated with an ESD detector to accomplish differently desired functions under the cross-power-domain ESD stress condition and the normal circuit operation condition, as presented in Fig. 11(a) and (b) [11]. The special driver

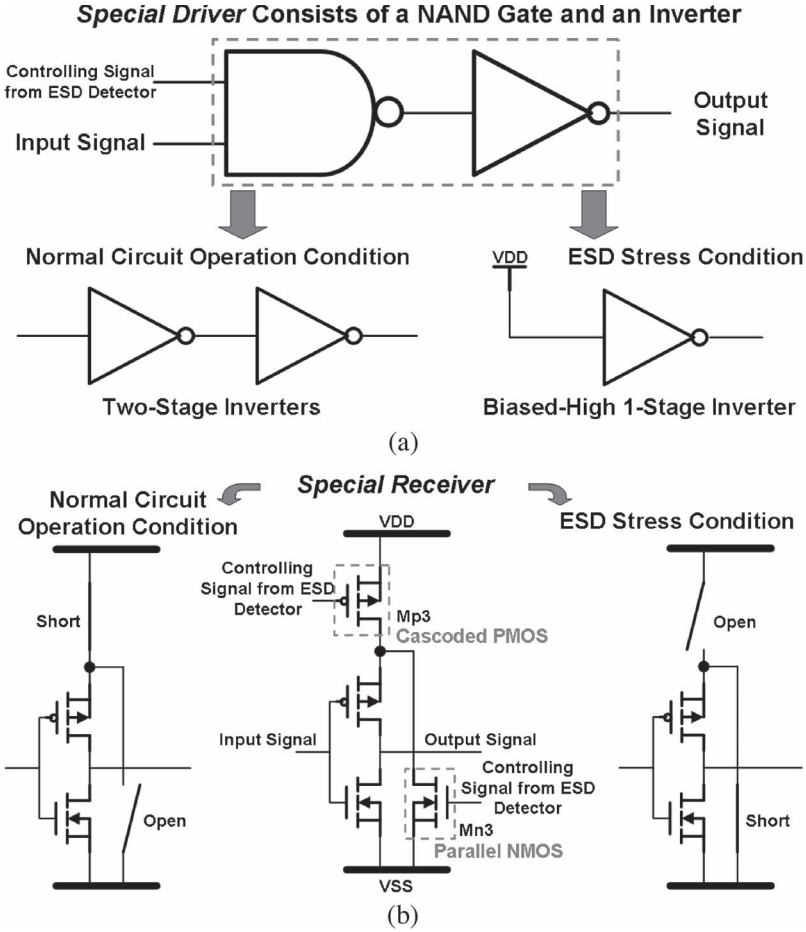

Fig. 11. ESD protection design with (a) special driver and (b) special receiver for interface circuits between separated power domains [11].

was composed of a one-stage NAND gate and a one-stage inverter. Through different signals from the ESD detector, the driver can be performed respectively as cascaded two-stage inverters and a biased-high one-stage inverter under a normal circuit operation condition and the VDD1-to-VDD2 cross-power-domain ESD stress, as illustrated in Fig. 11(a). In addition, the special receiver consisted of a one-stage inverter, a PMOS transistor (Mp3) cascaded on the inverter, and an NMOS transistor (Mn3) in parallel to the inverter. The cascaded PMOS and the parallel NMOS transistors, both of which were controlled by the ESD detector, will be respectively turned on and off under the normal circuit operation condition, whereas Mp3 and Mn3 will be respectively turned off and on under the cross-power-domain ESD stress, as shown in Fig. 11(b). Although such special designs in the driver and the receiver [11] can reduce and restrain the overstress voltage across the gate oxide of the receiver's PMOS and NMOS transistors, the complicated connection could be an obstacle to practical applications.

On the other hand, the GCT NMOS transistor [12] had been also proposed to act as a second ESD clamp for the interface circuits between separated power domains, as shown in Fig. 12. The GCT NMOS transistor can be turned on to clamp the overstress voltage across the gate oxide of the receiver's PMOS and NMOS transistors by the induced voltage drop between VSS1 and VSS2 under the cross-power-domain ESD stress.

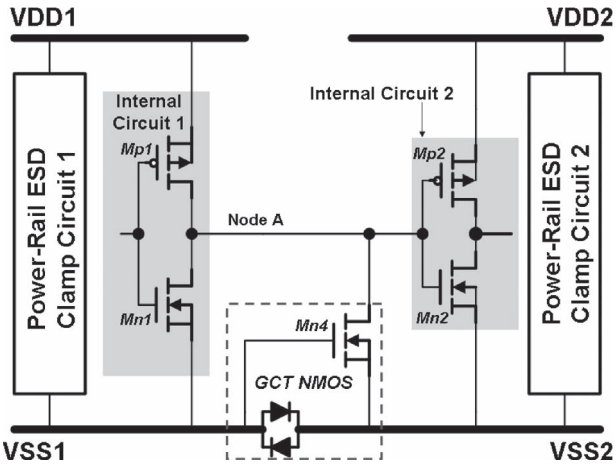

Fig. 12. ESD protection design with the GCT NMOS transistor for interface circuits between separated power domains [12].

However, it will be kept off due to the same voltage potential on VSS1 and VSS2 under the normal circuit operation condition. This active second ESD clamp design can achieve high ESD robustness under the cross-power-domain ESD stress [12]. In this paper, one new active ESD protection design for interface circuits between separated power domains was proposed to solve this problem.

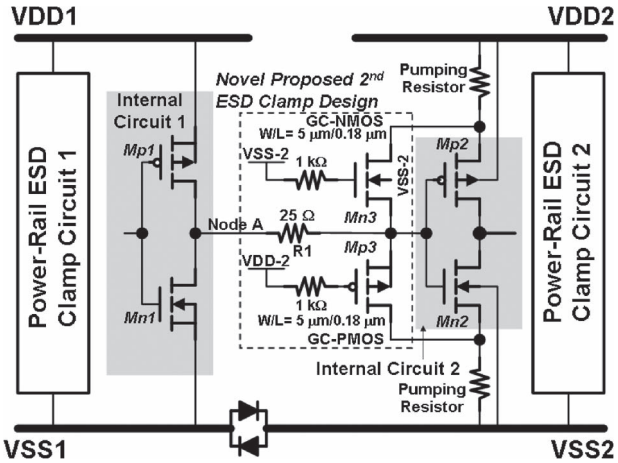

Fig. 13. Proposed cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors and the source pumping mechanism.

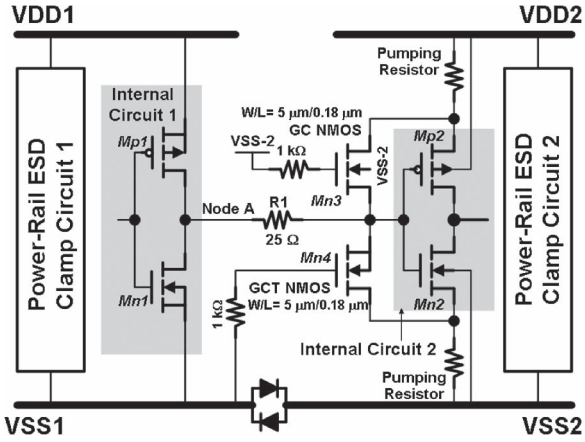

Fig. 14. Cross-power-domain ESD protection design with GCT NMOS and GC-NMOS transistors and the source pumping mechanism.

IV. New Cross-Power-Domain ESD Protection Design

A. Implementation of the New Proposed Design for Cross-Power-Domain ESD Protection

An ESD protection design was implemented by gate-controlled PMOS (GC-PMOS) and gate-controlled NMOS (GC-NMOS) transistors with the ESD-transition detection function for interface circuits between separated power domains, as shown in Fig. 13. The GC-PMOS (Mp3) and the GC-NMOS (Mn3) were placed near the receiver in the interface circuits to clamp overstress voltages across the gate oxides of the receiver's NMOS and PMOS transistors (Mn2 and Mp2), respectively. The gate terminals of GC-PMOS and GC-NMOS transistors were respectively connected to VDD2 and VSS2 through the 1-kΩ resistance. The 1-kΩ resistances are adopted to avoid the gate-oxide damages to GC-PMOS and GC-NMOS transistors during the ESD stresses. During the VDD1-to-VSS2 cross-power-domain ESD stress, the positive ESD voltage was applied at the VDD1 with the grounded VSS2. The gate-to-source voltage (Vgs) of the GC-PMOS transistor (Mp3) was high enough to turn this Mp3 on under VDD2 floating. The voltage potential of node A can be clamped by the turn-on Mp3 to restrict the overstress voltage across the receiver's NMOS transistor (Mn2). When the negative ESD voltage was applied at VDD1 with the grounded VSS2, the forward-biased parasitic diode, which consisted of N-well and P+ drain diffusion in Mp3, would provide excellent ability to clamp the voltage across Mn2. In addition, the GC-NMOS transistor (Mn3) was useful to prevent the ESD damage under the VDD1-to-VDD2 ESD stresses. When the positive ESD voltage was applied at VDD1 with grounded VDD2, the ESD current initially discharged by the desired path, which was the dashed line shown in Fig. 9(a). This ESD discharging current would induce the voltage levels on VDD1, VDD2, VSS1, and VSS2. The induced voltage level of VSS2 was higher than that of VDD2 under the positive VDD1-to-VDD2 ESD stresses. The GC-NMOS transistor (Mn3) could be turned on by the induced voltage levels of VSS2 and VDD2. Then, the voltage level at node A could be restricted to avoid damages to the gate oxide in the interface circuits. The GC-NMOS transistor could also be turned on in the negative ESD stresses since the voltage level at node A would be lower than that of VSS2. On the other hand, the parasitic n-p-n bipolar transistor in Mn3 could be triggered on to restrict the voltages across the gate oxides of Mn2 and Mp2 under the VDD1-to-VDD2 ESD stresses.

According to previous studies, gate oxide breakdown voltages of gate-to-source terminals and gate-to-bulk terminals are quite different in NMOS transistors [17]. The gate oxide breakdown voltage of the gate-to-source terminal is remarkably lower than that of the gate-to-bulk terminal. To enhance the ESD robustness of the input stage with the thin gate oxide in the nanoscale CMOS process and extend the design windows of ESD protection circuits, the source pumping design was used to reduce the ESD voltage across the gate-to-source terminal in the NMOS transistor of the input stage under HBM and CDM ESD stresses [17], [18]. In Fig. 13, a resistor also was inserted between VDD2 (or VSS2) and the source terminal of Mp2 (or Mn2) to comprise the source pumping mechanism. The partial ESD currents could be conducted by turned-on Mp3 and Mn3, and also raised the source-terminal potentials of Mn2 and Mp2 to reduce the voltage across the gate-to-source terminals of Mn2 and Mp2. The source pumping mechanisms can be expected to further enhance the ESD robustness of the receivers in interface circuits under the cross-power-domain ESD stresses.

B. Experimental Results

The cross-power-domain ESD protection design with the GC-PMOS and GC-NMOS transistors was implemented in a 0.13-μm 1.2-V CMOS process. Two other different cross-power-domain ESD protection designs, which were diodes [10] and a GCT NMOS transistor [12], were also compared with the design with the GC-PMOS and GC-NMOS transistors under the same process. The cross-power-domain ESD protection design with diodes was identical with the aforementioned scheme, as shown in Fig. 10. However, the GCT NMOS transistor was only substituted for the GC-PMOS transistor to construct

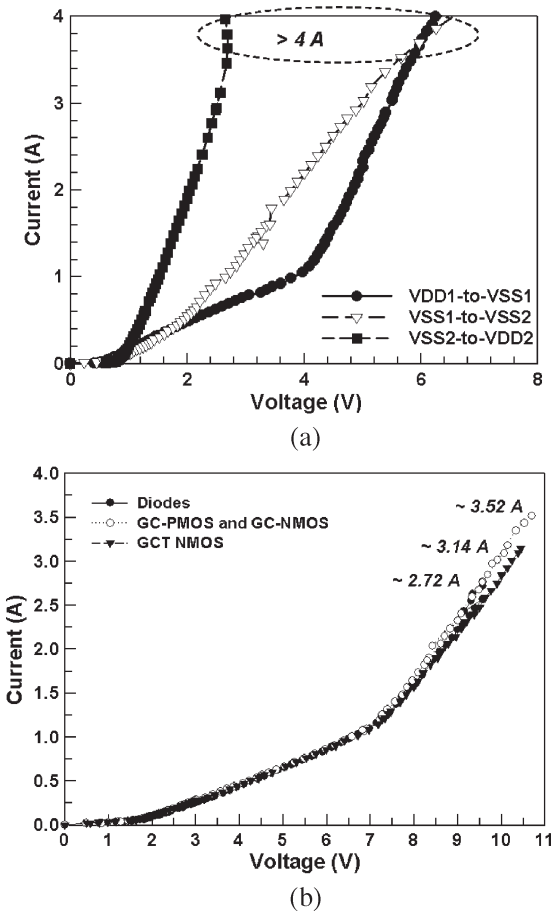

Fig. 15. (a) TLP measured I–V characteristics (100 ns) of the cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors under VDD1-to-VSS1, VSS1-to-VSS2, and VSS2-to-VDD2 three different stress combinations. (b) TLP measured I–V characteristics (100-ns) of the three different cross-power-domain ESD protection designs under VDD1-to-VSS2 stresses.

complete cross-power-domain ESD protection in this paper, as shown in Fig. 14. Both device sizes (W/L) of the GC-PMOS (Mp3) and GC-NMOS (Mn3) transistors are 5/0.18 μm. Then, the value of R1 is 25 Ω. Because the ESD currents were not mainly discharged by Mn3 and Mp3, these transistors did not need to occupy huge device dimensions. The equivalent perimeter of the diodes is 5 μm, and the device size (W/L) of the GCT NMOS transistor is also 5/0.18 μm in this paper. These cross-power-domain ESD protection designs had the identical ESD protection elements of the power-rail ESD clamp circuit in each power domain and the bidirectional diode connection between separated power domains. The I–V characteristics of these three designs were measured by a transmission-line-pulse (TLP) system, which generated the current pulses with 100-ns duration time and 10-ns rise time to be able to obtain the device characteristics under high-current stresses [19].

The TLP I–V characteristics of the cross-power-domain ESD protection design with the GC-PMOS and GC-NMOS transistors under VDD1-to-VSS1, VSS1-to-VSS2, and VSS2-to-VDD2, three different stress combinations, was measured and illustrated as in Fig. 15(a). The symbol of VDD1-to-VSS1 (VSS1-to-VSS2 or VSS2-to-VDD2) means that the TLP current pulse was applied at VDD1 (VSS1 or VSS2) under

TABLE II
HBM AND MM ESD ROBUSTNESS OF THE DIFFERENT CROSS-POWER-DOMAIN ESD PROTECTION DESIGNS UNDER VDD1-TO-VSS2 AND VDD1-TO-VDD2 ESD TESTING CONDITIONS

VDD1 to VSS2			
Designs	**Diodes**	**GCT NMOS**	**GC-PMOS and GC-NMOS**
HBM	3.5 kV	4.5 kV	4.5 kV
MM	450 V	450 V	550 V
VDD1 to VDD2			
Designs	**Diodes**	**GCT NMOS**	**GC-PMOS and GC-NMOS**
HBM	2 kV	3.5 kV	4.5 kV
MM	300 V	350 V	400 V

grounded VSS1 (VSS2 or VDD2). Therefore, the VDD1-to-VSS1 curve presents the TLP I–V characteristic of a power-rail ESD clamp circuit, which consists of an RC-based ESD-transient detection circuit and a main power-rail ESD clamp NMOS transistor between VDD1 and VSS1. Then, VSS1-to-VSS2 is the TLP I–V characteristic of the bidirectional diode connection between VSS1 and VSS2, whereas VSS2-to-VDD2 is the TLP I–V characteristic of the parasitic drain-bulk diode in the power-rail ESD clamp NMOS transistor between VSS2 and VDD2. Moreover, the TLP measured results of all three different cross-power-domain ESD protection designs were shown in Fig. 15(b). Under the VDD1-to-VSS2 stresses, these three different cross-power-domain ESD protection designs presented high second breakdown currents (It2). The cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors had the highest It2 value of about 3.52 A. The HBM and MM ESD robustness of these three designs were presented in Table II under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses. The new proposed ESD design had the highest ESD robustness among all ESD stresses. However, the cross-power-domain ESD protection design with diodes presented unexpected ESD robustness under VDD1-to-VDD2 ESD stresses. The related attributions of the low ESD robustness in the design with diodes would be discussed and explained by failure analysis in Section IV-C.

In addition, the influence of the source pumping mechanism was investigated in cross-power-domain ESD protection designs with the GCT NMOS transistor. The comparisons between the cross-power-domain ESD protection designs with and without a source pumping resistance are shown in Fig. 16(a). The It2 value of the design with a source pumping resistance was significantly higher than that without a source pumping resistance. The It2 values of the designs with and without a source pumping resistance are about 3.14 and 2.26 A under the VDD1-to-VSS2 TLP stresses, respectively. On the other hand, the other TLP measured results, in which

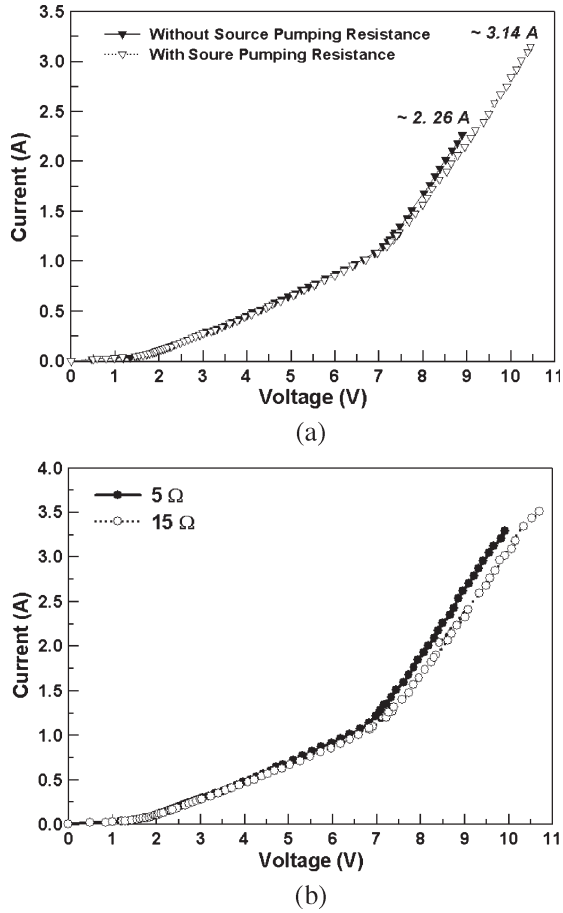

Fig. 16. Influence of the source pumping mechanism on the TLP measured I–V characteristics of the cross-power-domain ESD protection designs under VDD1-to-VSS2 stresses. (a) With or without a source pumping resistance in the design with the GCT NMOS transistor. (b) With a source pumping resistance of 5 or 15 Ω in the design with GC-PMOS and GC-NMOS transistors.

the cross-power-domain ESD protection designs were adopted as GC-PMOS and GC-NMOS transistors, with the different source pumping resistances of 5 and 15 Ω, are also shown in Fig. 16(b). The It2 values were increased by increasing the resistance of the source pumping resistors. According to the measured results, the source pumping resistance can be expected to enhance the ESD robustness for the cross-power-domain ESD protection designs. However, these source pumping resistances would also cause the body effect and affect the circuit performance on the receiver.

C. Failure Analysis and Discussion

The cross-power-domain ESD protection design with diodes presented lower ESD robustness among all ESD testing conditions, as shown in Table II. However, the lower ESD robustness of the ESD protection design with diodes can be attributed to two completely different failure mechanisms under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses, respectively. First, the failure spot of the design with diodes was located at the source side of the driver's PMOS transistor under VDD1-to-VSS2 ESD stresses, as shown in Fig. 17(a) and (b). This failure spot only occurred on the source side of the driver's PMOS transistor. The gate area and drain side of the driver's

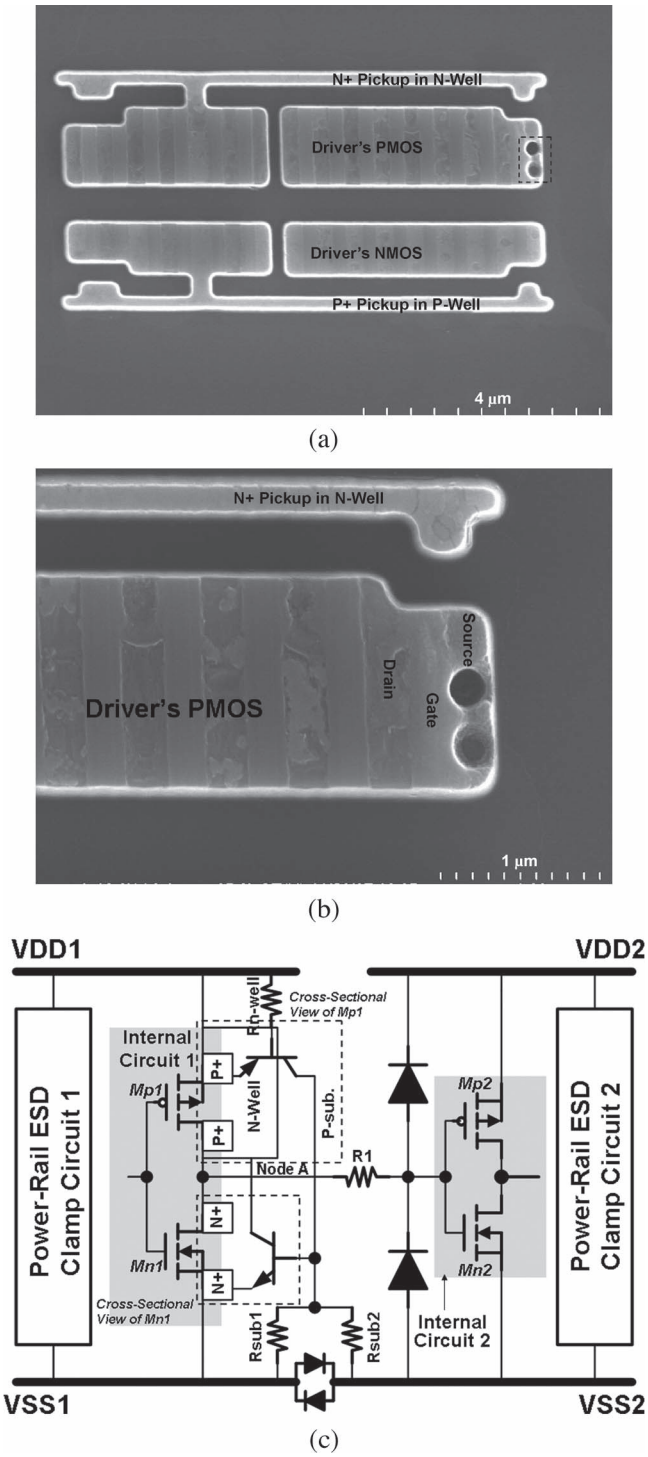

Fig. 17. (a) After the VDD1-to-VSS2 HBM ESD stress, the failure spots of the cross-power-domain ESD protection design with diodes were located at the source side of the driver's PMOS transistor (Mp1). (b) Zoomed-in view of the failure spot. (c) Failure mechanism of the cross-power-domain ESD protection design with diodes under the VDD1-to-VSS2 HBM ESD stress.

PMOS transistor did not need to be destroyed after VDD1-to-VSS2 ESD stresses, as illustrated in Fig. 17(b). The failure mechanism could be explained that the vertical p-n-p bipolar transistor was turned on to cause the serious contact spike on the source side, as shown in Fig. 17(b) and (c). This vertical p-n-p bipolar transistor consisted of the P+ source diffusion

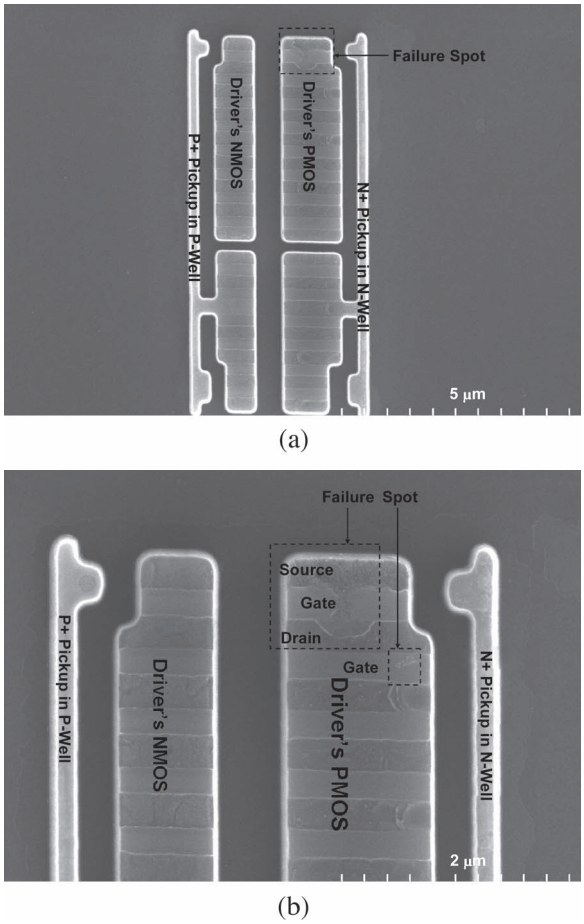

Fig. 18. (a) After the VDD1-to-VSS2 HBM ESD stress, the failure spots of the cross-power-domain ESD protection design with GC-PMOS and GC-NMOS transistors were located at the driver's PMOS transistor (Mp1). (b) Zoomed-in view of the failure spot.

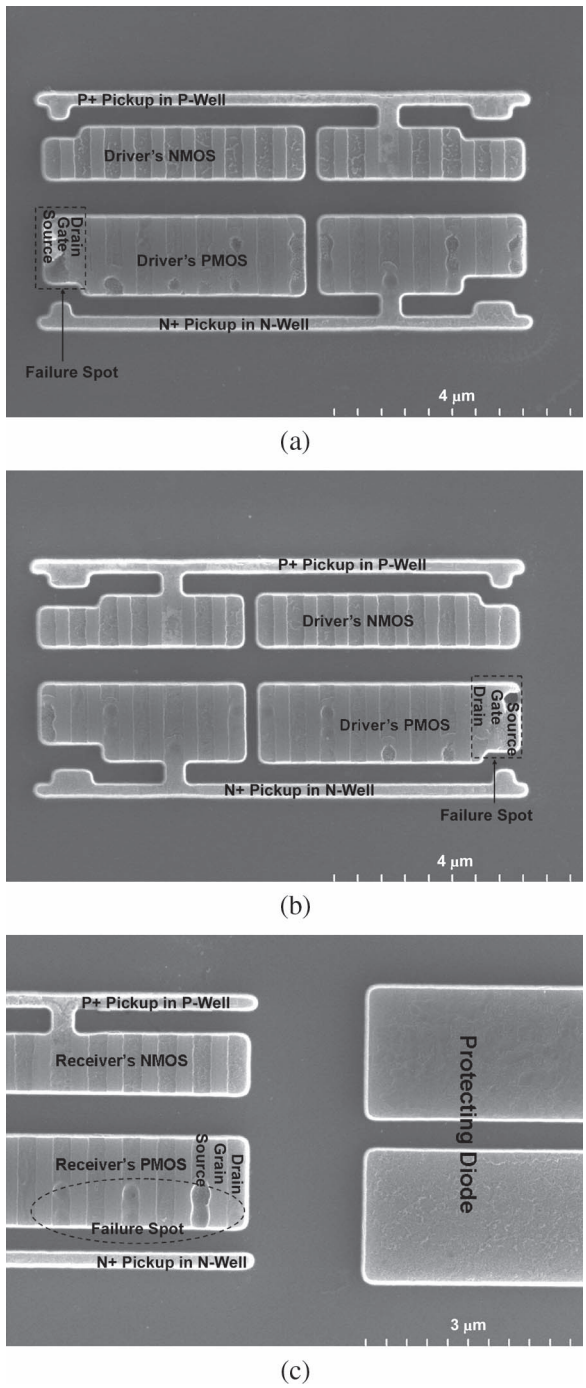

Fig. 19. (a, b) Both cross-power-domain ESD protection designs with diodes and GC-PMOS and GC-NMOS transistors have the failure spots at the driver's PMOS transistor (Mp1) after VDD1-to-VDD2 ESD stresses. (c) Other failure spots of cross-power-domain ESD protection designs with diodes were found at the receiver's PMOS transistor (Mp2) after the VDD1-to-VDD2 MM ESD stress.

of the driver's PMOS, the N-well, and the mutual P-substrate, as shown in Fig. 17(c). Furthermore, this vertical p-n-p bipolar transistor would easily incorporate with a lateral n-p-n bipolar transistor, which consists of the n-well, the p-substrate, and the N+ source diffusion of the driver's NMOS to construct a parasitic SCR path between VDD1 and VSS1, as also illustrated in Fig. 17(c). Because the protecting diode between node A and VSS2 was under the reverse biasing condition, the partial ESD current could not conduct from the driver's PMOS transistor to grounded VSS2. The partial ESD current could be discharged through this SCR path between VDD1 and VSS1 and the diode between VSS1 and VSS2 since no guard ring and pickup were installed between the driver's PMOS and NMOS transistors in such a situation. In contrast, the failure mechanisms of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors were caused by the drain-to-source filaments that were clearly proved in Fig. 18(a) and (b). The partial ESD current conducted from the source side to the drain side in the driver's PMOS transistor to cause the damage to the surface layer on this PMOS transistor under VDD1-to-VSS2 ESD stresses [12].

Second, the failure spot of the ESD protection design with diodes was located at the source and drain sides of the driver's PMOS transistor under the VDD1-to-VDD2 ESD stresses, as shown in Fig. 19(a). This failure spot was similar to those of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors under the VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses, as shown in Figs. 18(b) and 19(b). Since the protecting diode between node A and VDD2 was under the forward biasing condition, the ESD currents could easily conduct from the driver's PMOS transistor to grounded VDD2. This discharging path sustained

a huge ESD current to cause the source-to-drain filament on the driver's PMOS transistor, as presented in Fig. 19(a). Moreover, the failure spot was also found in the receiver's PMOS transistor after VDD1-to-VDD2 ESD stresses, particularly in the MM ESD event, as shown in Fig. 19(c). This failure spot did not occur on the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors. The ESD protection design with diodes conducted a huge ESD current, which caused the damage to the receiver's PMOS transistor under VDD1-to-VDD2 MM ESD stresses. Therefore, the unsuitable current distributions of the cross-power-domain ESD protection design with diodes caused the lower ESD robustness under VDD1-to-VSS2 and VDD1-to-VDD2 ESD stresses. Because these ESD protection designs were mainly focused on the receiver's gate oxide threat, the failure spots did not need to be located on the receiver except that of the ESD protection design with diodes. However, according to the above measured results and failure analyses, the ESD robustness of the cross-power-domain ESD protection designs with GCT NMOS, GC-PMOS, and GC-NMOS transistors seemed to be restricted and dominated by the failure mechanism of the driver's PMOS transistors. The blocking resistance, which is shown in Fig. 8, should be appropriately inserted between the driver's source terminal and VDD1 in order that the ESD robustness of the interface circuits between separated power domains could be further enhanced.

V. Conclusion

Due to circuit performance considerations, the IC product has two separated power domains to cause ESD failures in interface circuits between different power domains. MM ESD currents are discharged through some unexpected paths in the interface circuits during the ND-mode ESD stress. Each failure mechanism of Pin-A and Pin-B has been clearly analyzed and illustrated by the failure spot images and ESD current discharge paths. The effective solutions have been proposed to overcome abnormal internal ESD damage by means of adding the blocking resistors to the interface devices and installing the suitable bidirectional diode connection cells between the separated power lines. The optimum modifications have been proven in the new version of the IC product to sustain the MM ESD level of greater than 200 V. Furthermore, the cross-power-domain ESD protection designs with the resistor-diode clamp, the special driver and receiver, or the GCT NMOS transistor have been reviewed to compare the ESD protection schemes for the interface circuits between separated power domains. Moreover, one new active ESD protection design with GC-PMOS and GC-NMOS transistors has been proposed and successfully verified to sustain 4-kV HBM and 400-V MM ESD stresses in a 0.13-μm 1.2-V CMOS technology. The source pumping mechanism was also proven to significantly enhance the ESD robustness under the cross-power-domain ESD stresses. Finally, the failure mechanisms of three different cross-power-domain ESD protection designs, which were the diodes and the GCT NMOS, GC-PMOS, and GC-NMOS transistors, have been distinctly illustrated according to the related ESD failure locations and discharge paths.

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