A Low-Power High-Speed Class-AB Buffer Amplifier for Flat-Panel-Display Application

Chih-Wen Lu and Chung Len Lee

***Abstract*—A low-power, high-speed, but with a large input dynamic range and output swing class-AB output buffer circuit, which is suitable for the flat-panel display application, is proposed. The circuit employs an elegant comparator to sense the transients of the input to turn on charging/discharging transistors, thus draws little current during static, but has an improved driving capability during transients. It is demonstrated in a 0.6 μm CMOS technology.**

***Index Terms*—Amplifiers, Buffer circuits, driver circuits, flat panel displays.**

I. Introduction

With the evolution of compact, light-weighted, low-power, and high-quality display, there is a big demand of developing the low-power consuming, high efficiency, and high-speed buffer circuit. The circuit should occupy a small die area, consume minimal power, have a settling time smaller than the horizontal scanning time, and a capability of offering high-current resolution which can accommodate up to 256 gray levels. For a 4 V of full scale, each gray level corresponds to 16 mV [1], [2].

Some output buffers were proposed and demonstrated in recent years. For examples, Yu *et al.* [3] proposed a class-B output buffer for flat-panel-display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage; Lee *et al.* [4] proposed a dynamic-bias technique, to increase the bias current of the differential input stage of a two-stage amplifier when the input voltage difference is large; and Khorramabadi [5] also proposed a class-B amplifier which had a better power efficiency but with a large-output transistor.

In this work, a class-AB CMOS output buffer circuit is proposed. The circuit achieves the large driving capability by employing a simple but elegant comparator circuit to sense the transients of the input to turn on charging/discharging transistors, which are statically **"off"** when no input is applied. This increases the speed of the circuit without increasing too much static-power consumption. The circuit also features a wide input voltage range and a large output swing.

II. The Proposed Class-AB Buffer

Fig. 1 shows the proposed class-AB buffer circuit. As a buffer, the output is connected to the inverting input (**in**$-$) and the input signal is applied to the noninverting terminal (**in**$+$). The differential pair M5–M6, which is biased by the constant current source M1–M4, is actively loaded by the current mirror formed by M7 and M8. M9 and M10 form a common-source output stage and the Miller-feedback R-C is for frequency compensation. When the M9–M10 output stage is to drive a large capacitive load of a flat-panel display under a step-wise input, it will have a small fall time but a large rising time since M9 is a constant current which provides limited charging capability to the load. To solve this problem, M11–M12, which forms a current comparator and a charging transistor M13 are added. The W/L of M12 is chosen the same as those of M7 and M8 to draw the same magnitude of current, $I/2$, where I is the biasing current of the input differential stage, as M7 and M8. However, the W/L of M11 is chosen to be a little bit larger than half of M4

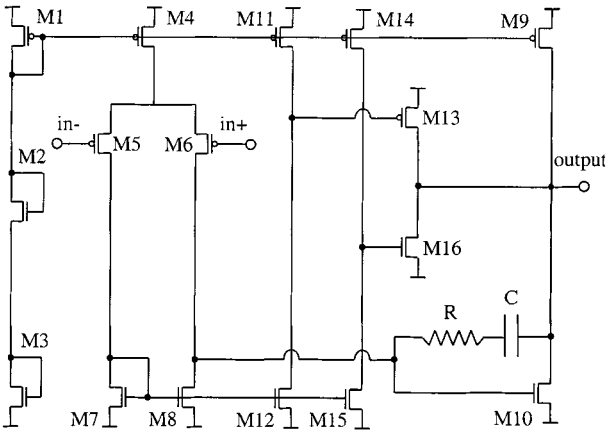

Fig. 1. The proposed class-AB buffer amplifier.

$$\left(\frac{W}{L}\right)_{11} = \frac{1}{2}\left(\frac{W}{L}\right)_{4} + \Delta\left(\frac{W}{L}\right). \tag{1}$$

In the stable state with no input, the output voltage equals to the input voltage. The currents flowing in M5, M6, M7, M8, and M12 are all $I/2$. At this moment, the current flowing in M11 is also $I/2$. However, since the aspect ratio of M11 is designed to be greater than half of M4, this will make M11 go out of the saturation region and be in the triode region. As a result, the gate voltage of M13 will be forced to be close to the value of V_{DD}. M13 will then stay at **"off."** That is, when no input is applied, M13 is cut off from the output. When there is an input, i.e., the input voltage of the noninverting terminal is raised, say, by a step voltage ΔV_1, the current in M5 will be increased to $(I/2) + (1/2)g_m\Delta V_1$ but the current in M6 will be decreased to $(I/2) - (1/2)g_m\Delta V_1$, where g_m is the transconductance of M5 and M6. That is

$$i_{D5} = \frac{I}{2} + \frac{1}{2}\, g_m \Delta V_1 \tag{2}$$

$$i_{D6} = \frac{I}{2} - \frac{1}{2}\, g_m \Delta V_1 \tag{3}$$

where

$$g_m = \sqrt{I\left(\frac{W}{L}\right)_5 \mu_p C_{ox}}. \tag{4}$$

μ_p and C_{ox} are the hole mobility in the p channel and the gate oxide capacitance per unit area, respectively. If i_{D5} is greater than $I/2 + \Delta I$

$$\Delta V_1 > 2\Delta I/g_m \tag{5}$$

where

$$\Delta I = \frac{1}{2}\,\mu_p C_{\rm OX}\Delta\left(\frac{W}{L}\right)(V_{SG11} - V_{tp})^2 \tag{6}$$

transistor M11 will go into the saturation region and its drain voltage, i.e., the gate voltage of M13 will decrease to turn on M13. M13 starts to charge the output node. The larger ΔV_1 is, the more M13 is turned on. Since V_{SG13} can reach a value of V_{DD}, the gate voltage of M13

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C.-W. Lu is with the Department of Electrical Engineering, National Chi-Nan University (e-mail: cwlu@ncnu.edu.tw).

C. L. Lee is with the Department of Electronics Engineering, National Chiao Tung University (e-mail: cllee@cc.nctu.edu.tw).

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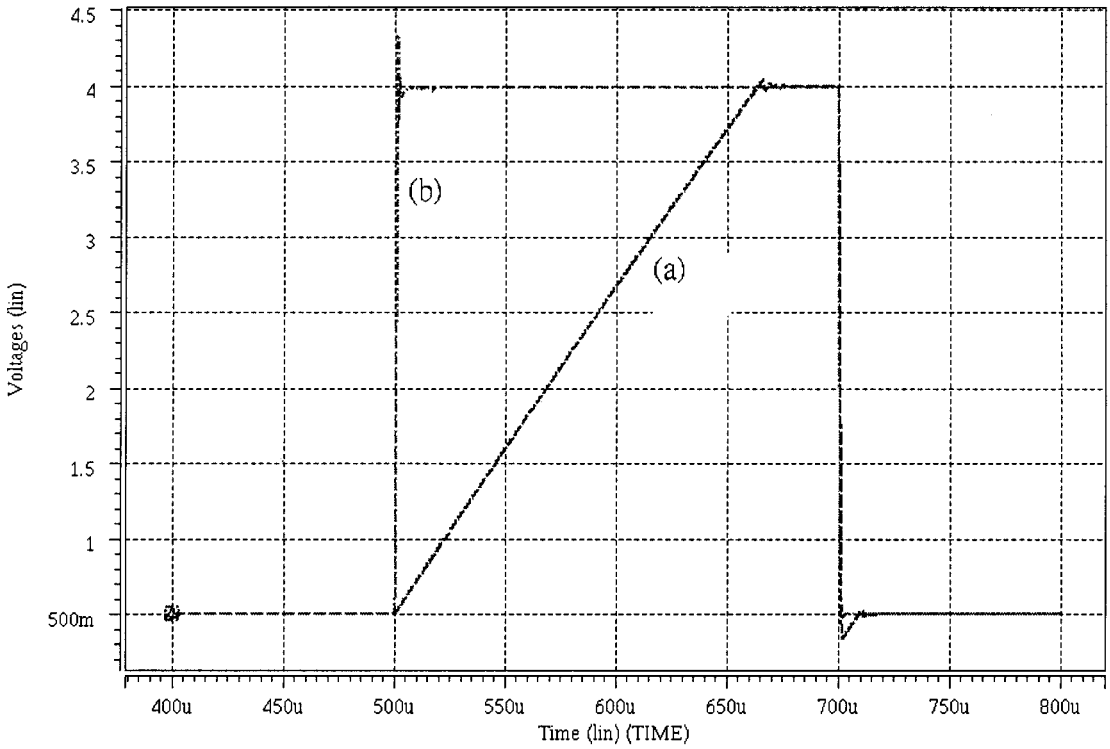

Fig. 2. The simulated responses of the outputs of the conventional amplifier and the proposed buffer amplifier, which are loaded with a large-size capacitor of 680 pF, with a square-wave input.

can be decreased to a really low and M13 can be turned to fully **"on"** to charge the output by a maximal speed. When the output voltage reaches the level that the voltage difference between the input and output is less than $2\Delta I/g_m$, M13 stops charging the output node. In this way, in addition to the original constant current source M9, the charging capability of this circuit is greatly improved for the rising edge of the input waveform.

If the buffer is to be used to drive a larger capacitive load, the driving capability can be improved by increasing the size of M13, M9, and M10. Increasing the aspect ratio of M13 does not increase the static current; however, increasing the sizes of M9 and M10 does increase the static current. That will increase the total power consumption. Hence, another comparator transistors M14–M15 and a discharge transistor M16 are added to improve the discharge capability without increasing the static current. M14–M16, which work in a similar way as do M11–M13, are to improve the discharging capability of the circuit when the input of the circuit is applied a negatively going input waveform. When the negatively going input waveform is larger than $2\Delta I/g_m$, M16, which originally stays **"off,"** is turned **"on"** to help discharge the load voltage. Since M13 and M16 are **"off"** when no input is applied, they draw no static current, thus do not consume static power. Hence, this configuration is a low power consumption but high-speed buffer.

Fig. 2 shows the simulated responses of the outputs of the conventional amplifier and the proposed buffer amplifier, which are loaded with a large size capacitor of 680 pF, with the input of a step-wise (0.5∼4 V). Curve (a) is the response of the conventional buffer and the curve (b) is for the proposed buffer. The settling times to settle to within 0.2% of the final voltage for the rising edges, are 175 and 1.5 μs for the outputs of these two buffer amplifiers, respectively. It can be seen that the charging capability is greatly improved for the rising edge of the input waveform.

III. Evaluation of Power Consumption

There are three components in the power dissipated in the amplifier. The static dissipation, which is due to the dc bias current from the power supply for each transistor; the dynamic dissipation due to the charging and discharging of the load capacitance; and the direct-path dissipation, which is due to the direct-path current going through both the pMOS and nMOS transistors during transitions.

For this circuit, the static energy dissipation during a scanning period can be expressed as

$$E_{\text{static}} = \frac{I_{\text{bias}} V_{DD}}{f_{\text{scanning}}} \tag{7}$$

where I_{bias} is the total dc bias currents for the whole circuit and f_{scanning} is the scanning frequency. The amplifier always consumes this static dissipation.

For the dynamic dissipation, during transitions, as the load capacitance is charged, charges are transferred from V_{DD} through the output pMOS transistor to the load. Power dissipation in this pMOS transistor is given by

$$\begin{aligned} P_{\text{charge}} &= (V_{DD} - V_0)\, i_L \\ &= (V_{DD} - V_0)\, C_L \frac{dV_0}{dt}. \end{aligned} \tag{8}$$

The energy dissipated in this pMOS device as the output charges from V_L to V_H is

$$\begin{aligned} E_{\text{charge}} &= \int_{V_L}^{V_H} P_{\text{charge}}\, dt \\ &= C_L V_{DD}(V_H - V_L) - \tfrac{1}{2} C_L \left(V_H^2 - V_L^2\right). \end{aligned} \tag{9}$$

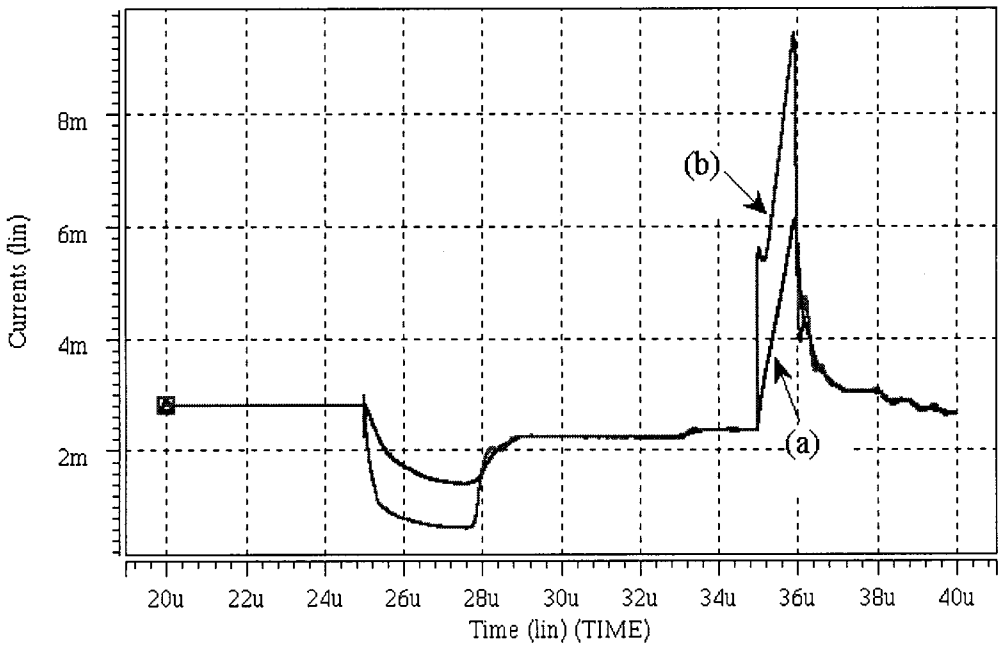

Fig. 3. The simulated results of the power supply currents for the conventional amplifier. Curve (a) is the current drawn from V_{DD} and curve (b) is the current drawn from V_{SS}.

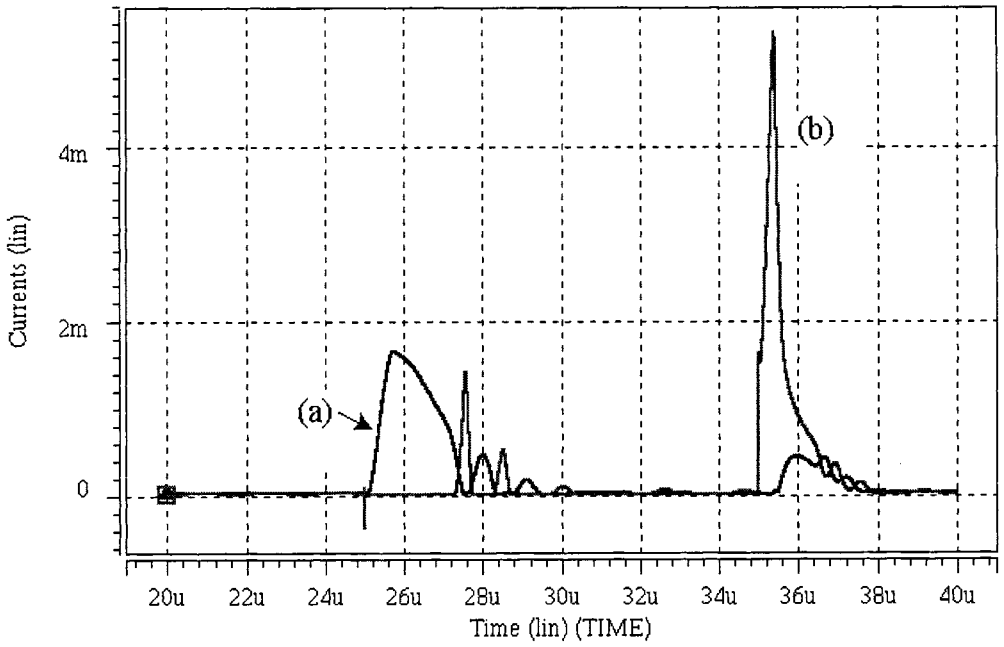

Fig. 4. The simulated results of the power supply currents for the proposed buffer amplifier. Curve (a) is the current drawn from V_{DD} and curve (b) is the current drawn from V_{SS}.

As the output discharges to a lower value, the power is dissipated in the output nMOS transistor. This power dissipation is

$$P_{discharge} = -V_0 i_L = -V_0 C_L \frac{dV_0}{dt}. \tag{10}$$

The energy dissipated as the output discharges from V_H to V_L is given by

$$E_{\text{discharge}} = \int_{V_L}^{V_H} P_{\text{discharge}}\, dt = \tfrac{1}{2} C_L \left(V_H^2 - V_L^2\right). \tag{11}$$

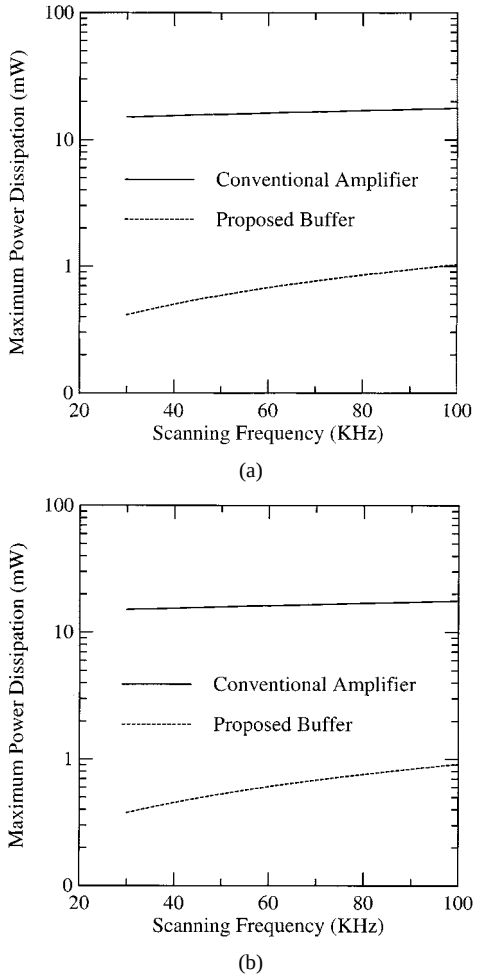

Fig. 5. (a) The maximum power consumption versus the scanning frequencies for a 3.5-V output voltage swing (0.5∼4 V) for the charging step of the conventional and proposed buffer. (b) The maximum power consumption versus the scanning frequency for a 3.5-V output voltage swing (0.5∼4 V) for the discharging step of the conventional and proposed buffer.

For the direct-path current power dissipation, it can be estimated by computing the area under the direct-path current plot which can be approximated by a triangular value. The dissipated energy is then given by

$$E_{dp} = \tfrac{1}{2} V_{DD} I_{\text{peak}} T_{dp} \tag{12}$$

where I_{peak} is the peak value of the direct-path current and T_{dp} is the duration of this current.

The total energy dissipated in the amplifier as the output charges from V_L to V_H during one scanning period is therefore

$$E_{\text{tot, charge}} = \frac{I_{\text{bias}} V_{DD}}{f_{\text{scanning}}} + C_L V_{DD} (V_H - V_L) - \tfrac{1}{2} C_L \left(V_H^2 - V_L^2\right) + \tfrac{1}{2} V_{DD} I_{\text{peak}} T_{dp}. \tag{13}$$

When the output discharges, the total dissipated energy during one scanning period is

$$E_{\text{tot, discharge}} = \frac{I_{\text{bias}} V_{DD}}{f_{\text{scanning}}} + \tfrac{1}{2} C_L \left(V_H^2 - V_L^2\right) + \tfrac{1}{2} V_{DD} I_{peak} T_{dp}. \tag{14}$$

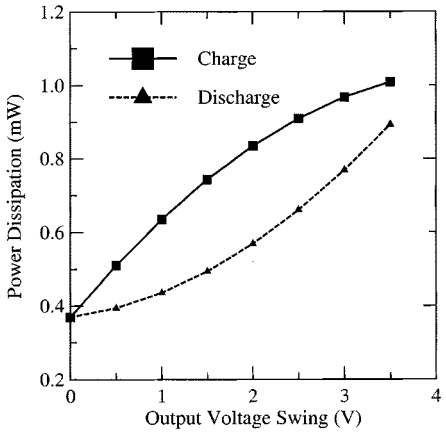

Fig. 6. The power consumption versus the output-voltage swing for a 97.8 KHz scanning frequency for the proposed buffer amplifier. The solid line is the power dissipation as the output voltage is charged from 0.5 V while the dash line is the one discharged to 0.5 V.

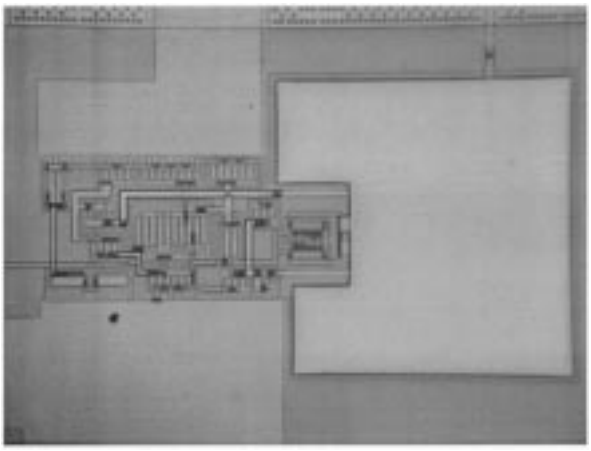

Fig. 7. The die photograph of the proposed output buffer.

The total average power dissipated in one buffer amplifier during one scanning period is

$$P_{\text{tot}} = f_{\text{scanning}} E_{\text{tot}}. \tag{15}$$

For a conventional amplifier circuit, for which only M1–M10 exist, the dc bias for M9 should be much large, as compared to our proposed circuit, in order to achieve the same driving. This greatly increases the static-power consumption. Fig. 3 shows the simulated results of the power-supply currents for the conventional amplifier, which is loaded with a large-size capacitor of 680 pF with a step-wise input of 0.5 V∼4 V. Curve (a) is the current supplied from V_{DD} and curve (b) is the current drawn from V_{SS}. There is a static current of 2.8 mA. Due to the voltage feed-through through the parasitic capacitance between the gate and drain of M4, the gate voltage of M9 will be raised up during the rising edge and pulled down during the falling edge of the input signal. Hence, the current is reduced during the rising edge and is increased during the falling edge of the input signal. This produces a direct-path current. In the figure, the peak value is 6.1 mA, the duration of the direct-path current is 2 μs, and the maximum transient current is 9.45 mA. Hence, the static power consumption is 14 mW and the maximum dynamic power consumption is 47.25 mW.

However, for our proposed amplifier circuit, it has an improved driving capability during transients but draws little static current. Fig. 4 shows the same simulation results of the proposed class-AB

buffer amplifier with the same input condition as that of Fig. 3. Curve (a) is the current supplied from V_{DD} and curve (b) is the current drawn from V_{SS}. The maximum transient current is 5.3 mA. However, the static current is only 29.8 μA. The maximum dynamic power consumption is 26.5 mW while the static power is only 149 μW, which are much smaller than those of the previous conventional amplifier circuit. For the direct-path currents, there exist only small ringings during transients and the maximum peak value is 0.45 mA.

The dynamic power consumption depends on the value of the output voltage swing. The maximum value occurs when the image on a column of the display is alternating black-and-white and pixel by pixel. However, when the image on a column is a constant gray level, the dynamic power is zero. The horizontal scanning frequency ranges from 31.5 to 97.8 KHz [3]. The power dissipation of the buffer can be estimated from equations (13)–(15) for a scanning period. Fig. 5(a) and (b) show the maximum-power consumption versus the scanning frequency with a 3.5 V output voltage swing (0.5∼4 V) for the charging and discharging steps, respectively, for the proposed buffer amplifier and the conventional amplifier. It can be seen that the power consumption of the proposed buffer amplifier depends on the scanning frequency. However, they are greatly reduced as compared with that of the conventional type of amplifier even for the scanning frequency up to 100 KHz. Fig. 6 shows the power consumption versus the output voltage swing for a 97.8 KHz scanning frequency for the proposed buffer. The solid line is the power dissipation as the output voltage is charged from 0.5 V while the dash line is the one discharged to 0.5 V. It can be seen that the power dissipation depends on the output voltage swing.

IV. Experimental Results

The proposed output buffer amplifier was fabricated using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.6-μm CMOS technology. The die photograph of the output buffer is shown in Fig. 7. Fig. 8 shows the measured results of the output with the input of a large dynamic range (1∼4.17 V) of a 100 KHz triangular wave of the proposed buffer amplifier loaded with a large size capacitor of 680 pF (not including parasitic capacitances of the pad and the test circuit). The lower trace is the input waveform and the upper one is the measured-output waveform. It can be seen that the output basically follows the input. The step response of the same buffer with a 100 KHz square wave is shown in Fig. 9, where traces (a) and (b) are the curves of the input and output, respectively. The input voltage range is 0.15–4 V. The settling times for the outputs to settle to within 0.2% of the final voltage are 1.6 and 1 μs for the rising and falling edges, respectively. These values are low as compared with those of [3]. In order to show the small-signal performance of the amplifier, Fig. 10 is the small-signal step response of an amplitude of 20 mV step waveform of the amplifier. The output waveform follows exactly as the input waveform with a small offset voltage of 6 mV. The total static current is 30 μA.

V. Conclusion

In this paper, we have proposed and demonstrated a low-power consumption, high speed, large output swing, and wide-input-voltage range, class-AB output buffer circuit which is very suitable for driving the large column line capacitance in the flat-panel display. The driving capabilities of the circuit are achieved by adding comparators which sense the rising and falling edges of the input waveform and then turn on an auxiliary driving transistor to help charging/discharging the output load. The auxiliary driving transistors stay at **"off"** when there is no input applied, thus drawing no static power. The theoretical

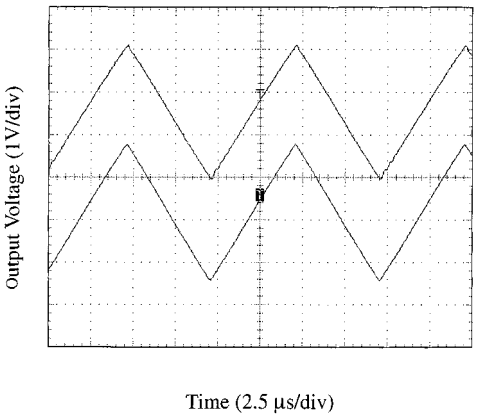

Fig. 8. The measured result of the proposed output buffer under a 100 KHz triangular input waveform of an amplitude of 1 V to 4.17 V under a 680 pF capacitance load. The lower trace is the input waveform.

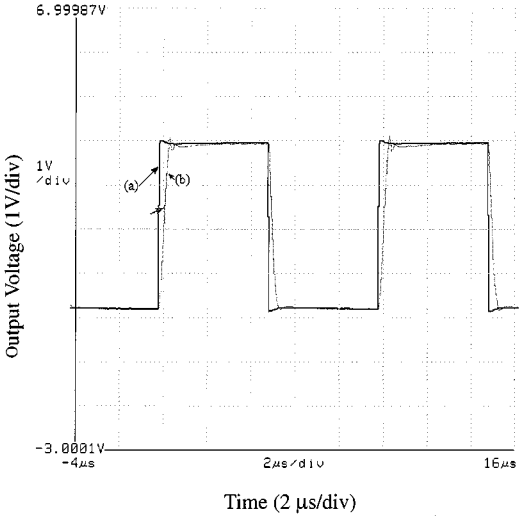

Fig. 9. The output-step response of the proposed output buffer with a 100-KHz square wave input under a 680 pF capacitance load. Traces (a) and (b) are the input and output waveforms, respectively.

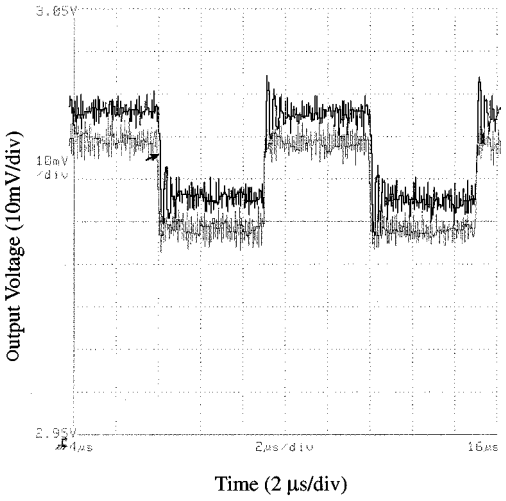

Fig. 10. The small signal-step response of the proposed output buffer. The amplitude of the step input is 20 mV. The lower trace is the input waveform.

power dissipations of the proposed class-AB buffer amplifier, which is loaded with a large-size capacitor of 680 pF with the input of a step-wise (0.5∼4 V) for a 97.8 KHz scanning frequency, are only 1 and 0.893 mW for charging and discharging, respectively. Experimental prototype output buffer implemented in the TSMC 0.6-μm CMOS technology had demonstrated that the circuit draws only 30 μA static current and exhibited settling times of 1.6 μs and 1 μs for rise and fall edges for the proposed circuit under a 680 pF capacitance load. The settling time for the rise edge is improved from 175 μs of the conventional buffer amplifier to 1.6 μs of the proposed buffer. The input swing is 3.85 V. The measured data do show that the proposed output buffer circuit is very suitable for the application in the flat panel as the display driver.

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On the Design of Low-Voltage, Low-Power CMOS Analog Multipliers for RF Applications

Carl James Debono, Franco Maloberti, and Joseph Micallef

***Abstract*—Novel low-voltage, low-power techniques in the design of portable wireless communication systems are required. Two system examples of low-power analog multipliers operating from a 1.2 V supply are presented. These proposed structures achieve the required multiplication function by using current processing. The circuits were fabricated using standard double-poly CMOS processes for a 900 MHz application. Measurement results of the prototypes are comparable to other higher voltage designs.**

***Index Terms*—Analog multiplier, CMOS RF, low power, low voltage.**

I. INTRODUCTION

Continuous growth in the demand for portable wireless systems has driven recent efforts to increase integration levels in RF transceivers [1]. The integrability and power consumption of the digital part of a communications transceiver will further improve with the downscaling of technologies. The bottleneck for further advancements is the analog front-end electronics [2]. In order to reduce the power consumption, architectures that require smaller currents must be developed. One approach is to use structures that function at a lower supply voltage.

Operation at 1.2 V is difficult to achieve with bipolar technologies since the base-to-emitter voltage is 0.7 V and the base-to-collector junction must be reverse biased. By contrast the MOS transistor allows the drain-to-source voltage to be lower than the gate-to-source voltage. Therefore, if the saturation voltage is kept at a few hundred millivolts there is enough room for some output dynamic range. This implies that low-voltage, low-power analog structures can be developed using CMOS technology.

The downconversion mixer is one of the indispensable analog blocks in a receiver, where its main function is that of frequency translation of the incoming RF signal to an intermediate frequency for further processing. Various authors have tackled the problem of designing low-voltage CMOS RF mixer architectures that permit satisfactory operation at frequencies higher that 900 MHz [3]–[11]. Mixers based on the Gilbert cell topology [3]–[6] all require stacking of a current source, the RF input pair, the local oscillator quad and the output loads, thus limiting the minimum supply voltage required by the circuit. The mixer proposed in [7] also requires a high bias voltage due to the stacking of transistors. The passive mixers proposed in [8], [9] have a better linearity than active mixer designs but require a high supply voltage required for the digital part in [8] and for the stacking in the opamp in [9]. The passive mixer proposed in [10] operates at a lower voltage than [8], [9] but it still uses transistor stacking limiting the minimum supply voltage. A different approach that requires only ground-connected transistors operating in saturation for the mixer core was taken in [11]. The minimum supply voltage of this approach is limited by the output buffer.

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C. J. Debono is with the Department of Electronics, University of Pavia, 27100 Pavia, Italy and also with the Department of Microelectronics, University of Malta, Msida MSD06, Malta (e-mail: carl@ele.unipv.it; cjdebo@eng.um.edu.mt).

F. Maloberti is with the Department of Electronics, University of Pavia, 27100 Pavia, Italy (e-mail: franco@ele.unipv.it).

J. Micallef is with the Department of Microelectronics, University of Malta, Msida MSD06, Malta (e-mail: jjmica@eng.um.edu.mt).

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