Characterization of the Novel Polysilicon TFT With a Subgate Coupling Structure

Kow Ming Chang, *Member, IEEE*, Yuan Hung Chung, Chi-Gun Deng, Yuan Fu Chung, and Jian-Hong Lin

***Abstract*—We have proposed and fabricated a novel polysilicon thin film transistor (poly-Si TFT) with a subgate coupling structure that behaves as an offset gated structure in the OFF state while acting as a conventional nonoffset structure in the ON state. The OFF state leakage current of the new TFT is two orders of magnitude lower than that of the conventional nonoffset TFT, while the ON current of the new TFT is one order of magnitude higher than that of the offset TFT and is almost identical to that of the conventional non-offset TFT. The ON/OFF current ratio of the new TFT is greatly improved by two orders of magnitude. No additional photo-masking steps are required to fabricate the subgate of the new TFT and its fabrication process is fully the same as the conventional nonoffset TFTs.**

***Index Terms*—Polysilicon thin film transistor (poly-Si TFT), offset gated structure, ON/OFF current ratio, photomasking steps, subgate coupling structure.**

I. Introduction

POLYSILICON thin-film transistors (poly-Si TFTs) have received increasing interest in the applications of active matrix liquid crystal displays (AMLCDs) and static random-access memories (SRAMs) due to their high mobility [1]. However, a large OFF state leakage current is one of the many problems for poly-Si TFTs. It has been reported that a dominant leakage current mechanism is the field emission via grain boundary traps by a high electric field near the drain [2]. Several structures have been proposed to suppress the leakage current by reducing the drain electric field such as the offset gated structures (offset TFTs) [3]–[6], the lightly doped drain structures (LDD TFTs) [7], and the field induced drain structures (FID TFTs) [8]. But additional photomasking steps and ion-implantation steps are required in most of the above structures. The offset region of the offset TFT, the LDD region of the LDD TFT, and the FID region of the FID TFT will introduce an extra series resistance to decrease the TFT ON current [9]. Moreover, process damage would be caused by the additional ion-implantation in the LDD region which can be attributed to reason that the implanted damage can not be fully annealed out in the low temperature process (<600) °C of the poly-Si TFT. The misalignment problem would also occur with an additional phto-masking step to form the offset region in the offset TFT and the FID region in the FID TFT. It is desirable to have a TFT which would behave as an offset gated TFT in the OFF state, while acting as a conventional nonoffset TFT in the ON state [10].

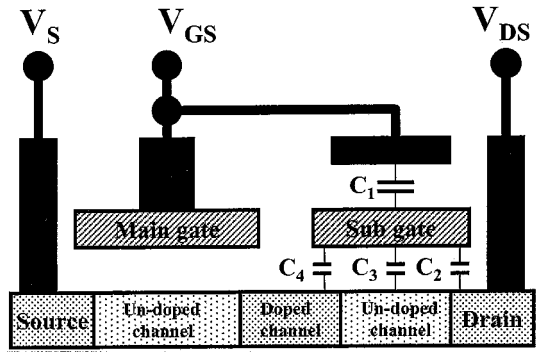
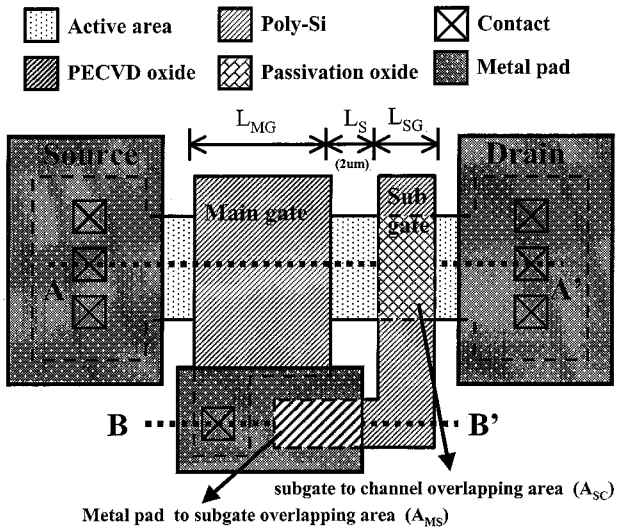
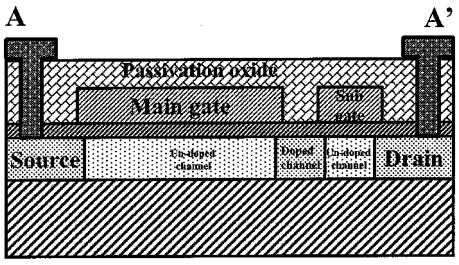


Fig. 1. Schematic diagram of the new TFT.



(a)



(b)

Fig. 2. (a) Top view of the new TFT, (b) cross-section view along the AA', and (c) cross-section view along the line BB'.

Manuscript received September 4, 2001; revised November 26, 2001. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC89-2215-E009-089. The review of this paper was arranged by Editor J. Vasi.

K. M. Chang, Y. H. Chung, C. G. Deng, Y. F. Chung, and J. H. Lin are with the Department of Electronic Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: kmchang@cc.nctu.edu.tw).

Publisher Item Identifier S 0018-9383(02)02118-4.

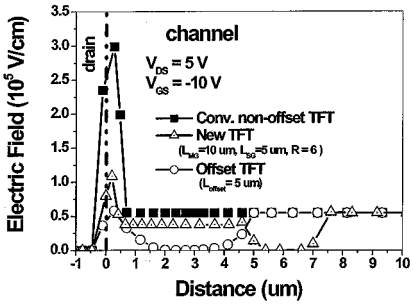


Fig. 3. OFF state electric along the channel at $V_{\rm DS} = 5$ V and $V_{\rm GS} = -10$ V for the conventional nonoffset TFT, the new TFT, and the offset TFT.

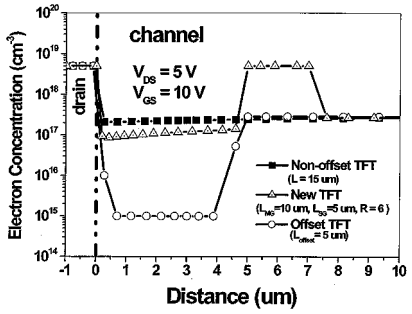


Fig. 4. ON state electron concentration along the channel at $V_{\rm DS} = 5$ V and $V_{\rm GS} = 10$ V for the conventional nonoffset TFT, the new TFT, and the offset TFT.

In this work, we propose a novel poly-Si TFT with a subgate coupling structure to reduce the OFF state leakage current without degrading the ON current. The OFF state leakage current of the new TFT shows two orders of magnitude lower than that of the conventional nonoffset TFT, so that the ON/OFF current ratio is significantly improved. Moreover, the fabrication processes of the new poly-Si TFT are fully identical with those of the conventional nonoffset poly-Si TFT.

II. Experiment

A. Device Structure

Fig. 1 shows the schematic diagram of the new poly-Si TFT. The subgate is floating and its potential is controlled by the main gate potential $V_{\rm GS}$, drain potential $V_{\rm DS}$, undoped channel potential $V_{\rm UC}$, and doped channel potential $V_{\rm DC}$. The subgate potential $V_{\rm SG}$ can be expressed as

$$V_{\rm SG} = \frac{1}{C_T}(C_1 \cdot V_{\rm GS} + C_2 \cdot V_{\rm DS} + C_3 \cdot V_{\rm UC} + C_4 \cdot V_{\rm DC})$$

where $C_T = C_1 + C_2 + C_3 + C_4$. C_1, C_2, C_3, and C_4 are the capacitances between the subgate and the main gate, drain region, undopoed channel, and doped channel, respectively. Fig. 2(a) shows the top view of the new poly-Si TFT. Figs. 2(b) and (c) show the cross-section views along the lines AA' and BB' of Fig. 2(a), respectively. The parameter R is defined as the area ratio of $A_{\rm MS}/A_{\rm SC}$ where $A_{\rm MS}$ is overlapping area between the metal pad and the subgate and $A_{\rm SC}$ is overlapping area between the subgate and the channel. The process sequences of the new poly-Si TFT are the same as the conventional nonoffset poly-Si TFT.

In the OFF state, the main gate has a negative potential ($V_{\rm GS} < 0$), and the drain potential is positive ($V_{\rm DS} > 0$). Therefore, the subgate potential determined by the previous equation is smaller than the main gate potential. The drain electric field can be reduced as compared to the conventional nonoffset TFT, so that the new poly-Si TFT can acts as the offset poly-Si TFT in the OFF state if the area ratio R is properly adjusted.

In the ON state, both the main gate potential and the drain potential are positive ($V_{\rm GS} > 0, V_{\rm DS} > 0$). The subgate potential is almost equivalent to the main gate potential at high $V_{\rm GS}$ and $V_{\rm DS}$, so that the new poly-Si TFT behaves as the conventional nonoffset TFT in the ON state.

B. Device Fabrication

The main process sequences of the new poly-Si TFT are as follows. First, an undoped 1000 Å-thick amorphous silicon (α-Si) films are deposited on the 5000 Å-thick thermal oxide by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then the α-Si film is crystallized to become the polycrystalline silicon film at 600 °C for 24 h. After the active channel region has been defined, 480 Å-thick gate oxide and 3000 Å-thick amorphous silicon gate are deposited and patterned. p^+ ion implantation (5×10^{15} cm^{-2}, 50 KeV) is used to form the source/drain regions for N-channel TFT. The 3000 Å-thick passivation oxide is deposited and the dopant activation is performed at 600 °C for 24 h. Then a contact etch and an aluminum pad formation are carried out. The aluminum pads are sintering in N_2 gas at 400 °C for 30 min. The conventional nonoffset TFT is fabricated alongside of the new TFT. The offset gated TFT is also fabricated with an additional offset mask. Finally, NH_3 plasma treatment is performed on all samples for 1 h at 350 °C.

III. Results and Discussion

A. Device Simulation

The two-dimensional (2-D) simulation of the new poly-Si TFT is carried out by MEDICI. Fig. 3 shows the simulated electric field along the channel from the drain in the OFF state ($V_{\rm DS} = 5$ V, $V_{\rm GS} = -10$ V). It is observed that the maximum electric field of the new TFT is much smaller than that of the conventional nonoffset TFT and only slightly higher than that of the offset TFT. Therefore, it is expected that the OFF state leakage current of the new TFT is much lower than that of the conventional nonoffset TFT and is comparable to that of the offset TFT. Fig. 4 shows the electron concentration along the channel from the drain in the ON state ($V_{\rm DS} = 5$ V, $V_{\rm GS} = 10$ V). The electron concentration of the new TFT shows two orders of magnitude higher than that of the offset TFT and is comparable to that of the conventional nonoffset TFT. This implies that the ON current of the new TFT should be much higher than that of the offset TFT and almost identical with that of the conventional nonoffset TFT.

B. I-V Measurement

The $I_{\rm DS}$-$V_{\rm GS}$ characteristics for the new TFT, the conventional nonoffset TFT, and the offset TFT are compared in Fig. 5.

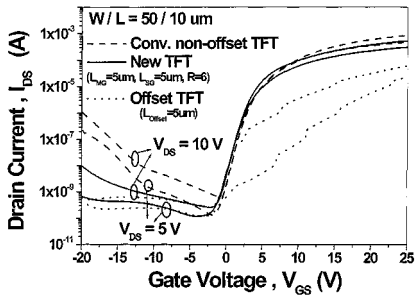


Fig. 5. $I_{\rm DS}$–$V_{\rm GS}$ characteristics for the conventional nonoffset TFT, the new TFT, and the offset TFT.

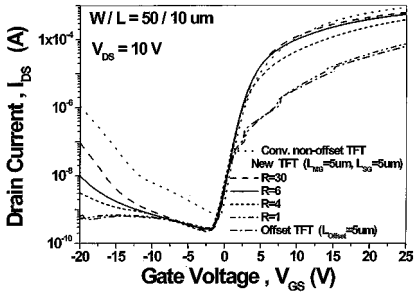


Fig. 6. $I_{\rm DS}$–$V_{\rm GS}$ characteristics for the conventional nonoffset TFT, the new TFT with various area ratio R, and the offset TFT.

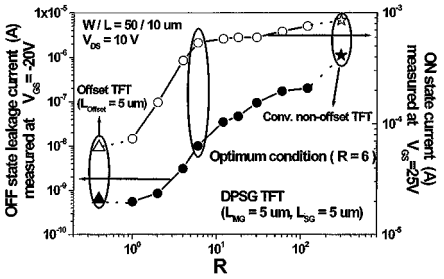


Fig. 7. OFF state leakage current and the ON state current for the conventional nonoffset TFT, the new TFT with various area ratio R, and the offset TFT.

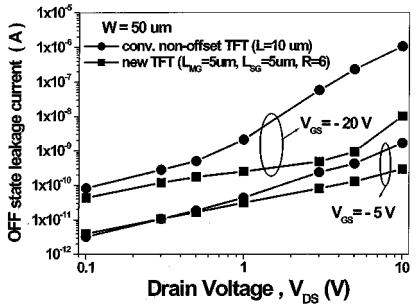


Fig. 8. OFF state leakage current for the conventional nonoffset TFT and the new TFT at $V_{\rm GS} = -20$ V and $V_{\rm GS} = -5$ V.

It is observed that the ON current of the new TFT is almost identical to the conventional nonoffset TFT and one order of magnitude higher than that of the offset TFT. The OFF state leakage current of the new TFT is two orders of magnitude lower than that of the conventional nonoffset TFT at $V_{\rm GS} = -20$ V. As the drain voltage is reduced to $V_{\rm DS} = 5$ V, the OFF state leakage current of the new TFT is almost same as that of the offset TFT.

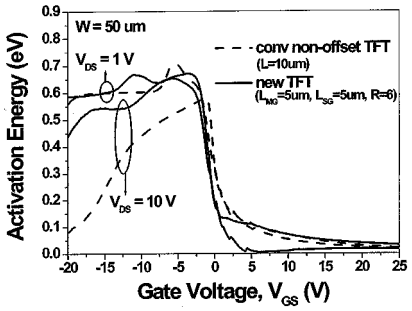


Fig. 9. Activation energy of the conventional TFT and the new TFT at $V_{\rm DS} = 1$ V and $V_{\rm DS} = 10$ V.

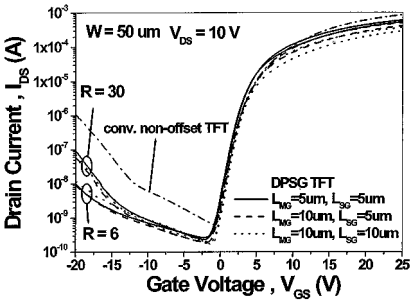


Fig. 10. $I_{\rm DS}$–$V_{\rm GS}$ characteristics of the conventional TFT and the new TFT with various combinations of main gate length $L_{\rm MG}$ and subgate length $L_{\rm SG}$.

It is also found that the ON/OFF current ratio is remarkably improved by two orders of magnitude in the new TFT.

Fig. 6 shows the effect of area ratio R on $I_{\rm DS}$-$V_{\rm GS}$ characteristics at $V_{\rm DS} = 10$ V. As R increases up to 30, the new TFT behaves as the conventional nonoffset TFT. On the other hand, as R decreases down to 1, the new TFT acts as an offset TFT. Fig. 7 shows the OFF state leakage current measured at $V_{\rm GS} = -20$ V and the ON current measured at $V_{\rm GS} = 25$ V for various area ratios R. The optimum condition of the new TFT can be achieved at $R = 6$. Fig. 8 shows that the OFF state leakage current of the new TFT measured at $V_{\rm GS} = -20$ V and $V_{\rm GS} = -5$ V as a function of the drain potential $V_{\rm DS}$. It is observed that the OFF state leakage current of the new TFT has less dependence on $V_{\rm DS}$ than that of the nonoffset TFT. This is because the dependence of the drain electric field on the drain potential in the new TFT is weaker than that in the conventional nonoffset TFT. Fig. 9 shows the activation energy for the first new TFT and the conventional nonoffset TFT measured at $V_{DS} = 1$ V and $V_{DS} = 10$ V with the temperature from 25 °C to 125 °C. The activation energy E_{AV} is extracted from the equation of $I = I_0 \bullet \exp(-E_{AV}/kT)$, where T is the absolute temperature k is the Boltzman constant, and I_0 is the pre-exponential factor. It is observed that the activation energy of the new TFT is higher than that of the nonoffset TFT in the OFF state at $V_{\rm DS} = 10$ V while the activation energy of the new TFT is identical with that of the nonoffset TFT in the OFF state at $V_{\rm DS} = 1$ V. The reduction of the activation energy of the conventional nonoffset TFT at high drain potential $V_{\rm DS} = 10$ V in the OFF state can be attributed to the high electric field near the drain [11]. Therefore, it implies that the drain electric field of the new TFT is smaller than that of the conventional nonoffset TFT in the OFF state. Fig. 10 shows the $I_{\rm DS}$–$V_{\rm GS}$ characteristics of the new TFTs with

various main gate lengths L_{MG} and subgate lengths L_{SG}. They show almost identical OFF state leakage currents, while the ON current is reduced for long channel. The OFF state leakage current of the new TFT is strongly determined by area ratio R.

IV. Conclusion

In this paper, a novel poly-Si thin film transistor with a subgate coupling structure is proposed and fabricated. The OFF state leakage current of the new TFT is greatly reduced without degrading the ON current. Moreover, the new TFT does not require any additional process steps to form the subgate and the fabrication sequences are the same as those of the conventional nonoffset TFT. The ON/OFF current ratio increased by two orders of magnitude can be obtained in the new poly-Si TFT.

References

[1] H. G. Fossum, A. Oritz-Conde, H. Shichijo, and S. K. Banerjee, "Anomalous leakage current in LPCVD polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1878–1884, 1985.

[2] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in sub-microm polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 1218–1223, July 1996.

[3] K. Tanaka, H. Arai, and S. Kohda, "Characterization of offset-structure polycrystalline-silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 9, pp. 23–25, Jan. 1988.

[4] B. H. Min, C. M. Park, and M. K. Han, "A novel offset gated polysilicon thin film transistor without an additional offset mask," *IEEE Electron Device Lett.*, vol. 16, pp. 161–163, May 1995.

[5] C. M. Park, B. H. Min, J. H. Jun, J. S. Yoo, and M. K. Han, "Self-aligned offset gated Poly-Si TFT's with a floating sub-gate," *IEEE Electron Device Lett.*, vol. 18, pp. 16–18, Jan. 1997.

[6] K. M. Chang, Y. H. Chung, G. M. Lin, J. H. Lin, and C. G. Deng, "A novel high-performance poly-silicon thin film transistor with a self-aligned thicker sub-gate oxide near the drain/source regions," *IEEE Electron Device Lett.*, vol. 22, pp. 472–474, Oct. 2001.

[7] C. T. Liu and K. H. Lee, "An experimental study on the short-channel effects in undergated polysilicon thin film transistors with and without lightly doped drain structures," *IEEE Electron Device Lett.*, vol. 14, pp. 149–151, Mar. 1993.

[8] H. C. Lin, C. M. Yu, C. Y. Lin, K. L. Yeh, T. Y. Huang, and T. F. Lei, "A novel thin-film transistor with self-aligned field induced drain," *IEEE Electron Device Lett.*, vol. 22, pp. 26–28, Jan. 2001.

[9] K. R. Olasupo, W. Yarbrough, and M. K. Hatalis, "The effect of drain offset on current-voltage characteristics in sub micron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 1306–1308, Aug. 1996.

[10] S. Lifshitz, M. Luryi, R. Pinto, and C. S. Rafferty, "Active-gate thin-film transistor," *IEEE Electron Device Lett.*, vol. 14, pp. 394–396, Aug. 1993.

[11] M. Kimura, "Field and temperature acceleration model for time-dependent dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 46, pp. 220–229, Jan. 1999.

Kow-Ming Chang (M'00) received the B.S. degree (with Great Distinction) in chemical engineering from National Central University, Chung-Li, Taiwan, R.O.C., in 1977, and the M.S. and Ph.D. degrees in chemical engineering from the University of Florida, Gainesville, in 1981 and 1985, respectively, where his doctoral research concerned the processing technologies of compound semiconductors.

In 1985, he joined the Department of Electronics Engineering and Semiconductor Research Center, National Chiao Tung University (NCTU), Hsinchu, Taiwan, where he is presently a Professor. From 1989 to 1990, he was a Visiting Professor with the Electrical Engineering Department, University of California, Los Angeles, where he was engaged in research on the system design of Electron Cyclotron Resonance Chemical Vapor deposition (ECR-CVD) for developing the low temperature processing technology. He was in charge of a 500 kev ion implanter, a selective tungsten LPCVD system, and two UHV-ECR-CVD systems installed in National Nano Device Laboratory (NDL), NCTU. His current research interests are in the physics, technologies, and modeling of heterojunction devices and optoelectronic devices, ULSI key technologies, CMOS devices, and MEMS technologies. He has published over 150 articles in these fields and has served as a Reviewer for international journals such as IEEE Electron Device Letters and the *Journal of Electrochemical Society*.

Dr. Chang is member of Phi Tau Phi, AIChE, and the Electrochemical Society.

Yuan Hung Chung was born in Tainan, Taiwan, R.O.C., in 1973. He received the B.S. and M.S degrees from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1995 and 1997, respectively, where he is currently pursuing the Ph.D. degree in the Institute of Electronics.

His current research interests are in the fabrication of the low-temperature polysilicon thin film transistors, low thermal budget ployoxides, and ultrathin gate-oxide reliability.

Chi-Gun Deng was born in Taipei, Taiwan, R.O.C., on August 28, 1977. He received the B.S. degree in electrical engineering from National Chiao-Tung University of Hsinchu, Taiwan, R.O.C. in 1999, where he is currently pursuing the M.S. degree at the Institute of Electronics.

His research interest is in the novel structure TFT. in which field he will pursue the Ph.D. degree.

Yuan Fu Chung was born in Changhua, Taiwan, R.O.C., in 1974. He received the B.S. degree from the Department of Electronics Engineering, National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1996, and the M.S. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1998.

He is currently a process integration engineer in Taiwan Semiconductor Manufacturing Company (TSMC). His current research interest is in the device failure analysis and ultrathin gate-oxide reliability.

Jian-Hong Lin was born in Taipei, Taiwan, R.O.C., on May 15, 1979. He received the B.S. degree in Industrial engineering from National Taiwan University of Hsinchu, Taiwan, R.O.C., in 2000. He is currently pursuing the M.S. degree at the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

His current research interests are in ULSI key technologies and nanodevice technologies.