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Fabrication of High Performance Low-Temperature Poly-Si Thin-Film Transistors Using a Modulated Process

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A modulated process (MP) for the fabrication of low temperature processed (LTP) polysilicon thin-film transistors (poly-Si TFTs) using fewer processing steps but resulting in improved performance is investigated in this study. The modulated process is characterized by combining the solid-phase crystallization (SPC) step and the implant annealing into a single annealing step processed after the source/drain implantation. This is to say that the processing step of SPC is omitted, such that the SPC and implant annealing are conducted simultaneously. In this way, the process time is substantially shortened and the device performance is significantly improved. The improvement of device performance is presumably attributed to the larger poly-Si grain in the channel region processed by the MP scheme. In addition, the MP samples have a better NH_3-plasma passivation efficiency than the conventional process (CP) samples; this also implies that the MP samples contain larger grains in the channel regions than the CP samples. The electrical stress-induced degradation of device characteristics for the NH_3-plasma passivated MP samples is attributed to the carrier-induced metastable defects in the channel region.
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Low temperature process (LTP) polysilicon thin-film transistors (poly-Si TFTs) have been intensively studied for the application to large-area active matrix liquid-crystal display (AMLCD).[1] Their primary advantages over the conventional amorphous silicon (α-Si) TFTs lie in their high driving current and the availability of both n- and p-channel TFTs. These features facilitate the integration of high performance complementary metal-oxide-semiconductor (CMOS) peripheral drivers with active switching elements on a single glass substrate, thus reducing the number of external connections for improved reliability and reduced cost.[2,3] The channel films for these devices are typically deposited in an amorphous phase, which is then crystallized to become the large-grain polysilicon phase with a smooth surface. Solid-phase crystallization (SPC) is a promising technique because of its simplicity, low cost, and excellent uniformity.[4] Given the upper limit of ~600°C for processing on the glass substrates,[5] SPC using low-temperature (600°C) furnace annealing requires very long anneal time (about 20 h or longer);[6] thus, it suffers from a substantial trade-off between performance and throughput. Various techniques have been employed to shorten the crystallization time, such as metal-induced crystallization,[7] plasma treatments before crystallization,[8] and laser-induced crystallization.[9] However, these techniques require many extra processing steps or need expensive processing equipment. In addition, for the fabrication of LTP poly-Si TFTs with traditional procedures, the implant annealing which is used to activate dopants and remove damage defects usually is carried out using furnace annealing at 600°C for a long time (about 12-24 h) after the source/drain implantation. The prolonged process time of both SPC and implant annealing causes low throughput in the fabrication of LTP poly-Si TFTs.

In this work, the LTP poly-Si TFTs were fabricated using a modulated process, in which the SPC and implant annealing are combined in one step so that the processing time is greatly reduced. This is to say that the processing step of SPC conventionally used for transforming the as-deposited amorphous silicon to polycrystalline silicon is to be omitted, such that SPC and implant annealing are conducted simultaneously. Because the as-deposited amorphous silicon channel regions and the implanted source/drain regions are crystallized simultaneously, the grain size in the channel region will be enhanced due to the difference of crystallization velocity between the two regions. Thus, high performance LTP poly-Si TFTs can be fabricated using the modulated process (MP) with a higher throughput than the conventional process (CP). Furthermore, the passivation scheme using NH_3 plasma is investigated with respect to the promotion of device performance. By comparing the difference of the passivation efficiency between the MP and the CP, we are able to identify the speculated mechanism that improves the TFT performance using the modulated process. Finally, the effects of dc electrical stress on TFT performance are also investigated.

Experimental

Two sets of self-aligned top-gated n-channel poly-Si TFTs were fabricated in this study using the CP as well as the MP. With regard to the devices fabricated by CP, the TFTs were fabricated following the traditional process procedures; this is, solid-phase crystallization (SPC) was performed at 600°C for 24 h in N_2 ambient immediately after the deposition of amorphous silicon, and the implant annealing was performed also at 600°C for 24 h in N_2 ambient after the source/drain implantation. As for the devices fabricated by MP, the process step of SPC was omitted and the implant annealing at 600°C for 24 h in N_2 ambient was the only thermal process, which was performed after the source/drain implantation. Aside from being different in this respect, all devices were fabricated according to the following procedures. A 110 nm thick low pressure chemical vapor deposition (LPCVD) amorphous Si layer was first deposited on a 500 nm thermal-oxide-covered Si substrate at 550°C using a SiH_4 process. Then, SPC was performed at 600°C for 24 h in N_2 ambient for phase transformation from amorphous silicon to polysilicon (for CP only, not for MP). Individual active regions were then patterned and defined. After a standard RCA clean, a 120 nm thick tetraethyl orthosilicate (TEOS) oxide was deposited to serve as the gate insulator. A second poly-Si film was subsequently deposited and patterned to define the gates of the devices. The TEOS oxide on the source/drain regions served as the etching stop because of the etching rate difference between the TEOS oxide and poly-Si during the reactive ion etching (RIE) gate etching. Next, the source/drain and gate regions were doped with phosphorus via self-aligned ion implantation at 40 keV to a dose of 5×10^{15} cm^{-2}. Then, implant annealing was performed at 600°C for 24 h in N_2 ambient. A 500 nm thick PE-TEOS oxide was deposited at 300°C. Finally, contact holes were opened, and 500 nm thick Al electrodes were deposited and patterned, followed by a sintering process at 400°C for 30 min in N_2 ambient. To passivate the trap states in the poly-Si channel, a group of TFTs, including CP and MP fabricated devices, were subjected to NH_3-plasma hydrogenation at 300°C for various times in a parallel plate reactor with a power density of 0.7 W/cm^2. In this study, all devices investigated have a gate width/length of 24/4 μm.

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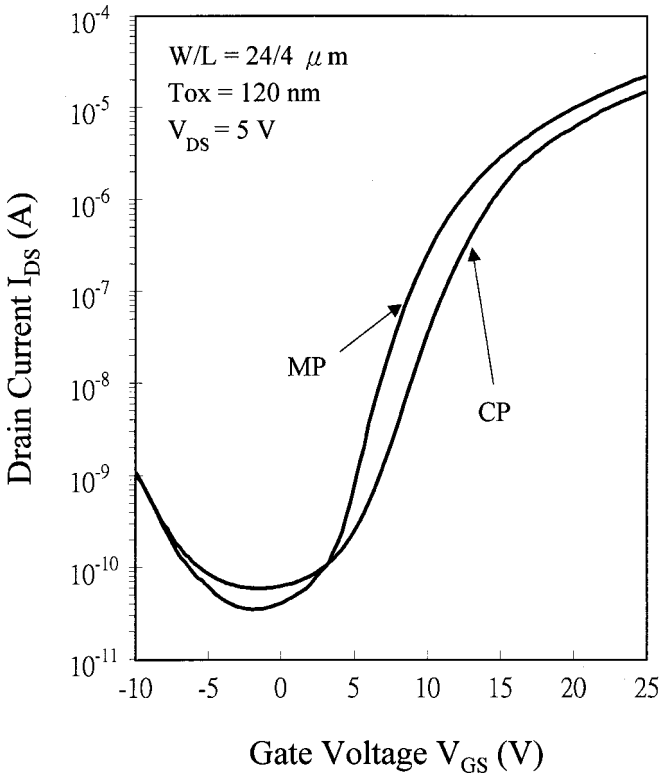

Figure 1. Transfer characteristics (I_{DS} − V_{GS}) of poly-Si TFTs fabricated with two different processes, CP and MP.

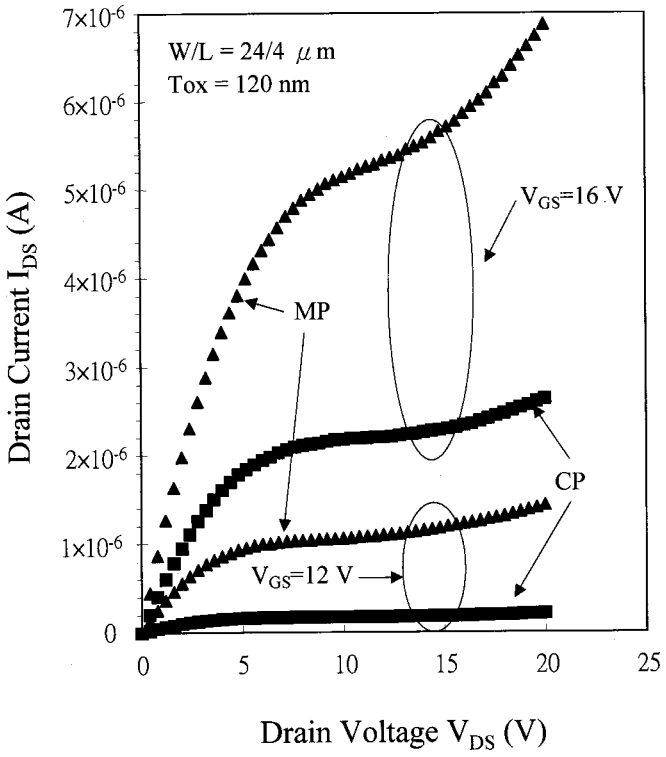

Figure 2. Output characteristics (I_{DS} − V_{DS}) of poly-Si TFTs fabricated with two different processes, CP and MP.

The *I-V* characteristics of the fabricated devices were measured using an HP-4145B semiconductor parameter analyzer. Various device parameters, including the threshold voltage (V_{TH}), subthreshold swing (*SS*), and minimum leakage current (I_{OFF}) were measured at a drain voltage of V_{DS} = 5 V. The threshold voltage is defined as the gate voltage which yields a drain current (I_{DS}) of 600 nA (I_{DS} = 100 nA × W/L). The field-effect mobility (μ_{FE}) is calculated from the maximum value of the transconductance at V_{DS} = 0.1 V. The maximum and minimum values of I_{DS} at V_{DS} = 5 V are designated as I_{ON} and I_{OFF}, respectively.

Results and Discussion

Effects of modulated process on device characteristics.—Figure 1 shows the typical transfer characteristics (I_{DS}-V_{GS}) at V_{DS} = 5 V for the poly-Si TFTs fabricated with two different processes, CP and MP. During the drain current measurement, the gate voltage was swept from −15 to 25 V. The measured as well as extracted key devices parameters, including V_{TH}, *SS*, μ_{FE}, I_{OFF}, and ON/OFF current ratio (I_{ON}/I_{OFF}) are summarized in Table I. Obvious improvement in devices characteristics was obtained by using MP instead of CP, as shown in Table I, V_{TH} decreased from 13.8 to 11.3 V, *SS* decreased from 2.02 to 1.81 V/dec, μ_{FE} increased from 4.85 to 7.43 cm^2/V · s, I_{off} decreased from 58.6 to 34.9 pA, and I_{ON}/I_{OFF} ratio increased from 2.5 × 10^5 to 6.3 × 10^5. Figure 2 shows the typical output characteristics (I_{DS}-V_{DS}) at two different gate voltages for the poly-Si TFTs fabricated with two different processes, CP and MP. It can be seen that the TFTs fabricated with MP exhibited significant improvement in the turn-on state performance. This improvement in the performance of the MP fabricated devices is presumably due to the larger grain size in the poly-Si channel, in which the enhancement of grain size is believed to be arisen from the difference of crystallization velocity between the implanted source/drain and the deposited α-Si channel regions.[10]

Table I. Comparison of device characteristics for poly-Si TFTs fabricated with the CP and the MP.

Parameters	CP	MP
Threshold voltage, V_{TH} (V)	13.8	11.3
Subthreshold swing, *SS* (V/dec)	2.02	1.81
Field-effect mobility, μ_{FE} (cm^2/V s)	4.85	7.43
Leakage current, I_{OFF} (p/A)	58.6	34.9
ON/OFF current ratio, I_{ON}/I_{OFF}	2.5 × 10^5	6.3 × 10^5

The crystallization from an amorphous phase to a polycrystalline phase occurs through two processes, nucleation and grain growth.[11] As the SPC annealing proceeds, nuclei are first generated in the films, and the growth of nuclei into grain follows. The grain growth starts at nuclei formation and stops when the adjacent grains come into contact with each other. To obtain the largest grain size, low nucleation rate and high grain growth rate are indispensable.[12] Moreover, it is well known that many implanted impurities, such as boron and phosphorus, have the effect of enhancing Si self-migration. Due to the increase in defect density in the implanted source/drain region, the self-migration coefficient is increased, causing decreased activation energies for both nucleation and grain growth.[13,14] As a result, the nucleation rate and the growth rate of grain are increased in the implanted source/drain region. Thus, the crystallization time of the implanted source/drain amorphous regions will be significantly reduced.[10]

Based on the above discussions, a crystallization model is proposed to account for larger grain size in the channel regions of the MP samples. With the SPC process for the nondoping channel regions combined with the implant annealing for the doped source/drain regions, nucleation sites will first appear in the implanted source/drain regions which have a higher nucleation rate due to larger self-migration coefficient. As the crystallization proceeds, nuclei grow into grains and individual grains in the source/drain regions continue to grow and coalesce into larger grains, while the

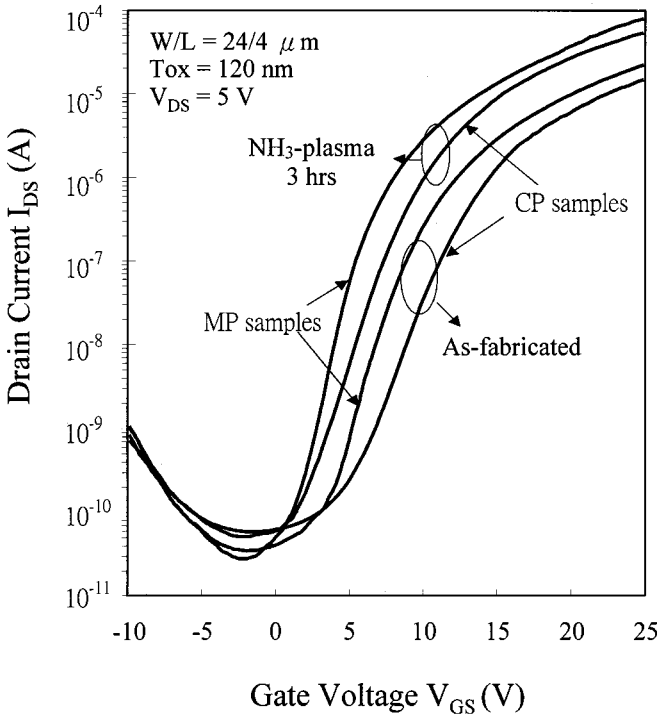

Figure 3. Transfer characteristics ($I_{DS} - V_{GS}$) of poly-Si TFTs before and after NH_3-plasma treatment for 3 h.

α-Si in the nondoping channel regions remains in the amorphous state because the incubation time in this region is larger than that in the source/drain region. Subsequently, the coalescing grains can act as seeds to grow laterally into the α-Si channel region. However, as the lateral growth proceeds and when the annealing time is larger than the incubation time of α-Si channel regions, nucleation will also begin to occur in the channel region followed by the grain growth. Finally, the lateral growth will stop when the laterally grown grains come into contact with the self-formed grains of the channel regions. Thus, the channel regions are crystallized laterally from the nucleation sites formed in the source/drain areas but the nucleation and grain growth rates of the channel regions will limit the distance of lateral growth. Moreover, we believe that the larger the difference of crystallization rates between the doped source/drain regions and the nondoping channel regions is, the larger the grain size will be in the channel regions. As for the CP, the grain size in the channel regions remains nearly unchanged during the implant annealing because the existing grains formed in the SPC step impede the regrowth of grains during the implant annealing.[15] Thus, we presume that the MP resulted in larger grains in the channel regions than the CP.

Effects of NH_3-plasma treatment.—It has been reported that large grain poly-Si films have a better passivation efficiency as a result of low defect density because of their smaller grain boundary density.[16] Thus, to confirm the speculation that the MP fabricated devices contain larger grains in the channel regions (as described above), the completed poly-Si TFTs were subjected to NH_3-plasma hydrogenation. Figure 3 shows the typical transfer characteristics ($I_{DS} - V_{GS}$) of poly-Si TFTs before and after NH_3-plasma treatment for 3 h. The plasma treatment clearly improved the transfer characteristic for both CP and MP devices. The measured, as well as extracted key devices parameters, are summarized in Table II. By comparing the date in Tables I and II, we found significant improvement in various devices characteristics for both CP and MP samples by the NH_3-plasma treatment, in particular the MP samples. To distinguish the passivation efficiency between the CP and MP samples,

Table II. Comparison of device characteristics for poly-Si TFTs fabricated with the CP and the MP after NH_3-plasma treatment for 3 h.

Parameters	CP	MP
Threshold voltage, V_{TH} (V)	9.5	6.9
Subthreshold swing, *SS* (V/dec)	1.71	1.16
Field-effect mobility, μ_{FE} (cm^2/V s)	11.7	17.3
Leakage current, I_{OFF} (pA)	51.2	27.7
ON/OFF current ratio, I_{ON}/I_{OFF}	1.5×10^6	2.9×10^6

the device characteristics were evaluated as a function of NH_3-plasma treating time. Figures 4 and 5 show the percentage improvement (*i.e.*, percentage decrease) in threshold voltage (V_{TH}) and *SS*, respectively, as a function of NH_3-plasma treatment time for both CP and MP samples. The extent of improvement in V_{TH} and *SS* continuously increased with the passivation time, and the improvement rate of MP samples is higher than that of CP samples, in particular the improvement in *SS* as shown in Fig. 5. It is well known that the effective trap state density at the grain boundary of the poly-Si/SiO_2 interface and the poly-Si channel region is closely related to the subthreshold swing ($S = dV_{GS}/d \log I_{DS}$). By neglecting the depletion capacitance in the active layer, the trap state density N_T can be estimated from the relation[17,18]

$$N_T = \frac{C_{OX}}{q}\left(\frac{q}{KT}\frac{S}{\ln 10} - 1\right)$$

where C_{OX} is the oxide capacitance. The trap state densities for the MP samples before and after the plasma passivation for 3 h are determined to be 5.28×10^{12} and 3.32×10^{12} cm^{-2}, respectively, while the corresponding densities for the CP samples before and

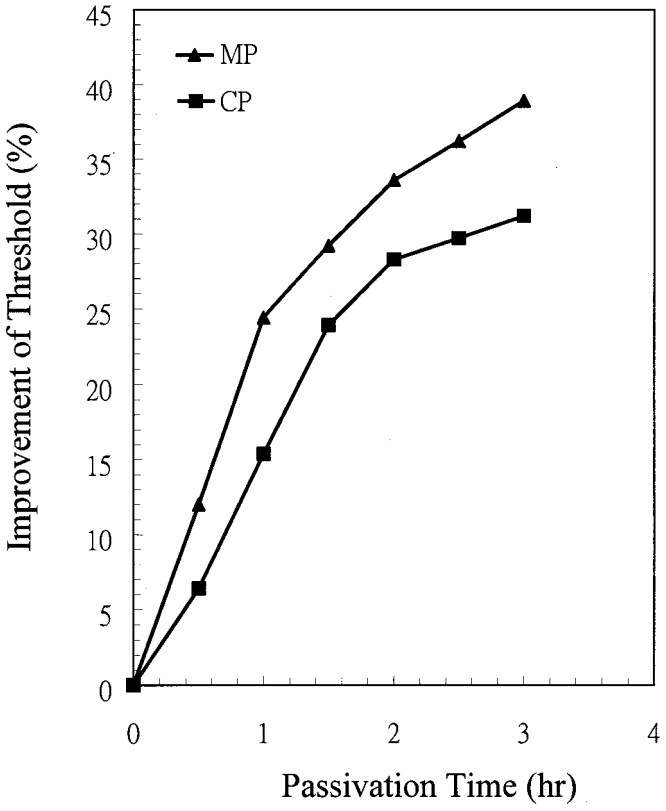

Figure 4. Improvement in threshold voltage (*i.e.*, percentage decrease in V_{TH}) as a function of NH_3-plasma passivation time for CP and MP samples.

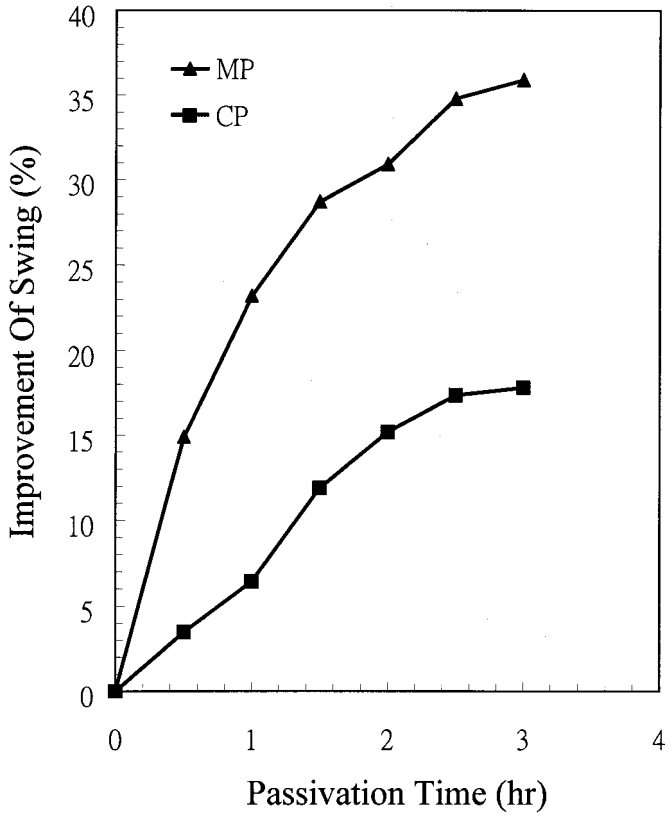

Figure 5. Improvement in subthreshold swing (*i.e.*, percentage decrease in *SS*) as a function of NH_3-plasma passivation time for CP and MP samples.

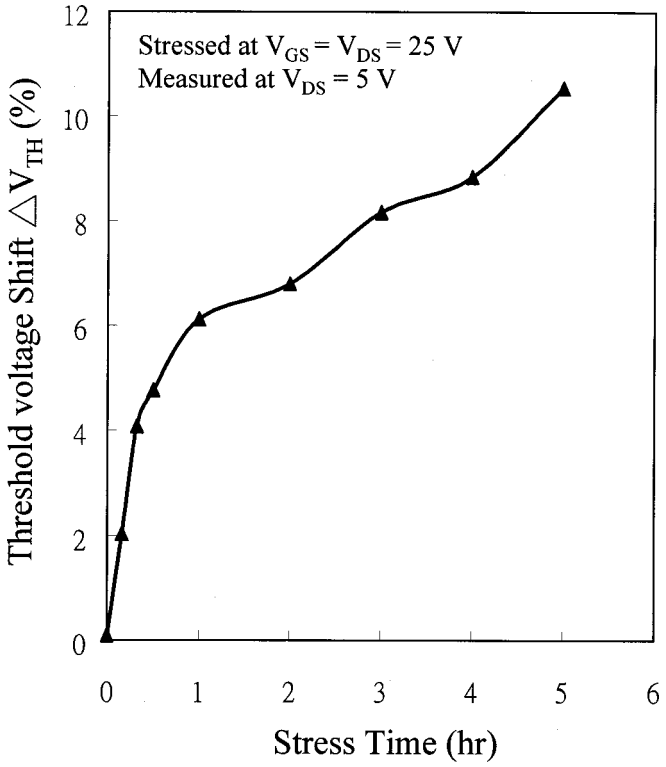

Figure 6. Threshold voltage shift *vs.* stress time for poly-Si TFT fabricated with the MP and NH_3-plasma treated for 3 h. The device was stressed at $V_{GS} = V_{DS} = 25$ V and measured at $V_{DS} = 5$ V.

after the plasma treatment are found to be 5.91×10^{12} and 4.97×10^{12} cm^{-2}, respectively. The NH_3-plasma treatment significantly reduced the trap state density for both MP and CP samples, in particular the MP sample. Since large grain poly-Si films have a better passivation efficiency because of their smaller density of grain boundary,[16] the larger grain in the channel regions of the MP samples is presumably responsible for the larger extent of N_T reduction. Thus, the higher passivation rate and better characteristic improvement for the MP devices, as shown in Fig. 4 and 5, imply that MP devices contain larger grain than the CP devices.

It has been reported that V_{TH} and *SS* are closely related to the dangling bond midgap states, while μ_{FE} is dominated by the intragranular band tail states in poly-Si TFTs. The dangling bonds midgap states have a faster response to hydrogenation, while the intragranular tail states respond more slowly to hydrogenation. Only when the hydrogenation concentration is so large as to fill both the midgap states and the tail states will a significant fraction of the tail states be passivated. Moreover, if the interior of the grains contains a large number of tail states, the passivation will be slow for this type of defect.[16] Thus, the NH_3-plasma passivation resulted in a larger improvement in *SS* for the MP sample than for the CP sample, while the improvement in μ_{FE} was nearly the same for both MP and CP samples.

From the above discussions, we may conclude that, as a result of larger grain size and thus lower grain boundary density in the poly-Si channel, the MP sample has a better passivation efficiency on grain-boundary dangling bonds, leading to a better improvement in *SS* and V_{TH}. The results are consistent with the speculation in the section on the Effects of the modulated process that the MP resulted in larger grain size in the channel regions than the CP. Thus, we suggest the combination of the SPC step and the implanting annealing into a single processing step for the fabrication of LTP poly-Si TFTs with the conventional self-aligned scheme. In this way, the devices characteristics can be improved while the process time is significantly reduced. Moreover, it is worth noticing that, if the difference of crystallization rate between the doped source/drain regions and the nondoping channel regions becomes sufficiently large, the modulated annealing process may result in only one single-grain boundary in the middle of the channel region for devices of very small dimensions. Thus, not only the device performance but also the characteristic uniformity can be improved, in particular the devices of very small geometry.

Reliability.—The reliability of poly-Si TFTs fabricated with the MP and NH_3-plasma treated for 3 h, was investigated with respect to dc electrical stress. Figure 6 shows the changes in V_{TH} as a function of stress time for ON-state stressing with $V_{GS} = V_{DS} = 25$ V. The percentage shift of threshold voltage ΔV_{TH} is defined $\Delta V_{TH}(\%) = [(V_{TH}$ after stress $- V_{TH}$ before stress$)/V_{TH}$ before stress$] \times 100\%$. It is found that the V_{TH} increased with the stress time, which is similar to the conventional LTP poly-Si TFTs reported in literature.[19,20] Furthermore, both μ_{FE} and I_{OFF} remained nearly unchanged after the dc electrical stress. Since the measured I_{DS}-V_{GS} characteristics after the dc electrical stress are nearly equal for the forward and reverse modes, the charge trapping in the oxide is presumably not the dominant degradation mechanism. Instead, the degradation of V_{TH} is presumably due to the carrier-induced metastable defects within the channel regions. The formation of the carrier-induced metastable defects is attributed to the breaking of the weak Si-Si and Si-H bonds in the poly-Si channel regions by the channel carriers during stressing.[20]

Conclusions

The modulated process (MP) for the fabrication of LTP poly-Si TFTs was investigated. The MP is characterized by combining the solid-phase crystallization (SPC) with the implanting annealing into a single annealing step processed after the source/drain implanta-

tion. In this way, the process time is substantially shortened and the poly-Si grains in the channel region can be significantly enlarged. As a result of larger grain size, the performance of the poly-Si TFTs fabricated with the MP scheme is superior to those fabricated with CP. The formation of larger grain size by the MP scheme is attributed to the difference of the crystallization velocity between the nondoping channel regions and the doped source/drain regions. Moreover, the passivation treatment by NH_3-plasma improved the device characteristics, and the passivation rate for the MP samples is higher than that for CP samples, which may imply that the MP samples contain larger grains in the channel regions than the CP samples. The electrical stress-induced degradation of devices characteristics for the NH_3-plasma passivated MP samples is attributed to the carrier-induced metastable defects in the channel region. In summary, the modulated process is a simple and high throughput process for the fabrication of high performance LTP poly-Si TFTs.

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