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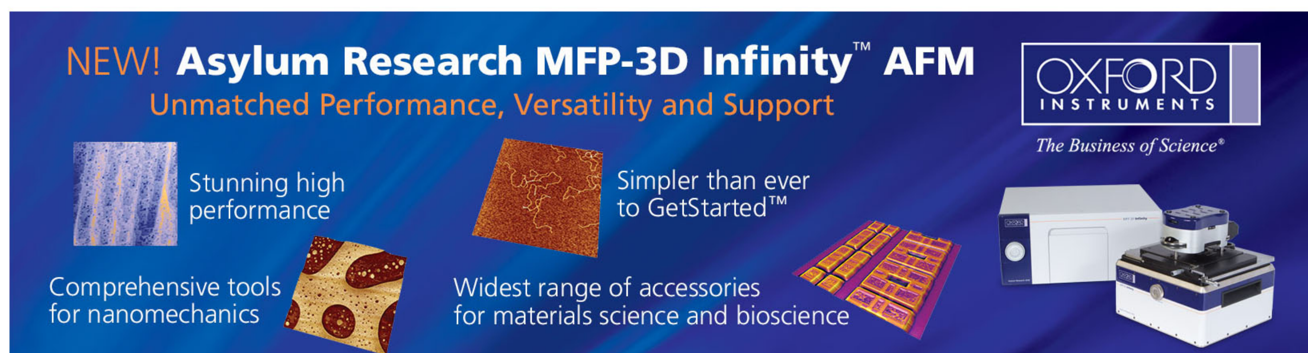

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Effect of annealing temperature on physical and electrical properties of $Bi_{3.25}La_{0.75}Ti_3O_{12}$ thin films on Al_2O_3-buffered Si

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The effect of annealing temperature, especially at high temperatures, on the physical and electrical properties of $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) thin films on Al_2O_3 (10 nm)/Si has been investigated. The width of memory window in capacitance–voltage curves for BLT/Al_2O_3/Si capacitors annealed at temperature range of 700 °C–950 °C increases with increasing annealing temperature. At the highest annealing temperature of 950 °C, a large ferroelectric memory window of 13 V is obtained under $\pm$15 V sweep voltage, and this large ferroelectric memory window should be related to the reduced leakage current. Owing to the excellent electrical properties, the high-temperature stable BLT/Al_2O_3/Si capacitor is compatible with current very large scale integrated technology process.
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Ferroelectric random access memories have attracted much attention recently because of the lower writing voltage and faster switching speed than those of Flash memory.[1–4] To further improve the cell size and device performance, one transistor (1T) ferroelectric metal–oxide–semiconductor field-effect transistor (FeMOSFET) type memory is desirable.[5–8] Unfortunately, the progress of 1T FeMOSFET memory is obstructed by the interface reaction between ferroelectric materials and Si that greatly degrades the device characteristics.[8,9] Recently, we have developed 1T memory using Pb(Zr,Ti)O_3 (PZT)[4] and Al_2O_3 (Refs. 10 and 11) stack gate dielectrics on Si and good memory characteristics are obtained. However, high-temperature stable ferroelectric materials on Si are still necessary for the process integration with current very large scale integrated (VLSI) technology.[12] Since further ferroelectric performance improvement and VLSI process integration are required, bismuth layer-structured ferroelectric $Bi_4Ti_3O_{12}$ has been paid attention due to its higher Curie temperature of 675 °C than that of $SrBi_2Ta_2O_9$ (SBT).[13] Recently, lanthanum-substituted bismuth titanate [$Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT)] were widely studied because of its enhanced nonfatigue behavior that is superior to PZT and comparable with SBT.[14] In this letter, our recent results will be reported on the effect of annealing temperature on the physical properties of BLT thin films and the memory properties of BLT/Al_2O_3/Si capacitor. Our results suggest that 1T BLT/Al_2O_3/Si FeMOS capacitor annealed at high temperatures exhibits large memory window due to very low leakage current.

4 in. (100) Si wafers with ~10 Ω cm resistivity were used in this study. For the FeMOS structure, a 10 nm thick Al_2O_3 gate dielectric was first formed on Si and the detailed formation procedure was reported previously.[10,11] Then, BLT films were deposited on Al_2O_3/Si by chemical solution deposition using spin coating at 4000 rpm for 30 s.[8] An excess of 10% Bi precursor was added to compensate for the Bi loss during annealing. After each coating, the deposited films were pyrolyzed for several minutes and the formed multilayer films were further annealed at the high temperatures of 700 °C, 850 °C, and 950 °C under an oxygen ambient. Au and Al were used as upper electrode and bottom electrode and the capacitor area is 5×10^{-4} cm^2. The phase and microstructure of BLT were observed by x-ray diffraction (XRD) and scanning electron microscopy (SEM). The elemental depth profiles were examined using secondary ion mass spectroscopy (SIMS). The electrical properties were characterized by capacitance–voltage ($C-V$) and current density–voltage ($J-V$) measurements.

Figure 1 shows the XRD patterns of BLT films annealed at different temperatures. It was observed that all BLT films are polycrystalline and high quality ferroelectric BLT could be obtained at the annealing temperatures of 700 °C–950 °C. For the BLT films annealed at 700 °C, the XRD pattern is similar to that of $Bi_4Ti_3O_{12}$ powder and no preferred orientation was identified. In the case of BLT films annealed at

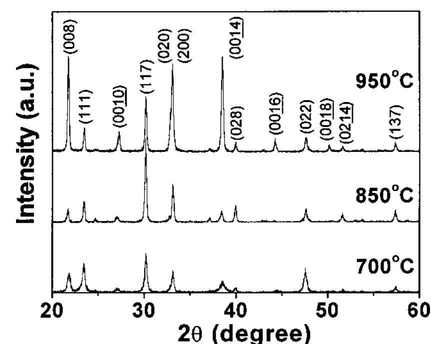

FIG. 1. XRD patterns of BLT films annealed at 700 °C, 850 °C, and 950 °C.

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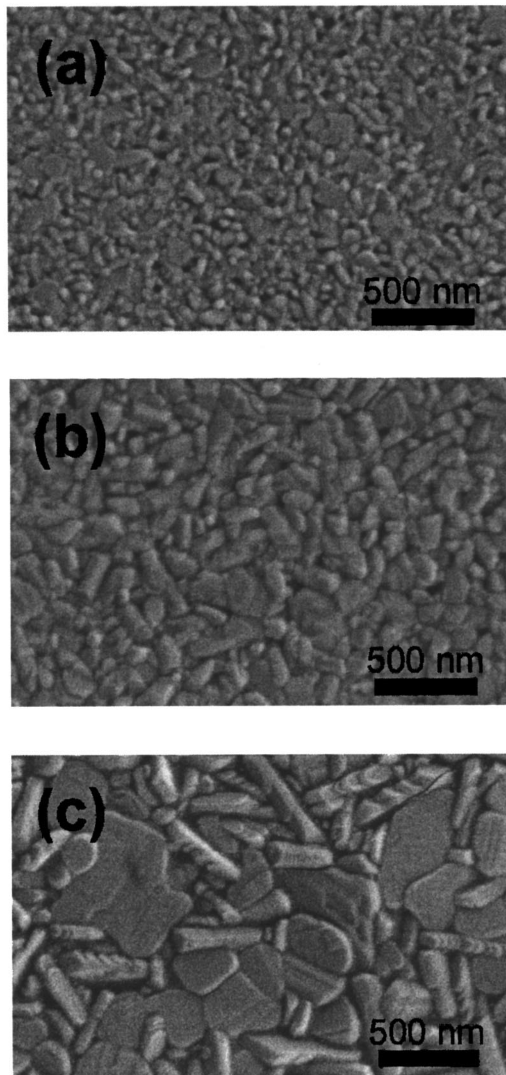

FIG. 2. SEM images of BLT films annealed at (a) 700 °C, (b) 850 °C, and (c) 950 °C.

850 °C, the intensity of (117) main peak increases. However, as the BLT films were annealed at 950 °C, the (008) peak becomes the strongest one, indicating that the preferred orientation[15] is different from that of the 700 °C and 850 °C annealed samples.

The surface morphology of BLT films annealed at 700 °C, 850 °C, and 950 °C was examined by SEM and is illustrated in Figs. 2(a), 2(b), and 2(c), respectively. The grain sizes of BLT films become larger as the annealing temperature increases. In addition to the rod-like grain shown in Figs. 2(a) and 2(b), the apparently large planar grains were observed for the BLT films annealed at 950 °C. The planar grains may correspond to the preferred orientation of XRD patterns shown in Fig. 1(c).

SIMS was used to investigate the elemental diffusion from BLT thin films through Al_2O_3 because Bi diffusion could cause the degradation of device performance.[16] Figure 3 shows the SIMS profile of BLT/Al_2O_3/Si annealed at 950 °C and no significant Bi diffusion was observed. This result demonstrates that Al_2O_3 dielectric would be a suitable material as the buffer layer between the BLT films and Si substrate in 1T FeMOS capacitor structure.

The $C-V$ characteristics of BLT/Al_2O_3/Si capacitors

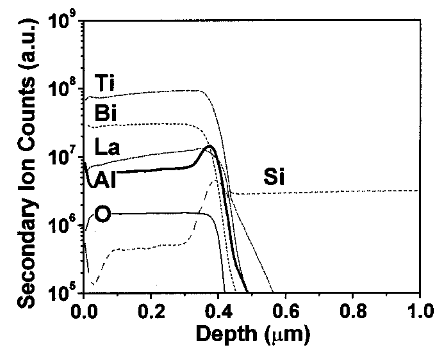

FIG. 3. SIMS spectra of BLT/Al_2O_3/Si annealed at 950 °C.

were measured at 1 MHz. Figure 4 shows the typical $C-V$ curves and the memory windows of BLT/Al_2O_3/Si annealed at 700 °C, 850 °C, and 950 °C. The well-behaved $C-V$ curves without distortion were obtained and this could be associated with the little diffusion observed in SIMS profile. As shown in Fig. 4, the positive memory window value is related to a clockwise hysteresis loop attributed to the ferroelectric behavior,[6,17] while the negative memory window value corresponds to the counter-clockwise hysteresis loop caused by the charge injection phenomenon. For the sample annealed at 700 °C, both ferroelectric and charge injection modes were observed. In sharp contrast, only ferroelectric mode was observed for the samples annealed at 850 °C and 950 °C and the memory window values become larger at higher write voltages up to ±15 V. A large memory window of 13 V was obtained for the 950 °C-annealed samples. Additionally, a memory window of ~2 V could be obtained under ±5 V sweep voltage in both samples annealed at 850 °C and 950 °C and this suggests the possibility for low-voltage operation.

We have also investigated the current–voltage characteristics because the leakage current is one of the most important properties for memory capacitor. Figure 5 shows $J-V$ curves of BLT/Al_2O_3/Si capacitors annealed at different temperatures. The leakage current density of BLT/Al_2O_3/Si annealed at 700 °C is 4.7×10^{-7} A/cm^2 at -100 kV/cm that is comparable to that of vanadium-doped $Bi_4Ti_3O_{12}$ (Ref. 18) but it increases rapidly at high voltages. On the other hand, for BLT/Al_2O_3/Si annealed at 850 °C and 950 °C, the leakage current reduces ~3 orders of magnitude at -100 kV/cm. The low leakage current is also smaller than our previous

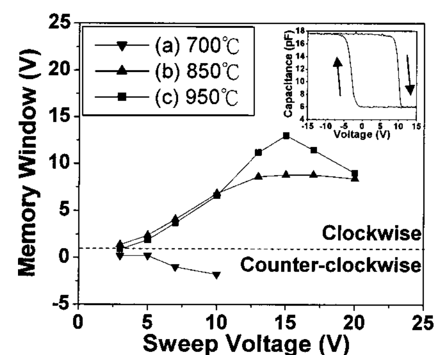

FIG. 4. Memory windows of BLT/Al_2O_3/Si capacitors annealed at 700 °C, 850 °C, and 950 °C. The inserted $C-V$ curves are the BLT/Al_2O_3/Si capacitors annealed at 950 °C with program/erase voltages of ±15 V.

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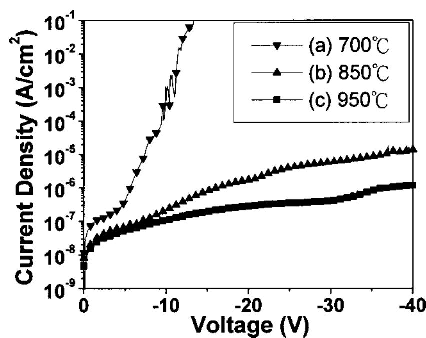

FIG. 5. $J-V$ characteristics of BLT/Al_2O_3/Si capacitors annealed at 700 °C, 850 °C, and 950 °C.

data of PZT/Al_2O_3/Si FeMOS.[5–8] In addition, no dielectric breakdown up to −40 V also implies that the BLT films annealed at high temperatures have better dielectric integrity than that annealed at 700 °C. This smaller leakage current and larger breakdown voltage may be related to the microstructure of BLT films shown in Figs. 2(b) and 2(c). The much reduced leakage current of BLT annealed at high temperatures is a strong advantage because this is directly correlated with the applied switching energy and scaling trend in VLSI technology.

In conclusion, we have studied the annealing temperature dependent characteristics of BLT/Al_2O_3/Si. At the annealing temperature of 950 °C, the large memory window of 13 V is obtained under ±15 V sweep voltage. The leakage current density is also reduced by three orders of magnitude lower than that annealed at 700 °C. Although future work is underway to investigate the possible mechanism of the enhanced electrical properties, the high annealing temperature makes the stack gate BLT/Al_2O_3/Si process compatible with current VLSI technology.

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