Evaluation of Electrical Characteristics of the Copper-Metallized SPDT GaAs Switches at Elevated Temperatures

Yun-Chi Wu, Edward Yi Chang, *Senior Member, IEEE*, Yueh-Chin Lin, and Li-Han Hsu

***Abstract*—Copper-metallized AlGaAs/InGaAs pseudomophic high-electron mobility transistor single-pole–double-throw (SPDT) switches utilizing platinum (Pt, 70 nm) as the diffusion barrier have been studied and demonstrated. As compared with the Au-metallized switches, the Cu-metallized SPDT switches exhibited comparable performance with insertion loss less than 0.5 dB, return loss larger than 20 dB, isolation larger than 35 dB, and the input power for 1-dB compression (input $P_{1\,\mathrm{dB}}$) of 28.3 dBm at 2.5 GHz. In order to evaluate the temperature-dependent impact on dc and RF characteristics of the copper-metallized switches for high-temperature applications, the switches have been tested at different temperatures. The device exhibits low thermal threshold coefficients ($\delta V_{\mathrm{th}}/\delta T$) of -0.25 mV/K from 300 K to 500 K, good microwave performance at 380 K with insertion loss less than 0.5 dB, isolation higher than 40 dB, and the input power for 1-dB compression (input $P_{1\,\mathrm{dB}}$) of 28.45 dBm at 2.5 GHz. To test the thermal stability of the Pt diffusion barrier, these switches were annealed at 250 °C for 20 h. After the annealing, the switches showed no degradation of the dc characteristics. In addition, after a high temperature storage life environment test at 150 °C, these copper-metallized switches remained capable of excellent power handling. To test the operation reliability of the copper-metallized switches, the copper-metallized switches were subjected to ON/OFF (control voltage $= +3/0$ V exchange) stress test for 24 h at room temperature. The devices maintained excellent RF characteristics after the stress test. Consequently, it is successfully demonstrated through these tests that copper metallization using Pt as the diffusion barrier could be applied to the GaAs monolithic microwave integrated circuit switch fabrication with good RF performance, high-temperature characteristics, and reliability.**

***Index Terms*—Copper metallization, platinum, pseudomophic high-electron mobility transistor (PHEMT), single-pole–double-throw (SPDT), switch, temperature.**

I. Introduction

COPPER has been used instead of aluminum as the interconnect metal for silicon integrated circuit technology since IBM adapted copper metallization in the silicon 0.18-μm technology [1]–[3]. The advantages of using copper metallization for Si technology include low resistivity and high electromigration resistance; however, there are only a few reports on the copper metallization of GaAs devices. Ti/Au interconnect metal has been extensively used for the manufacture of GaAs-based field-effect transistors and monolithic microwave integrated circuits (MMICs), and the reliability of the metal system has been well proven. The application of copper as the metallization metal for GaAs devices has several superior advantages over gold, such as lower resistivity, higher thermal conductivity, and lower cost, as compared with gold. In this paper, we characterized the electrical performance of the copper-metallized AlGaAs/InGaAs pseudomophic high-electron mobility transistor (PHEMT) single-pole–double-throw (SPDT) switches and compare the performance with the gold-metallized GaAs SPDT switches.

Copper diffuses very fast into GaAs if without any diffusion barrier and forms a deep acceptor in GaAs, which leads to the failure of the electrical properties of the GaAs devices. It was demonstrated that TaN can be used as the diffusion barrier for the backside copper metallization on GaAs semiconductor field-effect transistors [4], [5] and that WN_x can be used as the diffusion barrier for copper airbridges on low-noise GaAs HEMTs [6]. Furthermore, Pt was used as the diffusion barrier layer for copper-metallized switches in recent years [7], and a gold-free fully copper-metallized InP heterojunction bipolar transistor was also realized using Ti/Pt/Cu nonalloyed ohmic contacts with Pt as the diffusion barrier in recent years [8]. It has also been demonstrated that the Ti/Pt/Cu system structure was very stable even after being annealed up to 350 °C and that copper started to diffuse through the Pt diffusion barrier and formed a Cu_4Ti phase after being annealed at 400 °C, as investigated by X-ray diffraction data, Auger electron spectroscopy depth profiles, and the sheet resistance measurement [9]. In this paper, the temperature-dependent characteristics of the copper-metallized switches are studied. The thermal stability of the Pt diffusion barrier and the electrical reliability are also investigated.

II. Device Structure and Fabrication

The AlGaAs/InGaAs PHEMT SPDT switch wafer was grown on a 4-in semiinsulating GaAs substrate by metal–organic chemical vapor deposition. The structure, from bottom to top, is composed of a 600-nm superlattice buffer, a 13-nm undoped InGaAs channel, a 3-nm undoped AlGaAs spacer, a delta-doped layer, a 37-nm undoped AlGaAs Schottky layer, and a 60-nm n^+-GaAs capping layer, as shown in Fig. 1. The room temperature electron mobility and sheet carrier

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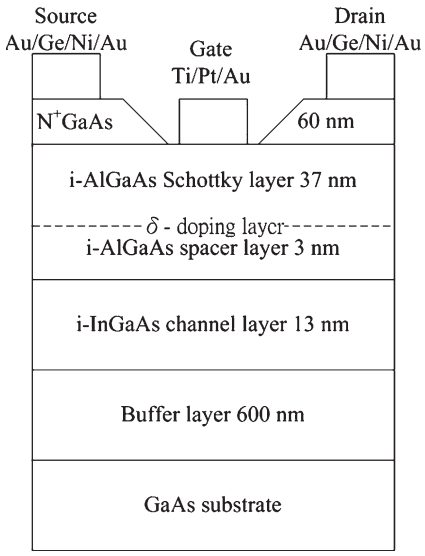

Fig. 1. Epitaxy structure of the PHEMT used in the copper-metallized AlGaAs/InGaAs SPDT switches.

concentrations of the device were 6500 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and $3.0\times10^{12}\ \mathrm{cm}^{-2}$, respectively.

The series/shunt SPDT switch process includes device active region definition, resistor formation, ohmic contact, gate formation, device passivation, capacitor, and interconnect formation. Wet etching with H_3PO_4-H_2O_2-H_2O solution was used for device isolation and epitaxial resistor formation. The ohmic contacts were formed by Au/Ge/Ni/Au evaporation followed by rapid thermal annealing at 410 °C for 30 s. The citric acid and hydrogen peroxide mixed solution was used for the gate recess process. Ti/Pt/Au metal was used as gate metal, and the gate was formed by the lift-off process. Plasma-enhanced chemical vapor deposition silicon nitride film was used for passivation and as the dielectric for capacitors. A 30-nm Ti layer and a 70-nm Pt layer were used as the adhesion layer and the diffusion barrier layer, respectively, for the top plate of the capacitor and the bottom layer of the interconnects [7], [9]. A 2-μm-thick copper metal was electroplated on the Ti/Pt layers with a Cu seeding layer for interconnects. Then, the electroplated copper was annealed at 200 °C for 2 h for eliminating the hydrogen embrittlement effect [10] and obtaining the film with the lowest resistivity and the smoothest surface [11], [12]. Finally, a 100-nm-thick silicon nitride was deposited for final passivation.

The AlGaAs/InGaAs PHEMTs used in the switches had a 0.5-μm gate length with dual fingers, and the drain-to-source spacing was 9 μm. The ohmic contact resistance for the PHEMTs was 0.12 $\Omega\cdot$mm, and the MIM capacitors used in the switches with 200-nm silicon nitride had a capacitance of 0.25-fF/μm^2. A 3 kΩ of gate resistor between the signal and control terminal was designed to provide isolation between the signal and control paths. The circuit schematic of the series/shunt SPDT switch is shown in Fig. 2. The control current of the GaAs SPDT switch is typically < 0.5 mA/mm.

III. Results and Discussion

The HEMTs in the switch fabricated using copper metallization showed similar dc characteristics in comparison with those

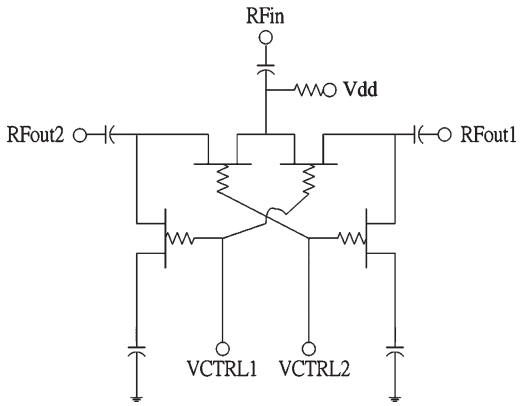

Fig. 2. Circuit schematic of the series/shunt SPDT switch.

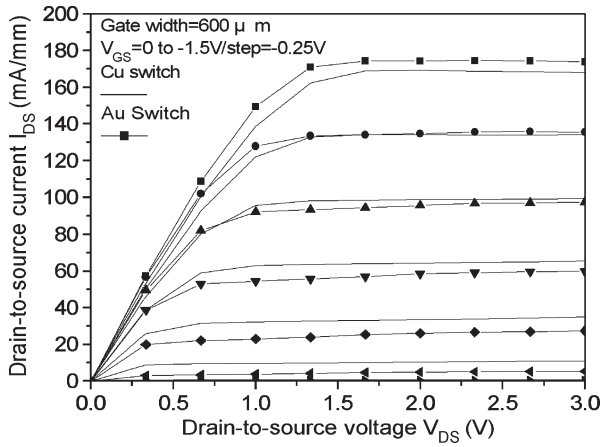

Fig. 3. I–V characteristics of AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length with copper and gold metallizations.

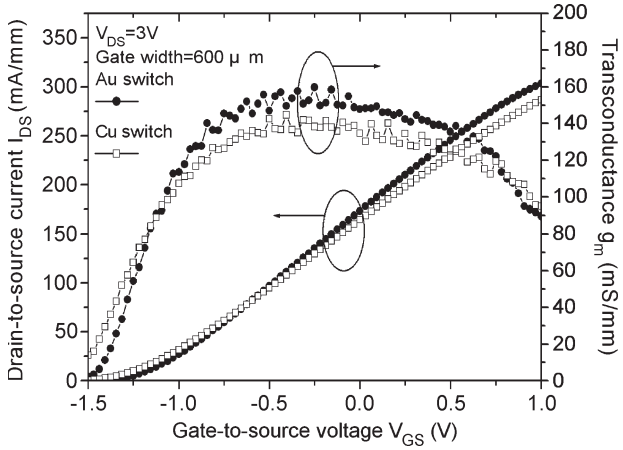

Fig. 4. Extrinsic transconductance and drain-to-source current versus V_{GS} bias characteristics of the AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length with copper and gold metallizations.

in the switch fabricated with traditional gold metallization. As shown in Figs. 3 and 4, a drain saturation current density of 160 mA/mm and an extrinsic transconductance of 140 mS/mm at $V_{\mathrm{DS}} = 3$ V were measured both for the copper- and the Au-metallized switches. The devices had a threshold voltage (V_{th}) of -1.5 V. The insertion loss, return loss, and isolation characteristics of the SPDT switches with copper metallization and with gold metallization measured at 2.5 GHz are shown in

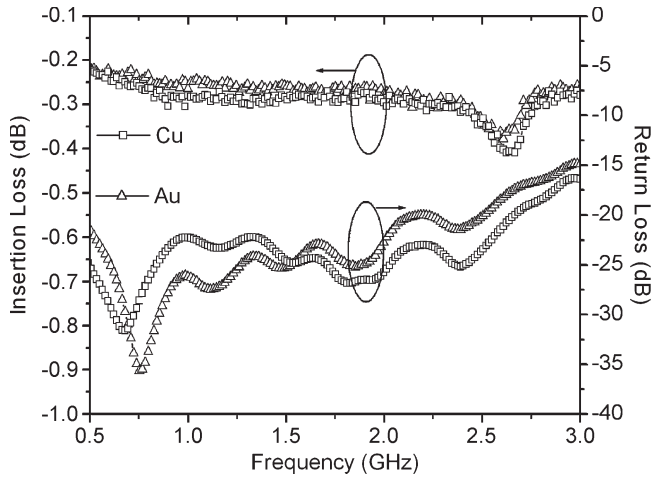

Fig. 5. Insertion loss and return loss versus frequency of the SPDT switches with copper and gold metallizations.

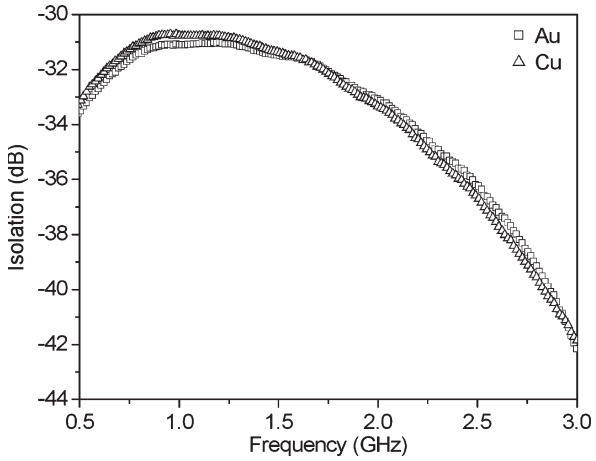

Fig. 6. Isolation versus frequency of the SPDT switches with copper and gold metallizations.

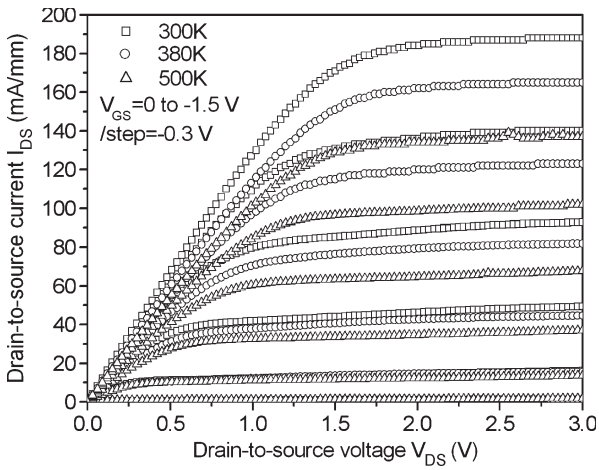

Fig. 7. I–V characteristics of the 0.5-μm gate length PHEMT used in the copper-metallized switches tested at 300 K, 380 K, and 500 K, respectively.

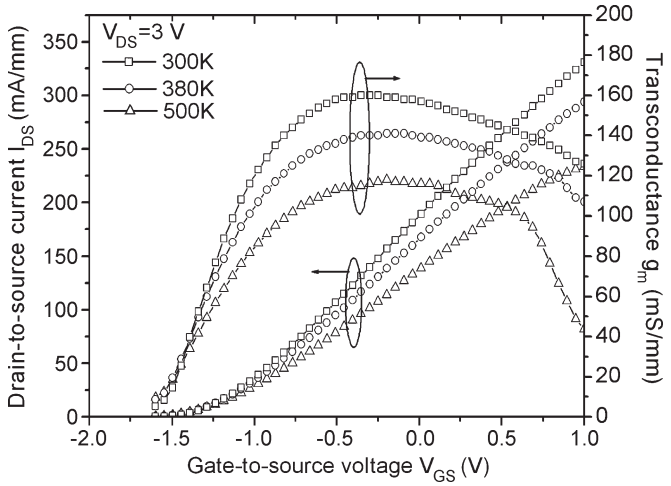

Fig. 8. Extrinsic transconductance and drain-to-source current versus $V_{\rm GS}$ bias characteristics of the 0.5-μm gate length PHEMT used in the SPDT switches when measured at 300 K, 380 K, and 500 K, respectively.

Figs. 5 and 6, respectively. The copper-metallized switch had an insertion loss of 0.33 dB, a return loss of 23.3 dB, and an isolation of 36.7 dB (control voltage $= +3/0$ V; input power $=$ 0 dBm) at 2.5 GHz. There is very little difference in the RF characteristics for the switches with copper interconnects and with gold interconnects. The small differences of these two switches were due to the nonuniformity of the wet chemical etch in the gate recess process. The nonuniformity of the wet chemical etch could cause the fluctuation of the ON-state resistance and OFF-state capacitance of the transistors which dominate insertion loss and isolation [7]. It appears from these data that copper metallization does not affect the SPDT HEMT switch performance.

In order to evaluate the temperature-dependent effect on the dc and RF characteristics of the copper-metallized switches, the switches were evaluated at different temperatures. The dc characteristics of the device were measured at different temperatures from 300 K to 500 K. Fig. 7 shows the current–voltage (I–V) characteristics at different high-temperature ambients. The extrinsic transconductance and the drain-to-source current versus the temperature for the copper-metallized SPDT switches were shown in Fig. 8. A drain saturation current density of 188 mA/mm and an extrinsic transconductance of 159 mS/mm at $V_{\rm DS} = 3$ V at 300 K were measured for the devices. While the background carrier concentration from the substrate rises exponentially with temperature, causing the 2-DEG concentration $(n_{\rm 2DEG})$ to increase in the active layer, the carrier velocity ν degraded seriously by the lattice scattering and carrier–carrier scattering mechanisms [13]. Therefore, $I_{\rm DSS0}$ drops at high temperatures due to the enhanced scattering mechanisms even though the carrier concentration increases at high temperatures.

Furthermore, the gate leakage current (I_G) as a function of the gate-to-drain voltage $(V_{\rm GD})$ is shown in Fig. 9. When the gate-to-drain voltage was biased at -22 V, the gate leakage currents were 430, 450, and 490 μA/mm at the temperatures of 300 K, 380 K, and 500 K, respectively. The gate leakage current increases with increasing temperature mainly due to the tunneling mechanism with thermionic emission and partly caused by the reduction of barrier height [14].

Fig. 10 shows that the $V_{\rm th}$ decreases with increasing temperature. The $V_{\rm th}$ of a δ-doped HEMT can be obtained by solving

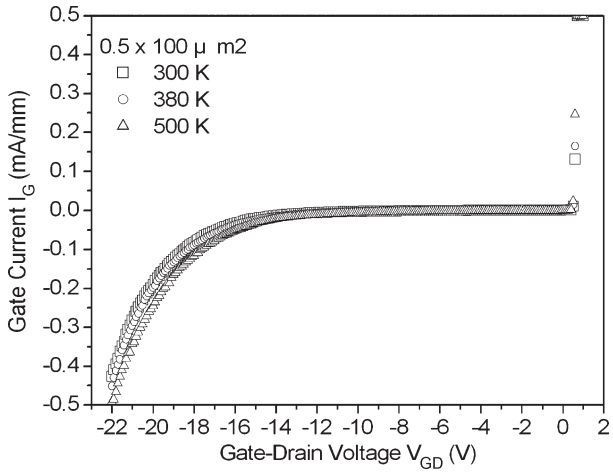

Fig. 9. Gate leakage current (I_G) as a function of the gate-to-drain voltage $(V_{\rm GD})$ for the PHEMTs used in the switches when tested at 300 K, 380 K, and 500 K.

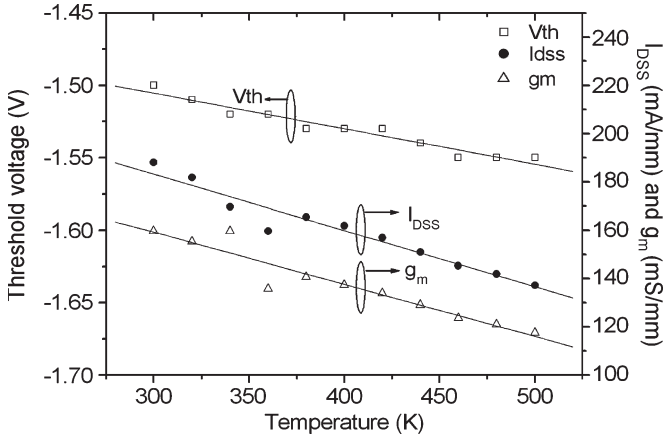

Fig. 10. Threshold voltage $(V_{\rm th})$, drain saturation current density $(I_{\rm dss})$, and extrinsic transconductance (gm) characteristics as a function of temperature for the copper-metallized AlGaAs/InGaAs PHEMT used in the SPDT switches.

the 1-D Poisson's equation (1) as follows [13], [15]:

$$V_{\rm th} = \frac{\Phi_B}{q} - \frac{\Delta E_c}{q} - \frac{n_{\rm 2DEG}(d_d + \Delta d)}{\varepsilon}. \qquad (1)$$

Among the aforementioned parameters, Φ_B is the Schottky gate barrier height, ΔE_c is the conduction-band discontinuity between the Schottky layer and the InGaAs channel, d_d is the distance between the gate and the $n_{\rm 2DEG}$ location, $(d_d + \Delta d)$ is the effective distance between the gate and the $n_{\rm 2DEG}$ location, and ε is the permittivity of the Schottky layer. Based on (1), while the temperature is increased, the threshold voltage decreases owing to the increase of the intrinsic channel carrier concentration $n_{\rm 2DEG}$ [13] and the lowering of the Schottky barrier height Φ_B [16], [17]. Moreover, the decrease of $V_{\rm th}$ is partly caused by the leakage current from a semiinsulating substrate with increasing temperature [14]. Based on the relationship of $V_{\rm th} = V_{\rm th0} - K(T - T_0)$, $V_{\rm th}$ is relatively temperature insensitive. The $V_{\rm th}$ shift from 300 K to 500 K was only -0.05 V, and $\delta V_{\rm th}/\delta T = -0.25$ mV/K as a result.

As shown in Fig. 10, the maximum extrinsic transconductance $(g_{\rm m,max})$ decreases with increasing temperature, which

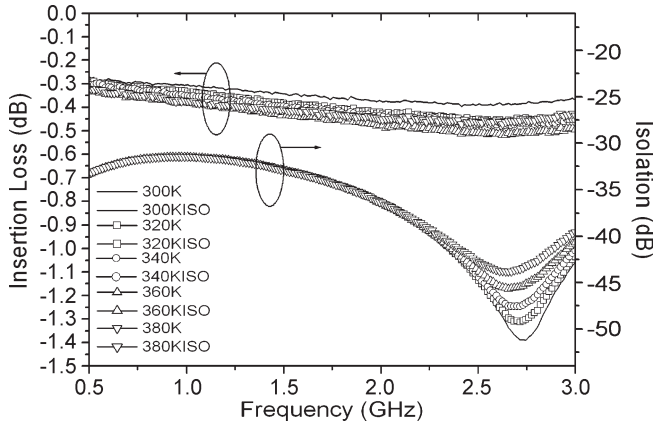

Fig. 11. Insertion loss and isolation versus frequency of the copper-metallized SPDT switches measured from 300 K to 380 K.

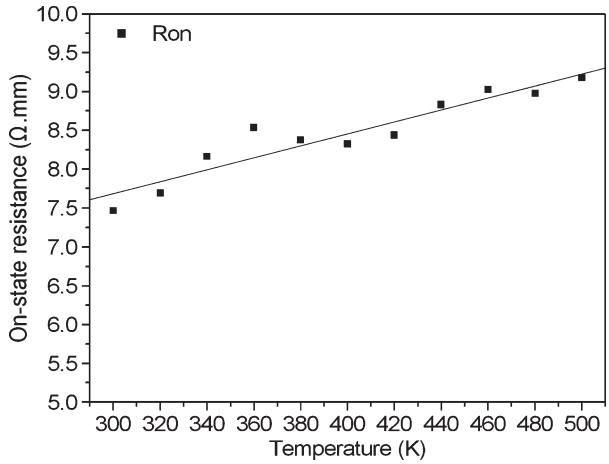

Fig. 12. ON-state resistance as a function of temperature for the SPDT switches.

is attributed to the decrease of the intrinsic transconductance [13] and the increase of the ohmic contact resistance [18], respectively, as the previous reports. Therefore, it can be seen that when the temperature is increased, the degradations of the device performance include the increase of the leakage current and the decrease of the breakdown voltage, threshold voltage, extrinsic transconductance, and drain saturation current density.

Furthermore, RF performances of the device were measured at high temperatures. Fig. 11 shows the insertion loss and isolation versus frequency of the SPDT switches with copper metallization from 300 K to 380 K. The isolation characteristics of the copper-metallized switches degraded slightly because of the increase of the leakage current from the semiinsulating substrate with increasing temperature. For this reason, the isolation is closely related to the OFF-state threshold characteristics which were affected by the leakage current. Although isolation of the copper-metallized switch was influenced by the thermal effect, it still maintained excellent isolation value higher than 35 dB.

In addition, the transistor had a small ON-state resistance which resulted in low insertion loss. However, the ON-state resistances of the copper-metallized switches measured at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 0.5$ V increased gradually from 300 K to 500 K, as shown in Fig. 12. The series resistance increased as

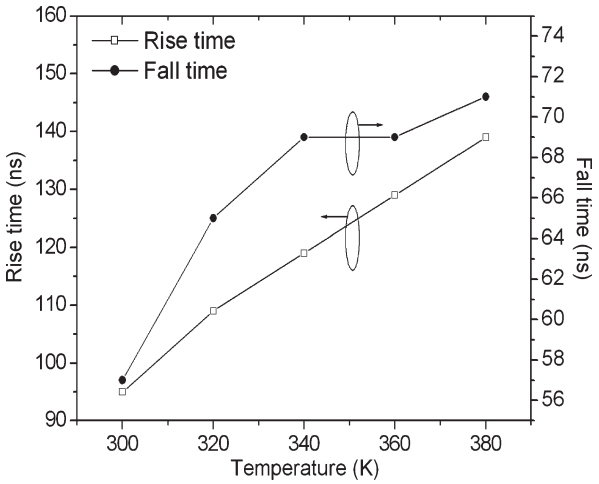

Fig. 13. Switching time as a function of temperature at 2.5 GHz for the SPDT switches.

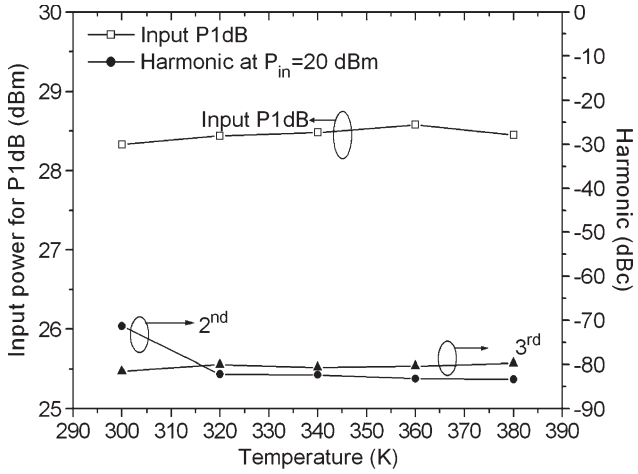

Fig. 14. Input power 1-dB compression and second and third harmonic characteristics for the SPDT switches as a function of temperature when tested at 2.5 GHz.

the source, drain, and gate resistances increased with increasing temperature because of the carrier scattering [19] which would result in the reduction of the carrier transport velocity (υ) and the electron mobility (μ_e) in the channel due to the lattice scattering and carrier–carrier scattering at elevated temperatures [13]. The degradation of ON-state resistance was also caused by the increase of the electrode contact resistance with temperature as verified in the previous reports [20]. This phenomenon led to the slight degradation of the insertion loss, but the increase in the insertion loss from 300 K to 380 K was only 0.08 dB, as shown in Fig. 11. Overall, for high-temperature operation, the copper-metallized switch had an insertion loss of 0.46 dB and an isolation of 42.79 dB (control voltage $= +3/0$ V; input power $= 0$ dBm) when tested at 2.5 GHz at 380 K. It is demonstrated that the copper metallization can be applied to the interconnects of the SPDT switches at high temperatures without affecting the switch performance.

Fig. 13 shows the thermal effect on the switching time for the copper-metallized switches. The switching time increases with increasing temperature primarily due to the degradation of the ON-state resistance.

The power limitation of the switch operation is as explained in [21]–[24], and the maximum input power $P_{\max}$ is expressed as

$$P_{\max} = \frac{(V_C - V_{\rm th})^2}{2Z_0} \tag{2}$$

where Z_0 is the line impedance and V_c is the absolute of the control voltage. It indicates that small threshold voltage and higher control voltage can improve the power handling capability of the FET switch. The input power 1-dB compression and the second and third harmonic characteristics of the copper switches as a function of temperature measured at 2.5 GHz are shown in Fig. 14. The value of the input $P_{1\,\rm dB}$ with different temperatures remained considerably steady because the threshold voltage shift was small and did not influence the power handling capability. The characteristics of the second and third harmonics from 300 K to 380 K under the input power of 20 dBm are shown in Fig. 14. The second and third harmonics

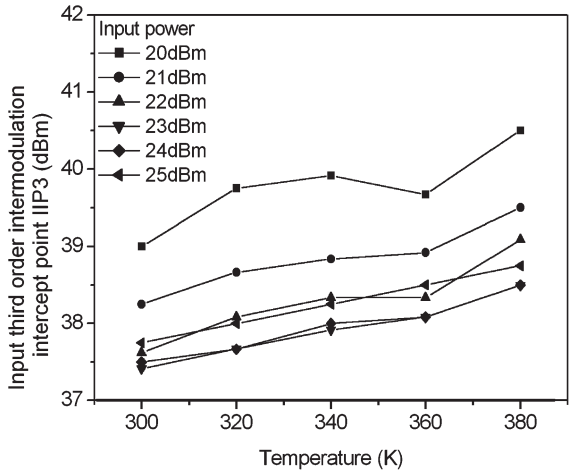

Fig. 15. Input IIP3 as a function of temperature under different input power conditions at 2.5 GHz.

of the device remained quite stable during this temperature range. The harmonic performance is highly associated with power handling capability [25], and the input $P_{1\,\rm dB}$ was kept at about 28.4 dBm in the current case. Fig. 15 shows the input third-order intermodulation intercept point (IIP3) versus different temperatures under several input power conditions. The IIP3 value of the device was kept at different temperatures. IIP3 of 40.5 dBm was achieved at 380 K when the input power was 20 dBm. Based on the aforementioned results, it can be seen that the power handling capability was closely related to the threshold characteristics and that the temperature dependence of the power handling capability was not obviously from 300 K to 380 K.

IV. Reliability Test

The copper-metallized switches were annealed at 250 °C for 20 h in order to test the thermal reliability of the Pt diffusion barrier for long-term period. Although small degradation of the ohmic contact resistance was observed in Fig. 16, the drain saturation current density and the extrinsic transconductance were not obviously influenced after annealing at 250 °C for

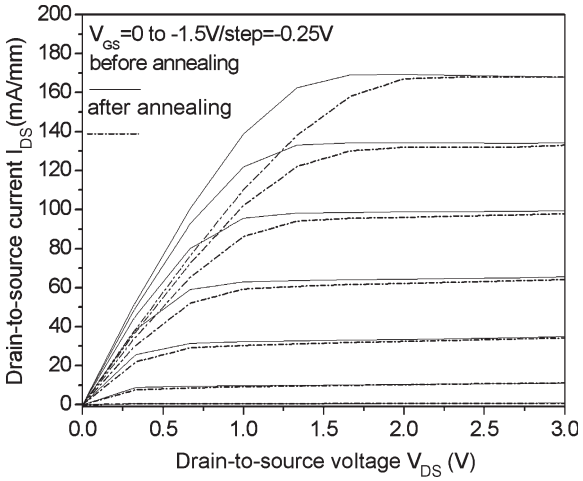

Fig. 16. I–V characteristics of the copper-metallized AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length before and after annealing at 250 °C for 20 h.

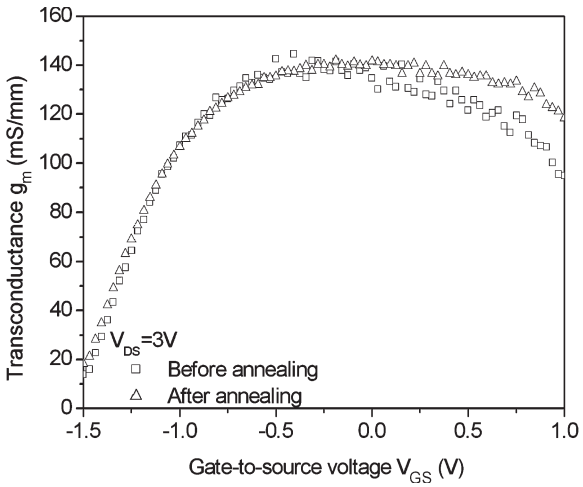

Fig. 17. Extrinsic transconductance versus $V_{\rm GS}$ bias characteristics of the copper-metallized AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length before and after annealing at 250 °C for 20 h.

20 h, as shown in Fig. 17 (less than 1% difference in drain saturation current density and less than 3% difference in extrinsic transconductance). These results indicate that Cu–Pt interconnect layers are quite stable and that platinum is an effective diffusion barrier against copper diffusion after thermal annealing. Thus, the copper-metallized SPDT switches have maintained the electrical performance without any significant change during the high-temperature ambient test.

Fig. 18 shows the output power versus input power of the copper-metallized SPDT switches at 2.5 GHz after annealing at 150 °C under nitrogen atmosphere for different annealing time; the input $P_{1\,\rm dB}$ (input power for 1-dB compression) maintained the same level without any obvious degradation after the long-term test. Hence, the copper-metallized switches demonstrated very good reliability and showed similar switch power handling capability after 144 h of high temperature storage life (HTSL) environment test.

To test the operation reliability of the copper-metallized switches, the copper-metallized switches were subjected to an ON/OFF stress test (control voltage = +3/0 V exchange) for

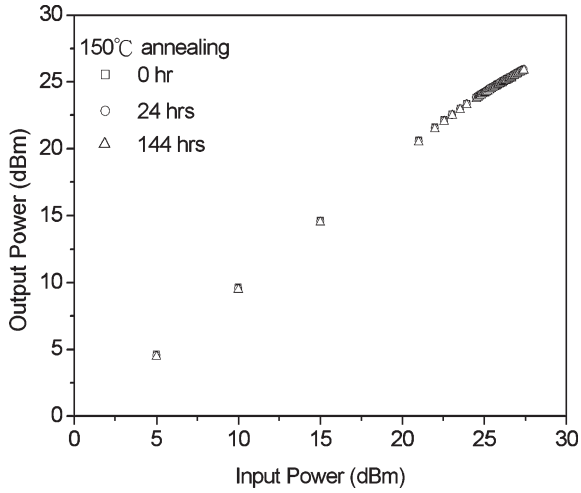

Fig. 18. Output power versus input power of the copper-metallized SPDT switches at 2.5 GHz after annealing at 150 °C for different annealing periods.

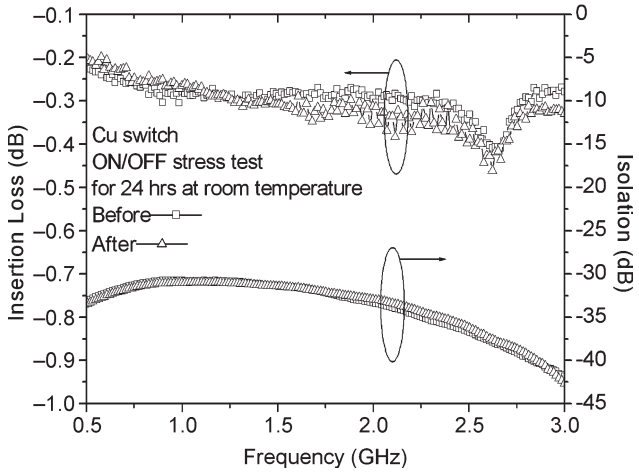

Fig. 19. Insertion loss and isolation versus frequency of the copper-metallized AlGaAs/InGaAs 0.5-μm PHEMT SPDT switches before and after ON/OFF stress test for 24 h at room temperature.

24 h at room temperature. As shown in Fig. 19, the copper-metallized switches showed very little change after the stress test. The insertion loss and isolation still remained stable. Almost no obvious change in the insertion loss and isolation occurred, which indicated that no significant degradation of ON-state resistance and OFF-state capacitance took place. It implies no copper diffusion into the active device region for the transistors after control voltage exchange stress for the copper-metallized SPDT switches using Pt as the diffusion barrier.

V. Conclusion

An SPDT GaAs switch fabricated with copper-metallized interconnects using Pt as the diffusion barrier has been fabricated and investigated. The copper-metallized SPDT switch exhibited an insertion loss of 0.33 dB, a return loss of 23.3 dB, and an isolation of 36.7 dB at 2.5 GHz; the performance is comparable with the performance of the traditional gold-metallized SPDT switches. The input power for 1-dB compression (input $P_{1\,\rm dB}$) of 28.3 dBm at 2.5 GHz was obtained for these switches. Moreover, the temperature-dependent effects on the insertion loss, isolation, switching characteristics, and power handling

capability of the copper-metallized switches using Pt as the diffusion barrier have also been investigated. The RF characteristics of the copper-metallized SPDT switch still remained quite stable and exhibited a low insertion loss of 0.46 dB, an excellent isolation of 42.79 dB, a high input $P_{1\,\mathrm{dB}}$ of 28.45 dBm, and a high IIP3 of 40.5 dBm at 2.5 GHz when tested at 380 K. On the other hand, the high-temperature reliability tests, including thermal stress test (annealing at 250 °C for 20 h) and the HTSL environment test, have also been done; no appreciable change of the dc and RF characteristics was observed for the SPDT switches after these tests. These results show that the copper metallization process using Pt as the diffusion barrier is a very reliable process and can be applied to the GaAs MMIC switch fabrication.

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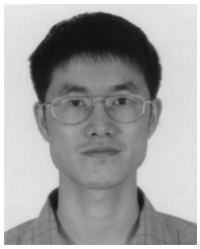

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