A Novel Laser-Processed Self-Aligned Gate-Overlapped LDD Poly-Si TFT

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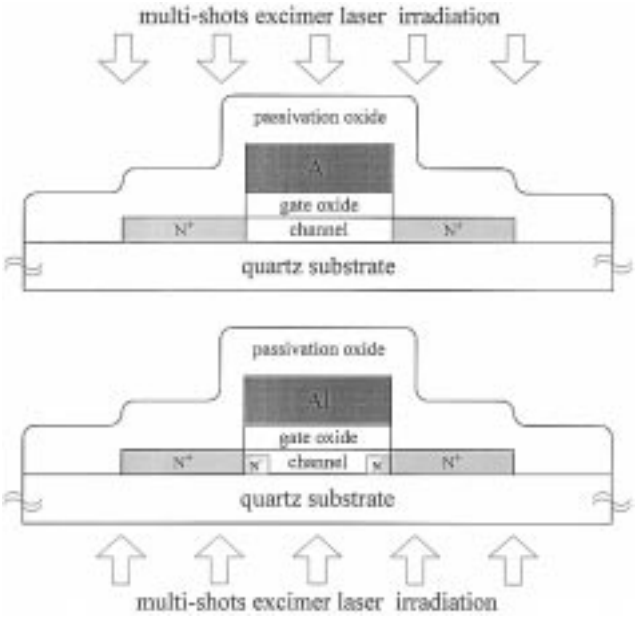
***Abstract*—A novel process for fabricating self-aligned gate-overlapped LDD (SAGOLDD) poly-Si thin film transistors (TFTs) was demonstrated. Laser irradiation for dopant activation was performed from the backside of the quartz wafer. The graded LDD structure was naturally formed under the gate edges due to the lateral diffusion of the dapants during the laser activation. In comparison with the conventional laser-processed self-aligned poly-Si TFTs, the SAGOLDD poly-Si TFTs exhibited lower leakage current, suppressed kink effect, and higher reliability. Moreover, the proposed process was simple and very suitable for low-temperature process.**

***Index Terms*—Excimer laser, poly-Si thin film transistor, self-aligned gate-overlapped LDD.**

I. Introduction

LOW-TEMPERATURE poly-Si (LTPS) TFTs have been widely studied for active matrix displays with integrated circuits, such as AMLCDs and AMOLEDs [1], [2]. For these applications, poly-Si TFTs must possess high performance and reliability while a low-cost selling point is maintained. An offset or lightly doped drain (LDD) structure has been widely used to reduce the leakage current and enhance device reliability by suppressing the electric field near the drain junction [3], [4]. However, it might degrade the device driving capability due to the large series resistance existing in the LDD regions [5]. Recently, gate-overlapped LDD structure has been adopted to suppress the high drain field effects for improving device reliability and reducing leakage current while a high on-state current remains. Many processes have also been proposed to produce the gate-overlapped LDD poly-Si TFTs [5]–[7]. Among them, including nonself-aligned and self-aligned processes, additional processes must be performed, which result in increase of the cost of fabrication. In this letter, we described a novel laser process for producing self-aligned gate-overlapped LDD structure. The process was simple and suitable for low-temperature process.



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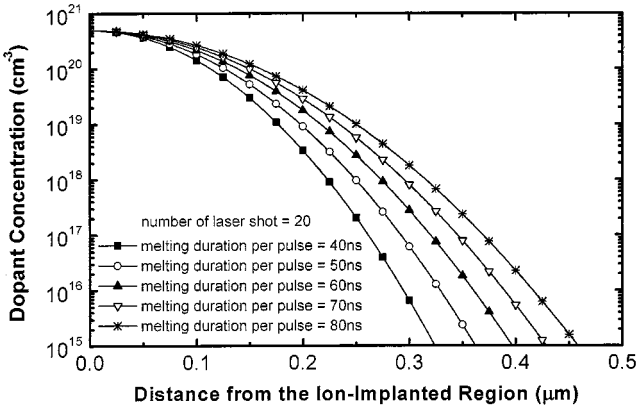

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Fig. 1. (a) The key process for fabricating poly-Si TFTs with self-aligned gate-overlapped LDD (SAGOLDD) structure. For conventional self-aligned (SA) poly-Si TFTs, laser irradiation for dopant activation was performed from the frontside of the substrate, while the proposed laser activation process for SAGOLDD poly-Si TFTs was performed from the backside of the substrate. (b) Estimation of lateral dopant distributions by using Fick's second law for different melting durations per laser pulse. The employed parameters were listed as follows: diffusion coefficient of phosphorus in melting silicon $(D_L) = 10^{-4}$ cm^2/s, number of laser shot $= 20$ and dopant concentration of diffusion source $= 5 \times 10^{20}$ cm^{-3}. The total melting duration $=$ melting duration per laser pulse $\times$ number of laser shot.

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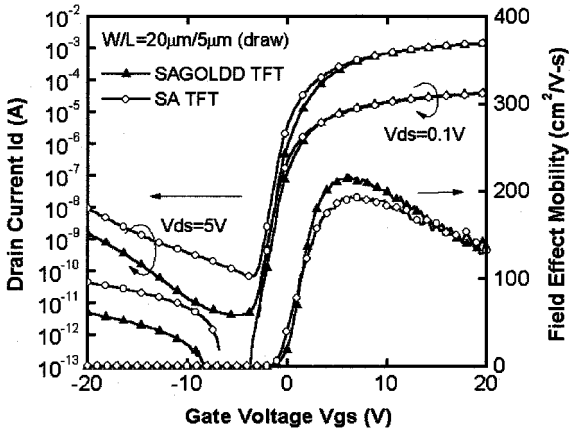

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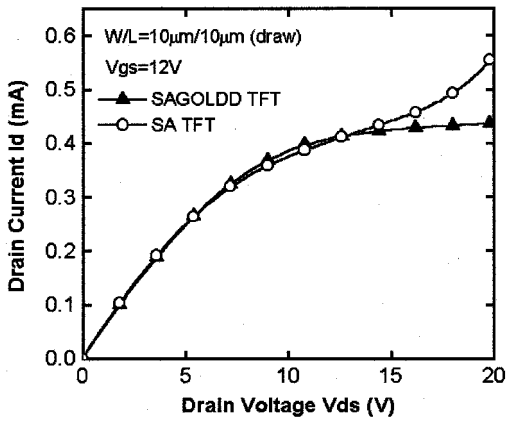
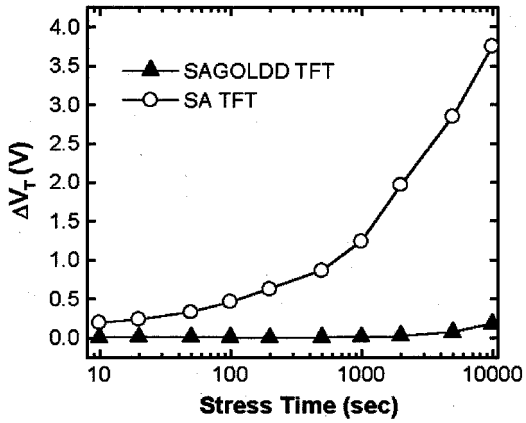


(b)

Fig. 2. Typical current–voltage (I–V) curves of SA and SAGOLDD poly-Si TFTs. (a) Transfer characteristics and (b) output characteristics.



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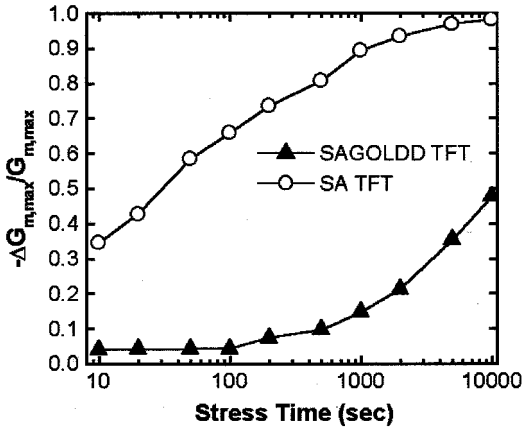

(b)

Fig. 3. Degradation of electrical characteristics in SA and SAGOLDD poly-Si TFTs under the hot carrier stress. (a) Threshold voltage shift ($\Delta V_T \equiv V_{T,\mathrm{final}} - V_{T,\mathrm{initial}}$) and (b) transconductance degradation. The DC stress condition was $V_{\mathrm{ds}} = 15$ V and $V_{\mathrm{gs}} = 4$ V for 10 000 s and device dimension was $W/L = 20\ \mu\mathrm{m}/5\ \mu\mathrm{m}$. Threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-8}$ A at $V_{\mathrm{ds}} = 0.1$ V.

II. Device Fabrication

The key process for producing self-aligned gate-overlapped LDD (SAGOLDD) structure is illustrated in Fig. 1(a). Excimer laser irradiation for dopant activation was performed from the backside of the quartz substrate. For conventional self-aligned (SA) poly-Si TFTs, dopant activation was carried out by excimer laser irradiation from the front-side of the substrate.

The devices were fabricated by the following sequence of processes. At first, a 1000 Å-thick a-Si thin film was deposited on fused quartz substrate by LPCVD at 550 °C. Then the a-Si thin film was crystallized by KrF excimer laser annealing (ELA) at room temperature in a vacuum ambient pumped down to 10^{-3} torr. In this work, ELA process conditions have been optimized to produce large-grain poly-Si thin film with acceptable uniformity. After defining the active device layer, a 1200 Å-thick TEOS gate oxide was deposited by PECVD at 400 °C. A 5000 Å-thick Al thin film was then deposited at room temperature by thermal evaporation for gate electrode. The Al thin film and gate oxide were etched by RIE to form gate electrodes. A self-aligned phosphorous implantation with dose of 5×10^{15} cm^{-2} was carried out to form source and drain regions. Next, a 3000 Å-thick oxide was deposited by PECVD as passivation layer. Dopant activation was carried out by 20-shots excimer laser irradiation from the frontside and backside of the quartz substrate at room temperature for fabricating SA and SAGOLDD poly-Si TFTs, respectively. Contact opening formation and metallization were carried out after dopant activation. Finally, poly-Si TFTs were passivated by 4 h NH_3 plasma treatment for further improving device performance.

III. Results and Discussion

The proposed process used the pulsed excimer laser irradiation not only to crystallize the a-Si thin films but also to activate and diffuse the dopants. The change of doping profile in the melting silicon was the key process to form graded dopant distribution under the gate edges. In principle, Fick's second law could be used in combination with appropriate boundary conditions, diffusion coefficient of phosphorus in melting silicon ($\sim 10^{-4}$ cm^2/s) [8] and melting duration to estimate the lateral doping profile after excimer laser irradiation. When lateral doping profiles were estimated, the ion-implanted regions were treated as the source effectively maintaining a constant value of dopant concentration during diffusion process. Since the diffusion coefficient of the phosphorus atoms in melting silicon is much greater than that in the solid, solid-state diffusion during the ultrafast heat cycle is negligible. Fig. 1(b) displays an estimation of lateral dopant distributions under the gate edges after laser activation.

In this work, when laser irradiation was applied from the backside of the quartz substrate, laser energy density was controlled in the region of partially melting the channel poly-Si thin film in order to maintain the large grains in the channel. If higher laser energy density had been applied to completely melt the poly-Si thin film, the large grains in the channel would be destroyed because of the metal gate acting as a heat sink, which was similar to laser crystallization applied to bottom-gate TFTs. As a result, similar quality of channel poly-Si layers should exist in SA and SAGOLDD poly-Si TFTs, excluding lateral dopant diffusion and recovery of implantation damage under the gate edges occurring in SAGOLDD poly-Si TFTs. The transmittance of the quartz substrate for KrF (248 nm) excimer laser was beyond 95%, as a result, most of laser energy could be absorbed by Si thin film without degrading the substrate. For this process applied to glass substrate, pulsed laser with longer wavelength, such as XeCl (308 nm), XeF (353 nm) excimer laser and solid-state pulse laser, could be adopted [9], [10].

Another advantage of this process was its capability of recovery of crystal damage under the gate edges caused by high-energy ion implantation. For conventional laser activation, this kind of damage could not be recovered due to the reflection of laser light by the metal gate, and would degrade the TFTs' performance [12].

The typical n-channel transfer characteristics and output characteristics of SA and SAGOLDD LTPS TFTs are shown in Fig. 2(a) and (b), respectively. The SAGOLDD poly-Si TFT exhibited lower leakage current and suppressed kink effect compared to the SA poly-Si TFT due to the reduction of drain field [11]. The mobility and on/off current ratio at $V_{\rm ds} = 5$ V of SAGOLDD poly-Si TFT were above 200 cm^2/V-s and 10^8, respectively. Slightly higher mobility of SAGOLDD poly-Si TFT might be attributed to the shortening of effective channel length resulting from the lateral dopant diffusion. Another possible reason might be the recovery of little implantation damage under the gate edges occurring in SAGOLDD poly-Si TFT. In this work, TFT with 1-μm channel length could work at low drain voltage, that is, the LDD length should be below 0.5 μm. Hot carrier stress was used to test the long-term reliability of poly-Si TFTs in our experiments. The dc stress condition was $V_{\rm ds} = 15$ V and $V_{\rm gs} = 4$ V for 10 000 s and device dimension was $W/L = 20\ \mu{\rm m}/5\ \mu{\rm m}$. An investigation has been shown that such a bias condition was a severe reliability testing condition [13]. Fig. 3(a) and (b) show the threshold voltage shift and transconductance degradation of SA and SAGOLDD poly-Si TFTs. Due to reduction of drain field in SAGOLDD structure, the SAGOLDD poly-Si TFT also exhibited much better hot carrier stress endurance in comparison with the SA poly-Si TFT [14].

IV. Conclusion

The SAGOLDD LTPS TFTs with high performance and reliability were successfully fabricated using a novel laser activation process. The proposed new process was simple and attractive for low-temperature process on transparent substrates.

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