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Characterization of Si/SiGe Heterostructures on Si Formed by Solid Phase Reaction

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We have characterized the $Si/Si_{0.6}Ge_{0.4}$ heterostructure formed by two-step solid-phase reaction. Single crystalline behavior is evidenced by X-ray diffraction. In sharp contrast to conventional strain-relaxed SiGe, an extremely smooth surface close to the Si substrate is measured by cross-sectional transmission electron microscopy and atomic force microscopy. Good material quality is further evidenced from the near identical current-voltage characteristics for thermal oxide grown on $Si/Si_{0.6}Ge_{0.4}$ and on the Si control sample.
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Although silicon-germanium (SiGe) heterostructures[1-11] on silicon (Si) have been studied extensively, one difficult challenge to integration of strained SiGe into current Si complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) processes is the low temperature ($T < 800°C$)[12] required to avoid strain relaxation and defect generation. This is because SiGe is generally grown by a low pressure chemical vapor deposition (LPCVD) at low temperature but current CMOS process must use a high temperature annealing for dopant activation after source-drain ion implantation.[12] Unfortunately, strain will be relaxed at high temperatures and may degrade the device performance by forming rough surface and pinholes.[4-8] In addition to low dopant activation, the low temperature restriction for strained SiGe also degrades gate oxide integrity, increases source-drain junction leakage, and is incompatible to modern high dielectric constant gate dielectrics.[13-14] Therefore, strain-relaxed SiGe has attracted much attention recently, but the strain relaxation related rough surface still prohibits further application of SiGe to current Si CMOS technology.[9-11] Recently, we have developed a strain-relaxed SiGe using a new high temperature solid phase reaction method; good integrity of p-MOSFET is obtained.[15-16] In this paper, we have characterized the Si/SiGe heterostructures on Si substrate by two-step solid-phase reaction. Good material quality is revealed by X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (XTEM). The primary advantage of this simple method is the full compatibility to the existing Si ultralarge-scale integration (ULSI) technology without the constraint of low temperature processing or alternating the performance of Si CMOS devices.

Experimental

Standard Si wafers of 10 Ω cm resistivity were used in this study. After a standard RCA clean, HF vapor passivation is used to suppress the native oxide formation before Ge deposition.[14-18] An amorphous Ge layer of 120 Å is selectively deposited by lithography in active region to form a single crystalline $Si_{0.3}Ge_{0.7}$ layer[15] by rapid thermal annealing (RTA) at 900°C for 60 s. More detailed material characterization can be found in our previous study.[15] Then Si/SiGe heterostructure is formed by a 150 or 300 Å amorphous Si deposition and subsequent RTA, while the thicker Si is used for material analysis and the thinner one is for device characterization.

MOS capacitors were fabricated by growing a 30 Å thermal oxide at 900°C, a 3000 Å poly-Si deposition, phosphorus doping, Al metallization, and patterning. XRD, cross-sectional TEM, secondary ion-mass spectroscopy (SIMS), capacitor leakage current, and capacitance-voltage (C-V) measurements are used to characterize the material property Si/SiGe heterostructure.

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Results and Discussion

Figure 1 shows the XRD spectra of one-step formed $Si_{0.3}Ge_{0.7}$ and two-step formed Si/SiGe heterostructure by solid-phase reaction. The comparable sharp and strong XRD peaks for $Si_{0.3}Ge_{0.7}$ and $Si_{0.6}Ge_{0.4}$ with Si substrate indicates a single crystalline and high quality $Si_{0.6}Ge_{0.4}$, where the single crystalline $Si_{0.3}Ge_{0.7}$ is previously demonstrated.[15] A Ge composition of 0.4 was obtained in Si/SiGe heterostructure from the relative XRD peak position to Si substrate. The composition change from $Si_{0.3}Ge_{0.7}$ to $Si/Si_{0.6}Ge_{0.4}$ may be due to additional Si supplied from top Si layer that dilutes the Ge content.

We have used XTEM to further characterize the top Si layer of the $Si/Si_{0.6}Ge_{0.4}$ heterostructure. As shown in Fig. 2, two uniform layers are observed on Si substrate and form the $Si/Si_{0.6}Ge_{0.4}$ heterostructure. No polycrystalline grain can be observed in XTEM that is consistent with the narrow and sharp XRD peak shown in Fig. 1. Good material quality is evidenced by the smooth surface, smooth interface, and almost defect free $Si/Si_{0.6}Ge_{0.4}$ heterostructure. In combination of smaller thickness of Si top layer with Ge composition decreasing after solid-phase reaction, the mechanism of second-step reaction is due to the intermixing of top Si with underneath SiGe. Further, TEM, shows that the formed $Si_{0.6}Ge_{0.4}$ and the remaining top Si layers are ~300 and ~160 Å that are in close agreement with the calculated data from the following reaction equations

$$0.3Si + 0.7Ge \rightarrow Si_{0.3}Ge_{0.7} \quad [1]$$

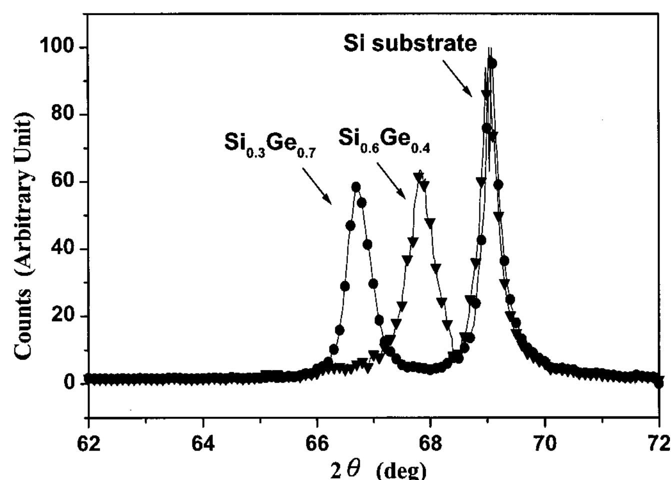

Figure 1. XRD spectra of one-step formed $Si_{0.3}Ge_{0.7}$ and two-step formed $Si/Si_{0.6}Ge_{0.4}$ heterostructure by solid-phase reaction.

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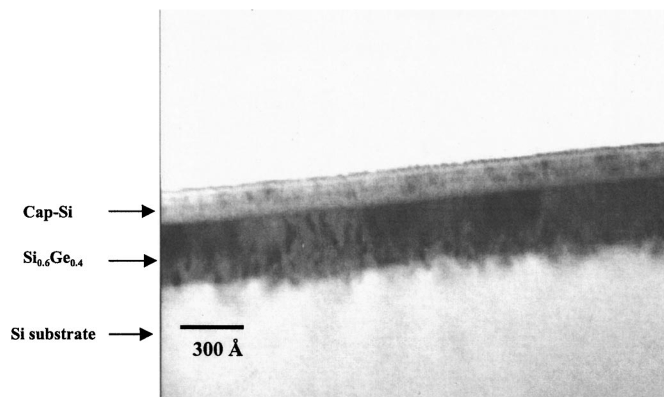


Figure 2. Cross-sectional TEM of the $Si/Si_{0.6}Ge_{0.4}$ heterostructure.

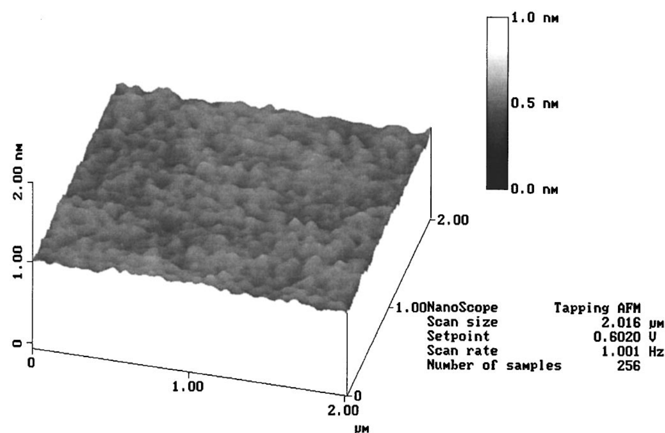
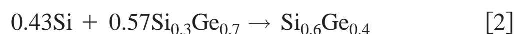


Figure 4. AFM surface topography of the $Si/Si_{0.6}Ge_{0.4}$ heterostructure.



$$0.43Si + 0.57Si_{0.3}Ge_{0.7} \rightarrow Si_{0.6}Ge_{0.4} \quad [2]$$

According to Eq. 1, a 120 Å deposited Ge will form a 170 Å $Si_{0.3}Ge_{0.7}$. From Eq. 2, the $Si_{0.3}Ge_{0.7}$ in turn gives a 300 Å $Si_{0.6}Ge_{0.4}$ and a remaining top 170 Å Si layer. The good agreement between calculated and transmission electron microscopy (TEM) measured data again suggests that the top Si layer is the main source of Si for $Si_{0.6}Ge_{0.4}$. This is reasonable because the top amorphous Si layer has weaker bonding than bottom single crystalline Si or $Si_{0.3}Ge_{0.7}$ layers.

We have further measured the composition profile of $Si/Si_{0.6}Ge_{0.4}$ heterostructure. As shown in Fig. 3, a uniform composition of SiGe measured by SIMS is consistent with the sharp XRD peak in Fig. 1. A thin Si layer at top surface with very low Ge is also observed that suggests the composition transition from $Si_{0.3}Ge_{0.7}$ to $Si/Si_{0.6}Ge_{0.4}$ originated from top Si. The long graded Ge composition tail adjacent to uniform $Si_{0.6}Ge_{0.4}$ may be due to Ge diffusion into Si substrate. Because the graded Ge profile is naturally formed during the solid-phase reaction, it is important for strain relaxation of the uniform $Si_{0.6}Ge_{0.4}$ layer and achieving a smooth $Si/Si_{0.6}Ge_{0.4}$ interface in Fig. 2.

Because the device performance of the MOSFET is directly related to the surface roughness before and after oxidation,[14,18] we have used atomic force microscopy (AFM) to further measure the surface roughness of Si/SiGe heterostructure. The top Si layer calculated from above equations is about 20 Å. As shown in Fig. 4, a root-mean-square (rms) value of 1.5 Å is measured that is close to the original Si surface value of 1.2 Å. The small rms roughness is also consistent with the smooth surface observed by TEM. To our best knowledge, this is the smoothest surface of strain relaxed Si/SiGe that can be used for further device application.

We have further characterized the $Si/Si_{0.6}Ge_{0.4}$ heterostructure by measuring the capacitor leakage current. As shown in Fig. 5, almost identical I-V characteristics are obtained for 30 Å thermal oxides grown on both $Si/Si_{0.6}Ge_{0.4}$ and Si that suggests the excellent quality of oxide grown on $Si/Si_{0.6}Ge_{0.4}$ heterostructure. The comparable electrical characteristics with Si control sample is because the thermal oxide is grown on top Si instead of on SiGe that avoids the weak GeO_x inside the SiO_2 matrix.[1-2]

The quality of oxide grown on $Si/Si_{0.6}Ge_{0.4}$ heterostructure is further examined by the C-V characteristics. Figures 6a and b show the measured high and low frequency C-V curves and interface trap density (D_{it}) plot, respectively. The D_{it} as a function of energy is obtained directly from measured C-V data. The close match between high and low frequency capacitance values indicates the high oxide quality with low bulk and interface defects. This is further evidenced from the low minimum interface trap density of $6 \times 10^{10}\ eV^{-1}/cm^2$, which is already good enough for MOSFET applications.[14]

Conclusions

We have demonstrated a simple method to fabricate Si/SiGe heterostructure with good material quality, which is fully compatible

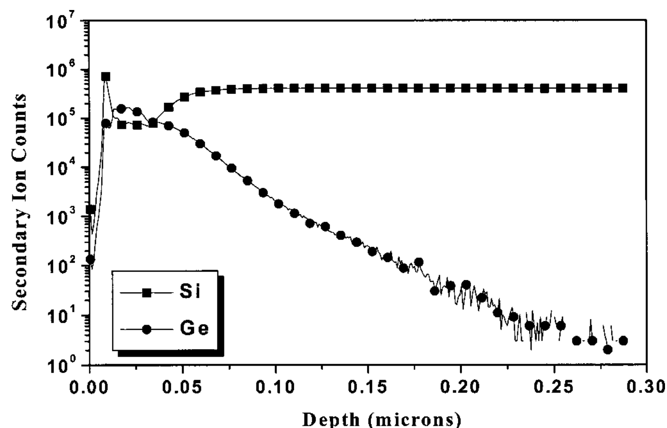


Figure 3. SIMS profile of the $Si/Si_{0.6}Ge_{0.4}$ heterostructure.

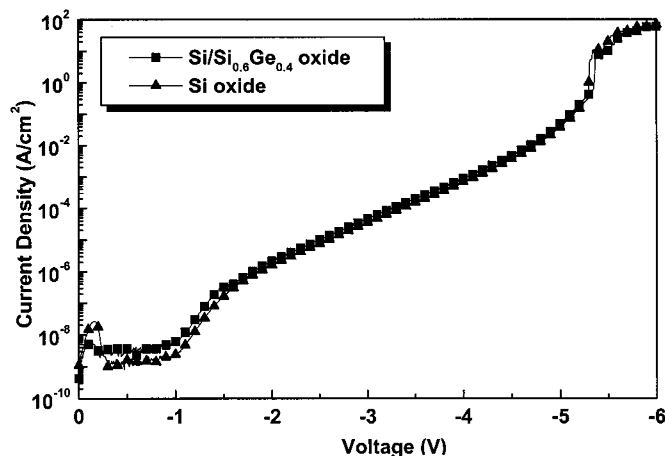


Figure 5. I-V characteristics of 30 Å thermal oxide grown on Si and $Si/Si_{0.6}Ge_{0.4}$.

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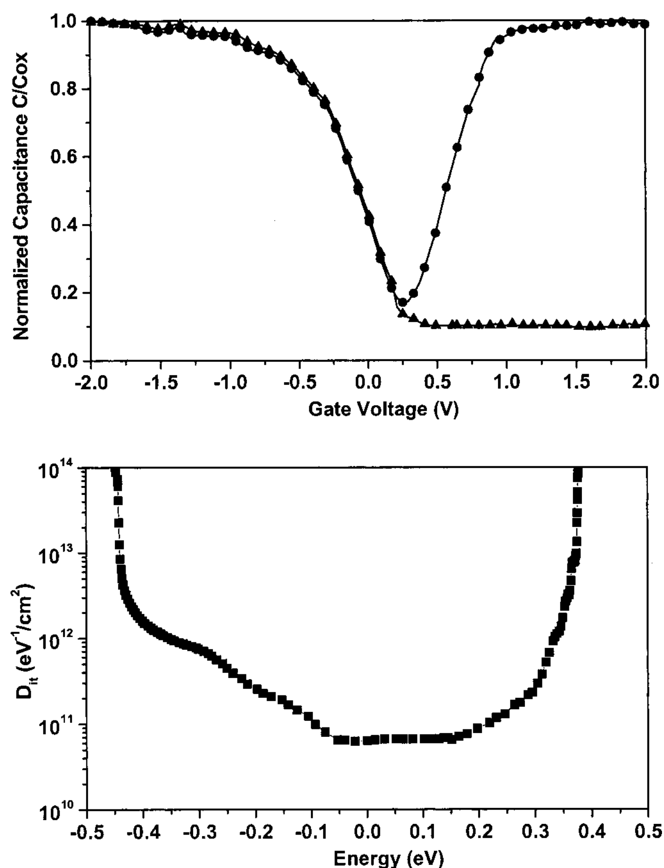

Figure 6. (a, top) C-V characteristics and (b, bottom) interface trap density plot of 30 Å thermal oxide grown on Si and $Si/Si_{0.6}Ge_{0.4}$.

to the existing Si CMOS technology. The excellent oxide quality grown on Si/SiGe is evidenced from the almost identical oxide leakage current with control thermal SiO_2, which can be further used for p-MOSFET application.

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