Ambipolar Schottky-Barrier TFTs

Horng-Chih Lin, *Senior Member, IEEE*, Kuan-Lin Yeh, Tiao-Yuan Huang, *Fellow*, Ruo-Gu Huang, *Student Member, IEEE*, and Simon M. Sze, *Life Fellow, IEEE*

***Abstract*—A novel Schottky-barrier metal-oxide-semiconductor thin-film transistor (SBTFT) was successfully demonstrated and characterized. The new SBTFT device features a field-induced-drain (FID) region, which is controlled by a metal field-plate lying on top of the passivation oxide. The FID region is sandwiched between the silicided drain and the active channel region. Carrier types and the conductivity of the transistor are controlled by the metal field-plate. The device is thus capable of ambipolar operation. Excellent ambipolar performance with on/off current ratios over 10^6 for both p- and n-channel operations was realized simultaneously on the same device fabricated with polysilicon active layer. Moreover, the off-state leakage current shows very weak dependence on the gate-to-drain voltage difference with the FID structure. Finally, the effects of FID length are explored.**

***Index Terms*—Ambipolar, field-induced drain, Schottky barrier, TFT.**

I. INTRODUCTION

SCHOTTKY barrier (SB) MOS transistor, which employs metallic source and drain [1], eliminates the source/drain (S/D) implantation and subsequent annealing steps. It is therefore simpler in processing and inherently suitable for low temperature processing. It is also excellent in short-channel effect control, due to the inherently shallow silicide junction [2], [3]. Moreover, it is also capable of bichannel operation [4]. With these advantages, it thus appears to be quite attractive for applications to nanoscale devices as well as large-area electronics.

Conventionally, SB MOS devices employ a self-aligned silicidation (salicide) process to form the silicided S/D. Gate sidewall spacers are required to avoid bridging between the gate electrode and the silicided S/D [1]–[7]. However, the resultant SB MOS transistors generally suffer from severe leakage current and poor on/off current ratio. This is due to the much larger junction leakage current inherent in Schottky diodes, compared to p-n junction diodes. Another shortcoming is that it is almost impossible to fabricate SB MOS transistors with acceptable n- and p-channel characteristics simultaneously for ambipolar operation [4]. This is due to the constraint imposed by the fixed barrier height of the Schottky contact of a given metallic layer.

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H.-C. Lin and S. M. Sze are with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. (e-mail: hclin@ndl.gov.tw).

K.-L. Yeh and R.-G. Huang are with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

T.-Y. Huang is with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. and also with National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

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In this work, we have demonstrated a novel poly-Si Schottky barrier thin-film transistor (SBTFT) device that can effectively improve the on/off current [8]–[11]. The new device employs a field-plate (or subgate) to induce an electrical drain extension in the active poly-Si layer. The unique field-induced drain (FID) feature reduces the off-state leakage effectively while maintaining a reasonable on-current value, resulting in significant improvement in the device performance. Excellent ambipolar operations were demonstrated, for the first time, on the same SBTFT with FID structure.

II. DEVICE FABRICATION

Detailed fabrication steps have been previously described [8], [9]. Fig. 1(a) and (b) show key processing steps for devices with the conventional and FID structure, respectively. Briefly, Si wafers capped with a thermal oxide layer were used as the starting substrates. A 50-nm amorphous Si active device layer was deposited at 550 °C by low-pressure chemical vapor deposition (LPCVD), and subsequently crystallized by a solid-phase re-crystallization (SPC) treatment at 600 °C in N_2 for 24 h. After patterning the active device region, a 20-nm CVD gate oxide layer and a n^+ poly-Si (200 nm) layer were deposited. The n^+ poly-Si gate layer was delineated to form the main gate. Next, a 200-nm CVD oxide layer was deposited, followed by lithographic step to define the offset regions for the new TFT device with FID [Fig. 1(b)] Self-aligned sidewall spacers were simultaneously formed for the conventional devices during the reactive-ion-etching step used to define the offset regions in the new devices [Fig. 1(a)] Next, silicided S/D was formed by a self-aligned silicidation (salicidation) treatment, by first depositing a thin Co layer (15 nm, capped with 30 nm of TiN), followed by a rapid-thermal annealing step (550 °C, 30 s) and a wet etching step in H_2SO_4:$H_2O_2 = 3:1$ to remove the non-reacted metals. It should be noted that neither the channel nor the S/D region received any deliberate doping, so no post-implant annealing step was required. Wafers then followed a standard back-end processing to completion. The metal subgate in the new structure was formed simultaneously with the regular metal patterning, so no extra processing steps were required. A plasma treatment at 250 °C in NH_3 for 1 h was performed before measurements.

III. OPERATION OF SBTFT WITH FIELD-INDUCED DRAIN

The new structure [Fig. 1(b)] features an undoped Si active channel, a top metal field-plate (i.e., the subgate), and Schottky S/D. For device operation, a fixed bias is applied to the subgate to form a FID extension under the subgate region. So depending on the subgate bias polarity, the device can function as either an

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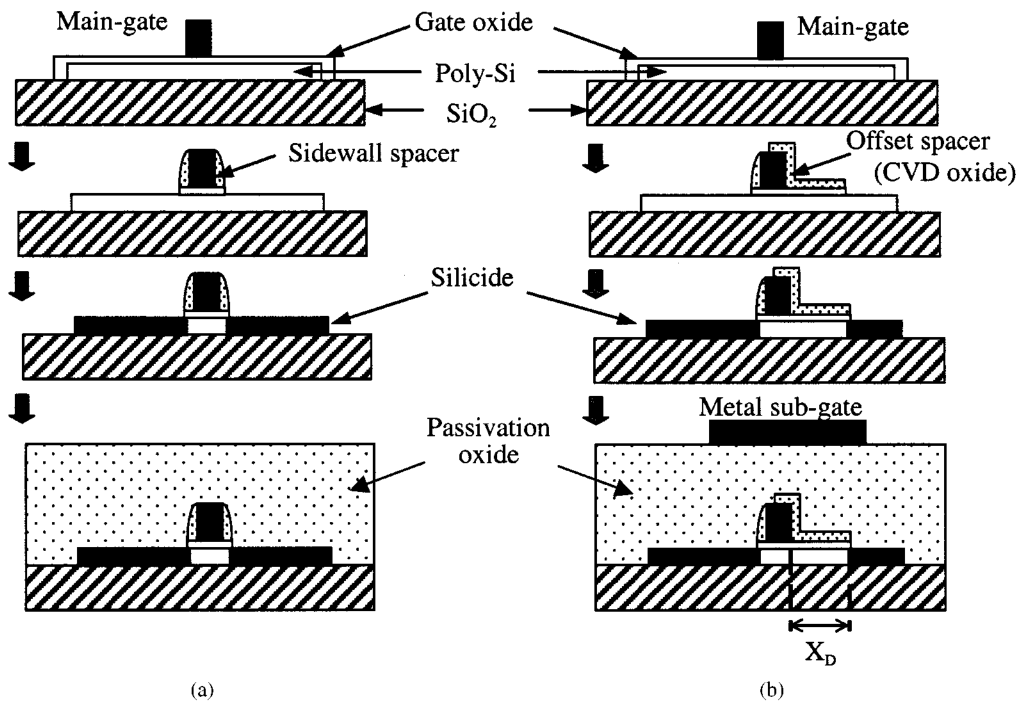

Fig. 1. Key fabrication steps for SBTFT devices with (a) conventional and (b) the new structure with field-induced drain (FID). X_D in (b) is the length of FID region in the channel.

n-channel transistor with positive subgate bias, or a p-channel transistor with negative subgate bias.

The new device is structurally similar to conventional SB MOSFETs [1]–[7], except that a FID extension is created between the channel and the Schottky drain. The FID extension serves to reduce the undesirable off-state leakage that has plagued all previous SB MOSFETs. Concomitantly, the new device can also be viewed as MOSFETs with FID [12], [13], with the exception that the heavily-doped S/D region is now replaced by Schottky S/D. The new structure thus retains all the advantages of FID such as low off-state leakage and low junction leakage. Finally, the use of Schottky S/D can greatly reduce processing steps (i.e., implant and subsequent annealing), and allows ambipolar operation, which further simplifies CMOS process integration.

IV. Results and Discussion

A. Characteristics of Ambipolar Operation

Fig. 2 depicts the ambipolar operation of the FID SBTFT [8]. Excellent on/off current ratios of over 10^6 are achieved for both n- and p-channel operations under proper bias conditions. It is interesting to note here that the turn-on behavior is somewhat retained for n-channel operation even when a zero sub-gate bias is applied. Meanwhile, the off-state leakage in p-channel operation is higher for subgate bias of zero volt than that of −50 V. These phenomena will be addressed later.

Fig. 3 compares the ambipolar (i.e., both n- and p-channel) subthreshold characteristics of the conventional and FID SBTFTs. It can be seen that SBTFT with conventional structure exhibits very poor performance for both p- and n-channel modes of operation [Fig. 3(a)]. On/off current ratios are around or less than 10^3. Moreover, the strong gate-induced drain leakage (GIDL)-like leakage current results in the V-shaped current-voltage *(I–V)* curves. In contrast, superior p- and n-channel device performances are simultaneously realized on the SBTFT with FID structure under proper sub-gate biases. As shown in Fig. 3(b), on/off current ratio as high as 10^6 is observed for both n- and p-channel modes of operation. In addition, the GIDL-like leakage current is effectively suppressed. It should be emphasized that these characteristics are obtained on the same device by simply changing the polarity of the sub-gate bias.

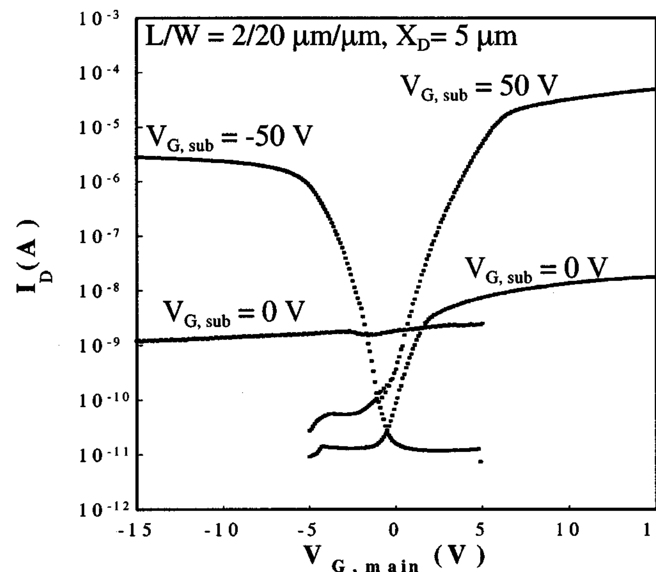

Fig. 2. Ambipolar subthreshold characteristics of a FID SBTFT. V_D is 5 and −5 V for n- and p-channel operations, respectively.

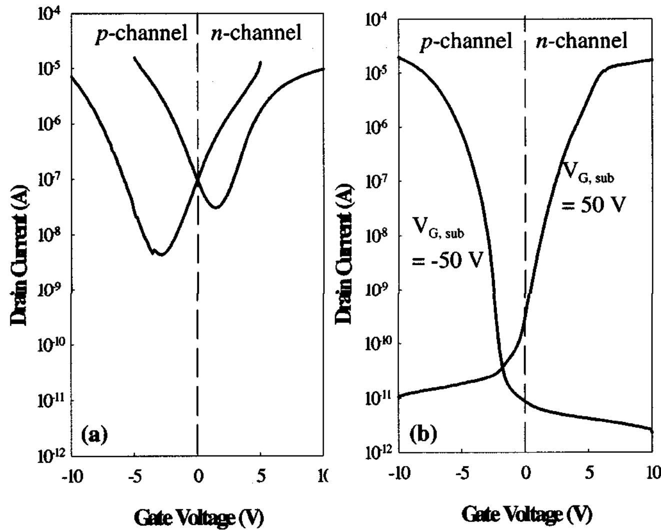

Fig. 3. Typical p- ($V_D = -5$ V) and n-channel ($V_D = 5$ V) subthreshold characteristics of SBTFT with (a) conventional and (b) FID structure. $L/W = 2/20$ μm/μm. X_D in (b) is 1 μm.

Output characteristics of the two types of devices are shown in Fig. 4. It is seen that the implementation of FID in the device improves the on-state currents for both p- and n-channel operations. The improvements can be ascribed to the elimination of the ungated channel regions existing under the sidewall spacers in the conventional devices. Since the bottom width of the sidewall spacers (~150 nm) is larger than the silicide thickness (~55 nm), the silicided S/D portion does not reach the channel region beneath the main-gate, leading to an increase in the parasitic resistance along the channel in the conventional device. This feature is quite different from that of SB MOS devices reported previously [4]–[7], in which the silicided S/D region overlaps with the gate. Although a self-aligned sidewall spacer also exists at the source side of our new device, however, the overlying metal subgate effectively covers the channel region underneath the spacer, so the parasitic resistance is reduced when a high subgate bias is applied. This phenomenon will be addressed in more detail later.

B. Leakage Mechanisms

As mentioned earlier, the GILD-like leakage current is also effectively eliminated, further highlighting the effectiveness of FID. A more detailed study on the conduction mechanisms of the leakage current was reported elsewhere [11]. Here, we briefly present qualitative conduction mechanisms with the band diagrams shown in Fig. 5 to explain the effectiveness of FID in reducing the leakage. In the figure, we concentrate only on the n-channel operation. Similar results could also be deduced for p-channel operation. For the conventional device, a high electric field is developed in the channel region near the drain side [Fig. 5(a)]. Such a high field would enhance the field emission as well as thermionic emission of holes from the silicided drain. On the other hand, formation of the FID with the band diagram shown in Fig. 5(b) tends to suppress the emission of holes from the drain. As a result, GIDL-like leakage could be eliminated.

C. Effects of FID Length

The n- and p-channel subthreshold characteristics for devices with a fixed main-gate length (e.g., 3 μm) but different X_D ranging from 1 to 10 μm are shown in Figs. 6 and 7, respectively. It can be seen that the leakage currents in the off-state and the subthreshold regions are essentially independent of the FID length. On the other hand, the on-state current increases as X_D becomes shorter. This trend is reasonable, since the parasitic resistance decreases with decreasing X_D. Nevertheless, the dependence on X_D is much stronger for the p-channel operation.

In Figs. 8 and 9, the drain currents for n- and p-channel operations are shown as a function of the subgate voltage. Devices with different X_D ranging from 1 to 6 μm were characterized. Drain voltages were 3 and $-$ 3 V for n- and p-channel operations, respectively. Two main-gate voltages $V_{G,\text{main}}$ were measured for each operation mode, i.e., 10 and 0 V for the n-channel and $-$ 10 and 0 V for the p-channel, to represent the "on" and "off" states, respectively. When a large $|V_{G,\text{main}}|$ was applied, the *I-V* curves in Figs. 8 and 9 could be regarded as the operation of FETs with the metal field-plate (or the subgate) serving as the transistor gate, while X_D became the transistor channel length, since the channel region underneath the main-gate acted simply as a "pseudo source".

V_{th} extracted from the "on" *I–V* curves of Figs. 8 and 9 is shown in Fig. 10 as a function of X_D. It is seen that the absolute value of V_{th} in long-channel (i.e., large X_D) devices is larger for p-channel operation mode. In addition, the short-channel effects (i.e., V_{th} roll-off shown in Fig. 10 and subthreshold punchthrough shown in Figs. 8 and 9) are much more severe for n-channel operation.

The asymmetrical V_{th} values for long-channel p- and n-channel operations can be ascribed to the existence of positive fixed charge normally observed at the oxide/Si channel interface [14]. However, this alone can not explain the asymmetrical short-channel effects shown in Fig. 10. Since n-channel operation shows much more severe short-channel effects, it strongly suggests that the background doping in our channel is n-type! After carefully reviewing the process history used in the device fabrication, we indeed found that the solid-phase crystallization (SPC) step was performed in a furnace previously used for n^+ diffusion. This reasonably explains the n-type background doping found in the channel, and illustrates the importance of carefully controlling the process environment, as it could significantly influence the device operation.

The n-type background doping in the channel can also explain the results shown in Figs. 6 and 7. As mentioned above, the on-state current for p-channel operation shows a much stronger dependence on the FID length, compared to the n-channel operation. This is because during the p-channel operation, conduction of holes in the offset channel is confined in the narrow inversion layer near the channel/oxide interface. In contrast, cross-sectional width for conduction of electrons in the offset channel during n-channel operation is wider due to the n-type background doping. The former case thus shows a stronger dependence on the FID length.

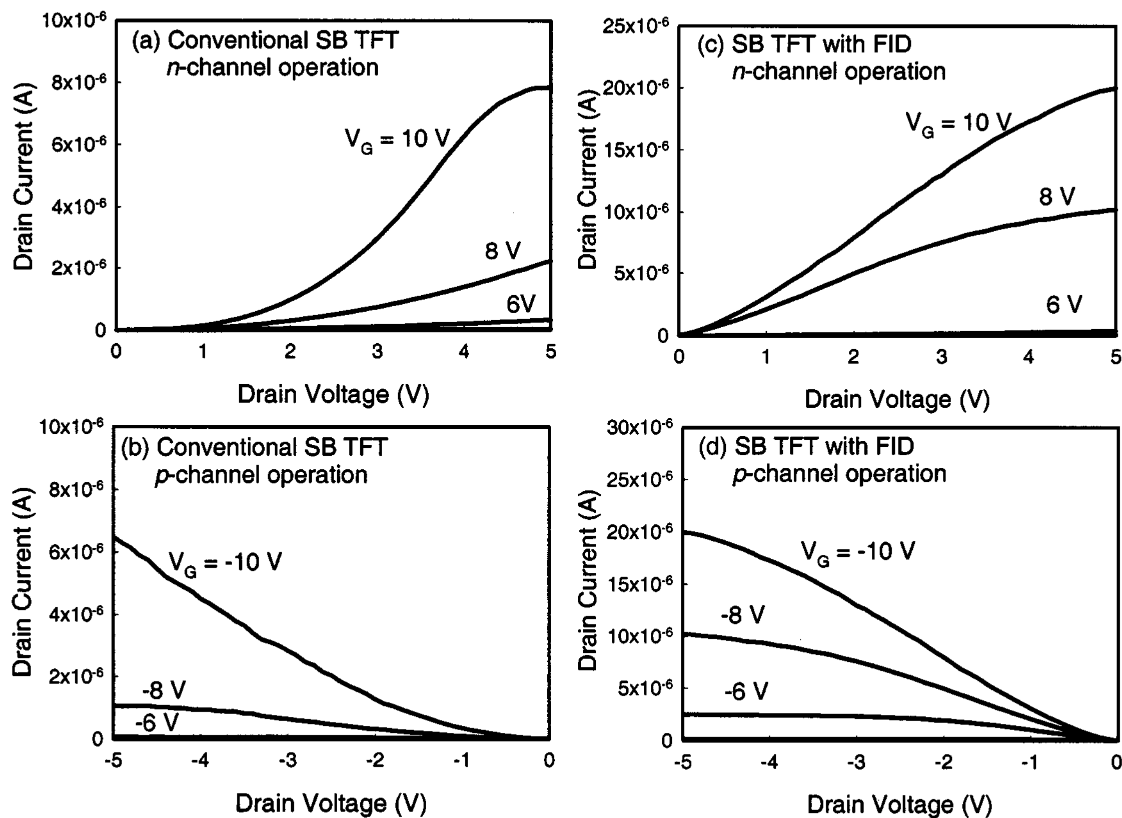

Fig. 4. Typical p- and n-channel output characteristics of SBTFT with (a) and (b) conventional and (c) and (d) FID structure. $L/W = 2/20\ \mu$m/μm. X_D in (c) and (d) is 1 μm.

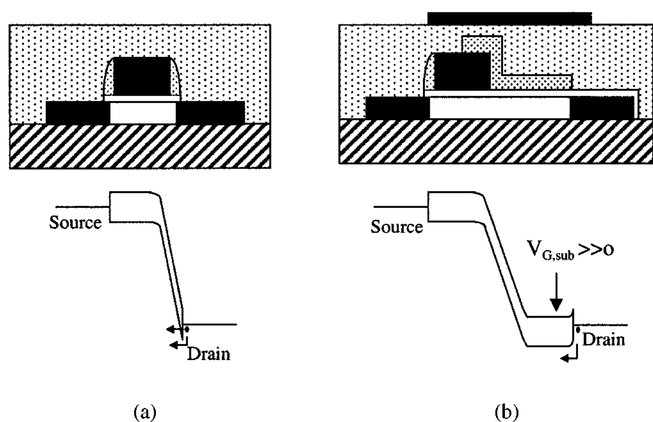

Fig. 5. Band diagrams for n-channel operation of SBTFTs with (a) conventional structure and (b) FID at off-state (i.e., $V_{G,\mathrm{main}} = 0, V_D = V_{\mathrm{DD}}$, and $V_{G,\mathrm{sub}} \gg 0$).

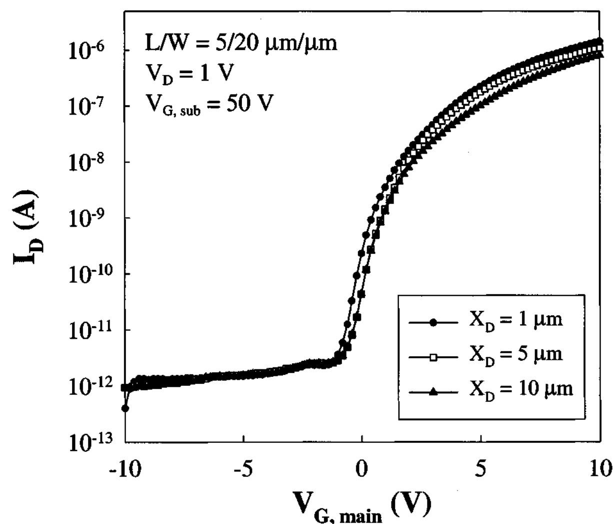

Fig. 6. Typical n-channel (V_d = 1 V) subthreshold characteristics of SBTFT devices with various X_D (e.g., 1, 5, and 10 μm). $L/W = 5/20\ \mu$m/μm.

Current ratios between the "on" and "off" states shown in Figs. 8 and 9 are depicted in Fig. 11. Owing to the severe short-channel effects and the n-type background channel doping mentioned above, ratio much larger than unity is retained at zero sub-gate bias in n-channel operation. This is consistent with the results shown in Fig. 2.

For long-channel (i.e., large X_D) devices, the drain current becomes nonsensitive to the main-gate bias, and the ratio approaches unity as the sub-gate bias becomes negative and positive for n- and p-channel operations, respectively. Band diagrams illustrated in Fig. 12 can be used to explain this phenomenon. In the figure, we concentrate only on the p-channel operation, although similar results can also be deduced for n-channel operation. When the subgate bias becomes positive, a strong electric field will be developed near the drain side. As a result, electron emission from the drain will be the dominant leakage mechanism, while the condition in the channel region

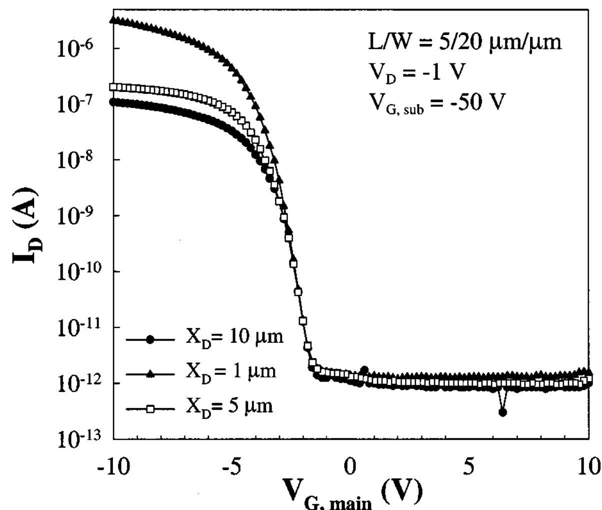

Fig. 7. Typical p-channel ($V_d = -1$ V) subthreshold characteristics of SBTFT devices with various X_D (e.g., 1, 5, and 10 μm). $L/W = 5/20$ μm/μm.

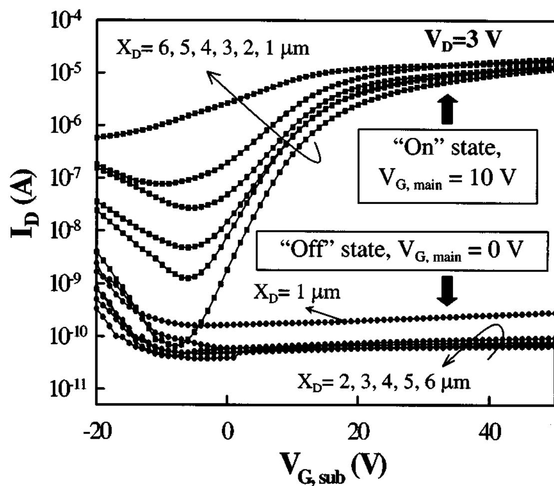

Fig. 8. Effects of the subgate bias and X_D on the n-channel operation of FID SBTFTs ($L/W = 5/20$ μm/μm).

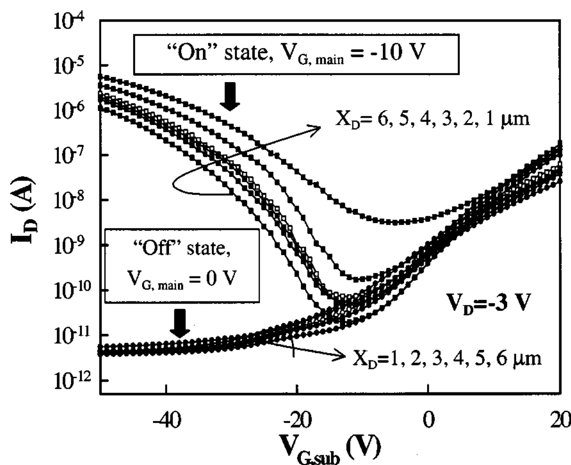

Fig. 9. Effects of the subgate bias and X_D on the p-channel operation of FID SBTFTs ($L/W = 5/20$ μm/μm).

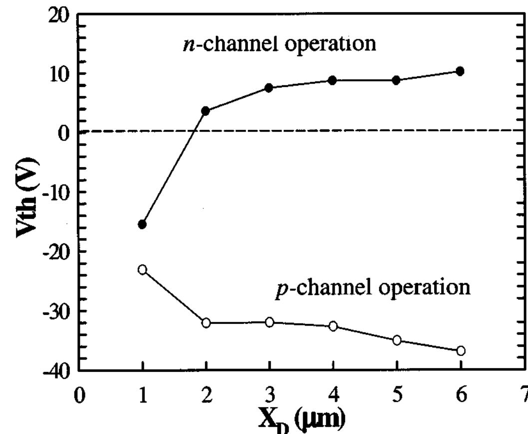

Fig. 10. V_{th} extracted from the "on" state *I–V* curves of Figs. 8 and 9 as a function of X_D.

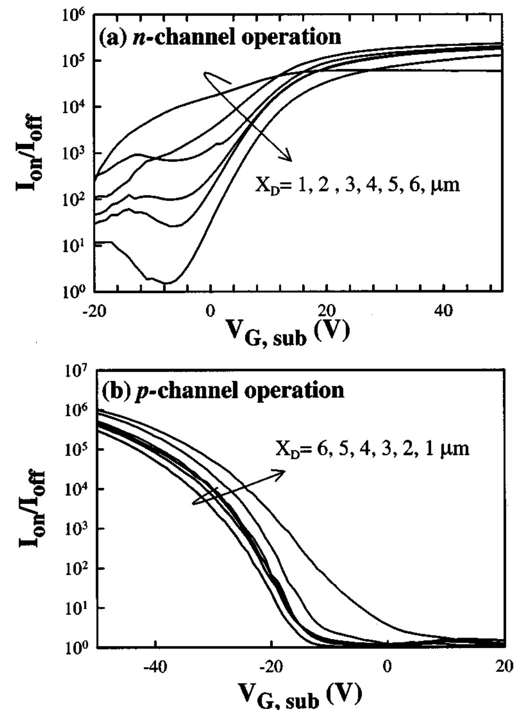

Fig. 11. Ratio between the "on" and "off" state currents (Figs. 8 and 9) for (a) n- and (b) p-channel operations.

underneath the main-gate (or the "pseudo source") has negligible effect. This could well explain why the off-state leakage is higher for p-channel operation with zero subgate bias than that with -50 V.

Finally, it should be pointed out that the drive performance of the proposed ambipolar device is not optimized in our experiment. This is because of the high barrier height ($\sim$0.5 eV) for both p- and n-channel operations used in our devices. Improvement could be made specifically for either p- or n-channel operations by adopting silicide materials with low barrier-height. For examples, ErSi and PtSi can be used for n- and p-channel operations, respectively. However, such improvement in drivability is achieved by compromising the capability of bi-channel operation.

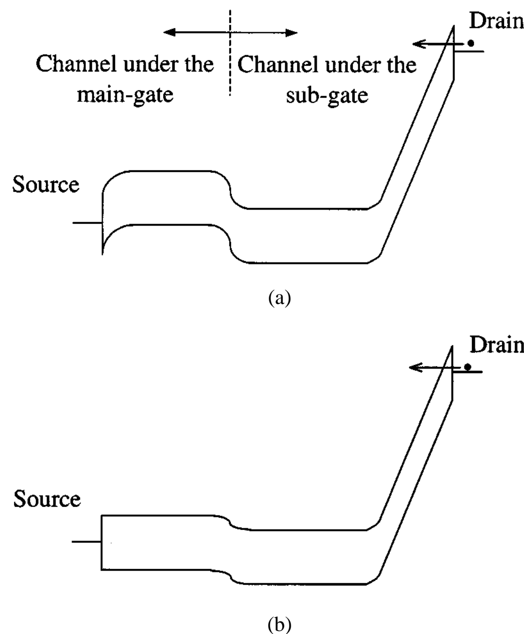

Fig. 12. Band diagrams for p-channel operation ($V_D = -3$ V) of FID SBTFT with a high positive subgate bias.

V. Conclusion

In summary, a novel implantless SBTFT with silicided S/D and FID extension capable of ambipolar operation is successfully demonstrated and compared with conventional SBTFTs. We found that while the conventional SBTFTs depict large GIDL-like leakage current and low on/off current ratio of less than 10^3, the new devices depict GIDL-free current characteristics with on/off current ratio as high as 10^6. This is achieved for both n- and p-channel modes of operation on the same device.

The proposed structure and its fabrication possess many advantages. First of all, all dopings (i.e., including the channel and S/D) and accompanying annealing steps are eliminated altogether, resulting in a much simplified overall process flow which is very suitable for low-temperature manufacturing. Second, the new structure is compatible with metal-gate processing, making feasible for the first time a fully implantless CMOS process, if metallic material such as TiN is adopted as the gate material. Third, no additional masking or processing steps is needed in the new structure. This is because the silcidation for forming the Schottky S/D can be performed simultaneously during the regular salicidation step, while the metal subgate can be formed simultaneously with metal interconnect. Fourth, the fully implantless process coupled with the ambipolar operation can greatly simplify CMOS process integration, resulting in an extremely low mask-count CMOS flow that is previously impossible. Finally, ambipolar modes of operation with superior characteristics are demonstrated for the first time, due to the unique device structure. The low current required for the subgate bias also allows the use of on-chip bias generator to simplify external power supply.

We also found that the channel region underneath the subgate has a lower $V_{\rm th}$ value and depicts much more severe SCE for n-channel operation. These trends are ascribed to the positive fixed charges at the oxide/channel interface and the n-type background channel doping, the latter could be explained by the prior furnace history used in the SPC step of the device fabrication.

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Horng-Chih Lin (S’91–M’95–SM’01) was born in I-Lan, Taiwan, R.O.C. on August 1, 1967. He received the B.Sc. degree in physics from National Central University, Chung-Li, Taiwan, in 1989, and the Ph.D. degree from the Institute of Electronics from National Chiao-Tung University, Hsinchu, Taiwan, in 1994.

In 1994, he joined the National Nano Device Laboratories, Hsinchu, as an Associate Researcher, and became a Researcher in 1999. His current research interests include plasma etching technology, salicide technology, thin-film transistor (TFT) fabrication and characterization, and reliability of CMOS devices.

Kuan-Lin Yeh was born in Hsinchu, Taiwan, R.O.C., on November 4, 1975. He received the B.S. degree in electrical engineering from Chang Chung University, Tao-Yuan, Taiwan, in 1998. He is currently pursing thePh.D. degree in the Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu.

His research interests are focused on the study of Schottky Barrier TFTs and low-temperature TFT processes.

Tiao-Yuan Huang (S'78–M'81–F'95) was born in Kaohsiung, Taiwan, R.O.C., on May 5, 1949. He received the B.S.E.E. and the M.S.E.E. degrees from National Cheng Kung University, Tainan, Taiwan, in 1971 and 1973, respectively, and the Ph.D. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1981.

After serving two years in the Taiwanese Navy, he joined the Chung Shan Institute of Science and Technology, Lungtan, working on missile development. Following two years with Semiconductor Process and Design Center, Texas Instruments, he has worked with several companies, including Xerox Palo Alto Research Center, Integrated Device Technology, Inc., and VLSI Technology, Inc. He had worked in various VLSI areas including memories (DRAM, SRAM, and nonvolatile memories), CMOS process/device technologies and device modeling/simulation, ASIC technologies, and thin-film transistors for LCD display. In 1995, he returned to Taiwan to become an Outstanding Scholar Chair Professor with National Chiao-Tung University and Vice President of National Nano Device Laboratories, National Science Council, Hsinchu, Taiwan. He has published over 150 technical papers in international journals and conferences, and holds over 40 patents.

Dr. Huang received the 1988 Semiconductor International R&D Technology Achievement Award for his invention of fully overlapped LDD transistors. He served on the technical committee of the IEEE International Electron Devices Meeting (IEDM) in 1991 and 1992. He also served on the program committee of the International Conference on Solid States Devices and Materials (SSDM) from 1996 to 1998.

Ruo-Gu Huang (S'00) was born in Taiwan, R.O.C. in 1976. He received the B.S. degree in electrical engineering from National Tsing-Hua University, Taiwan, in 1999, and the M.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2001.

He is an Engineer with the Core SOC Division of Macronix International Corporation, Hsinchu. His research interests include microelectronic devices and VLSI circuit design.

Simon M. Sze (M'66–SM'74–F'77–LF'01) received the B.S. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., the M.S. degree from the University of Washington, Seattle, and the Ph.D. degree from Stanford University, Stanford, CA, all in electrical engineering.

He was with Bell Laboratories from 1963 to 1989. He joined the faculty of Electronics Engineering Department, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1990. At present, he is UMC Chair Professor of NCTU, and President of the National Nano Device Laboratories. He has made pioneering contributions to metal-semiconductor contacts, microwave and photonic devices, and submicron MOSFET technology. Of particular importance is his invention of the nonvolatile semiconductor memory such as EEPROM and flash memory. This memory is a key component for the cellular phone, notebook computer, smart IC card, digital camera, and a host of portable electronic system. He has authored or coauthored over 150 technical papers and written and contributed to 24 books. His book *Physics of Semiconductor Devices* (New York: Wiley, 1969, 2nd ed., 1981) is the most cited work in contemporary engineering and applied science publications (over 12000 citations from ISI Press).

Dr. Sze has received the IEEE Ebers Award, the Sun Yat-sen Award, the National Science and Technology Award, and the National Chair Professor Award. He is a member of the Academia Sinica, the Chinese Academy of Engineering, and the U.S. National Academy of Engineering.