

# Characterization and Modeling of On-Chip Spiral Inductors for Si RFICs

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**Abstract**—The paper presents a complete characterization of on-chip inductors fabricated in BiCMOS technology. First, a study of the scaling effect of inductance on geometry and structure parameters is presented to provide a clear guideline on inductor scaling with suitable quality factors. The substrate noise analysis and noise reduction techniques are then investigated. It is shown that floating well can improve both quality factor and noise elimination by itself under 3 GHz and together with a guard ring above 3 GHz. Finally, for accurate circuit simulations, a new inductor model is developed for predicting the skin effect and eddy effect and associated quality factor and inductance.

**Index Terms**—Equivalent lumped circuit, inductors, modeling, skin effect.

## I. INTRODUCTION

THE SURGING demand of silicon-based radio frequency integrated circuits (RFICs) has raised tremendous interest in on-chip passive components. The on-chip spiral inductor is one of the key elements in monolithic RFIC designs such as amplifiers, mixers, filters, and oscillators [1]–[3]. Some essential features for integrated inductors include scalability in layout design, high quality factor, high self-resonant frequency ( $f_{SR}$ ), large inductance range with small inductor size, and good RF models.

Scalability of inductance values is important for optimized layout design. A methodology for scaling the inductance versus layout parameters is needed, with layout parameters including number of turns, coil width and spacing, and guard ring placement. There are also composite rules, which include parallel combination and series combination to maximize scaling range. A high quality factor is critical. The quality factor is important in that it is an index of contained electromagnetic energies (versus dissipated energy), provided to filters [2], [3] and to oscillators at tuned frequency [2], and an index of the impedance matching efficiency in front-end amplifiers [1], [2]. The quality factor can be degraded by parasitic resistance [4], [5] from lines and substrate, as well as reduced self-resonant frequency. The self-resonant frequency is the upper bound for an inductor to

be functional, determined by the parasitic capacitance resulting from the substrate and between coils. Both the quality factor and self-resonant frequency are major elements determining the allowed inductance range. As both parasitic resistance and capacitance can degrade inductor performance, developing methods of minimizing their induced loss is important in RFIC technology. The design of an on-chip inductor requires simultaneous optimization of scaling, quality factor, and self-resonant frequency, while still having a small silicon area for the sake of chip size.

In addition to inductance characteristic optimization, high-frequency models are also important for circuit design. RF models based on lumped equivalent-circuit [5]–[7] have successfully been developed [2]. A major shortcoming of these lumped models is that they cannot model high frequency characteristics very well because of the impacts of inherent connection wires' inductance and substrate capacitance [2], [5]–[7]. These works also ignored the frequency dependence of metal lines or substrate resistance at high frequencies due to skin effect [18]. In the works of Yoon [8] and Burghzrtz [9], a frequency-dependent resistance element was used to describe the resistance change due to the skin effect in the coil conductor and in the substrate. Nevertheless, the parameters for this resistance are hard to be determined or implemented into circuit simulators [10]–[12].

In this paper, we present a complete set of characterization of on-chip inductors in a BiCMOS process with two-level metal layers. Our works include the following: a) Give complete characterization and scaling rules of various inductor schemes with their dependencies of inductance and quality factor on geometry parameters. The parameters include inner opening diameter, number of turns, and coil conductor width and conductor interturn spacing, substrate contact guard ring distance, and parallel and series inductors. b) To raise the quality factors of integrated inductors by reducing substrate loss, a novel inductor configuration with a floating well underlaying is presented. It will be shown that this configuration can significantly improve the quality factor without  $f_{SR}$  reduction and without extra area-consumption. c) For accurate circuit simulation, a novel model is developed to model the substrate skin effect and eddy current effect and associated frequency-dependent resistance and inductance. The new model adopts a parallel combination of a resistor and an inductor on the signal-through path. The lumped-circuit approach is easy for parameters extraction and for SPICE implementation. This set of inductors can be easily implemented by generic CMOS or BiCMOS processes without extra implant or masking steps, which is important for low cost silicon systems [9].

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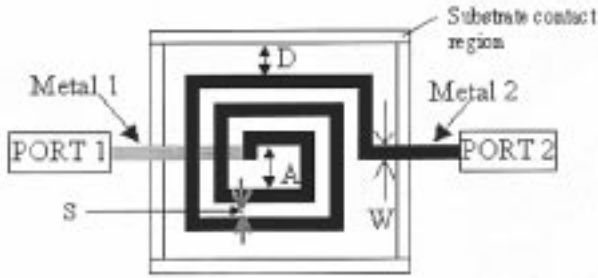


Fig. 1. Top view of a planar spiral inductor.

This paper is organized as follows: In Section II, the complete study of spiral inductor design and scaling is presented, where the characteristics of inductance, quality factor, self-resonant frequency ( $f_{SR}$ ), and frequency at  $Q_{max}$  are discussed. In Section III, the performance and noise improvement using the floating well are discussed and a detailed study of substrate isolation in P-well, N-epitaxial layer, and floating N-well are also presented. In Section IV, a novel inductor model with substrate skin effect and eddy current effect is given. Section V concludes the paper.

## II. SPIRAL INDUCTOR DESIGN AND SCALING EFFECT

### A. Experimental Setup

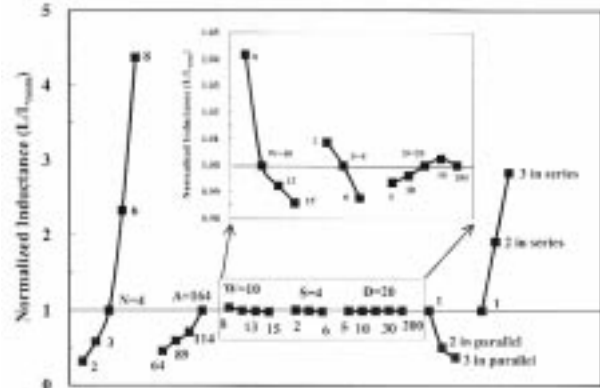
A 0.6- $\mu\text{m}$  double-layer metal BiCMOS technology is used to fabricate the on-chip spiral inductors. The N-type epilayer resistivity is 0.5 ohm-cm, the substrate resistivity is 10 ohm-cm, the thickness of Metal-1 and Metal-2 are about 0.7 and 1  $\mu\text{m}$ , respectively, and the oxide thickness between Metal-2 and the substrate is 2  $\mu\text{m}$ . A typical layout representation of a planar spiral inductor is shown in Fig. 1. The inductor is a three-turn Metal-2 square inductor. Metal-1 terminal is defined as port 1 and Metal-2 terminal is defined as port 2.

The configurations of the inductor include a variety of numbers of turns ( $N$ ), inner opening diameters ( $A$ ), coil conductor widths ( $W$ ), conductor interturn spaces ( $S$ ), substrate contact guard ring distances ( $D$ ), parallel-inductors, and series inductors. The substrate contact guard ring is used as a grounded wall shorted to the substrate in order to prevent the noise coupling in RFIC.

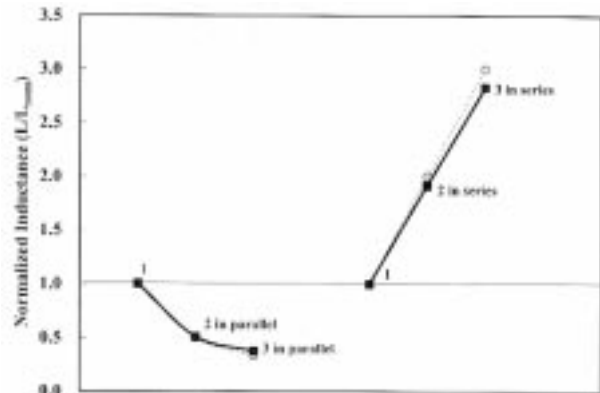
Scattering parameters are measured using on-wafer two-port G-S-G RF probes and an HP8510C Network Analyzer. Pad parasitic is de-embedded by subtracting out open pattern's  $y$ -parameters. The measured frequency range is from 100 MHz to 20 GHz. The inductance ( $L$ ) and quality factor ( $Q$ ) are extracted from the de-embedded  $Z$ -parameters using

$$\text{Inductance}(L) = \frac{\text{imag}(Z_{1\text{port}})}{2\pi f} \quad (1)$$

$$\text{Quality Factor}(Q) = \frac{\text{imag}(Z_{1\text{port}})}{\text{real}(Z_{1\text{port}})}. \quad (2)$$



(a)



(b)

Fig. 2. (a) Normalized inductances at 900 MHz for various inductor configurations with  $L_{nom} = 5.5$  nH. (b) Normalized inductances at 900 MHz only for inductors in parallel and in series. The hollow circles show calculated trends of 1/1, 1/2, 1/3, and 1, 1  $\times$  2, 1  $\times$  3, respectively. The rms error between the trend and measured inductance is 6.1%.

### B. Inductor Design and Characterization

1) *Inductance*: The normalized inductances at 900 MHz for various inductor configurations are shown in Fig. 2(a). Here,  $L_{nom}$  is the inductance of a single inductor configuration, with  $N = 4$ ,  $A = 164$   $\mu\text{m}$ ,  $W = 10$   $\mu\text{m}$ ,  $S = 4$   $\mu\text{m}$ , and  $D = 20$   $\mu\text{m}$ .  $L_{nom}$  is 5.5 nH at 900 MHz. Fig. 2 shows the inductance dependence on the number of turns ( $N = 2, 3, 4, 6, 8$ ), inner opening diameter ( $A = 64$   $\mu\text{m}$ , 89  $\mu\text{m}$ , 114  $\mu\text{m}$ , 164  $\mu\text{m}$ ), coil conductor width ( $W = 8$   $\mu\text{m}$ , 10  $\mu\text{m}$ , 13  $\mu\text{m}$ , 15  $\mu\text{m}$ ), conductor interturn space ( $S = 2$   $\mu\text{m}$ , 4  $\mu\text{m}$ , 6  $\mu\text{m}$ ), substrate contact guard ring distance ( $D = 5$   $\mu\text{m}$ , 10  $\mu\text{m}$ , 20  $\mu\text{m}$ , 30  $\mu\text{m}$ , 200  $\mu\text{m}$ ), the number in parallel (single, two in parallel, three in parallel), and the number in series (single, two in series, three in series). Inductance can be raised by the increase of  $N$ ,  $A$ , or  $D$  and the decrease of  $W$  or  $S$ . Inductance has a strong dependence on the number of turns ( $N$ ) and inner opening diameter ( $A$ ). The increase with  $W$  can be attributed to the increased coil-to-ground capacitance and so-induced reduction of frequency at  $Q_{max}$ . The increase with  $D$  behaved as expected, as a result of higher substrate parasitic resistance with larger  $D$  [13]. These results are useful for the optimization of inductance. On the right-hand side of Fig. 2(a), the inductances are shown to be proportional to the number of inductors in series and inversely proportional to the number of inductors in parallel. The proportionality is

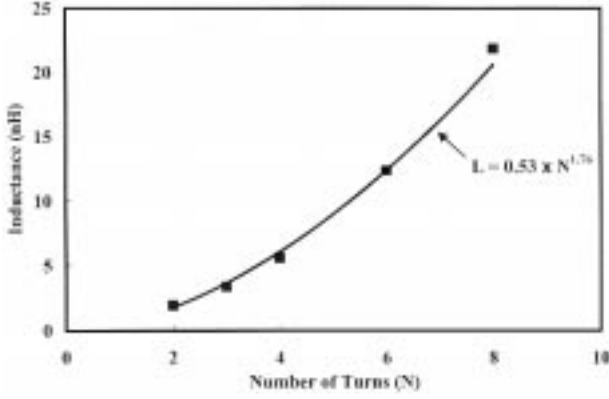


Fig. 3. Measured inductance at 100 MHz (solid squares) with number of turns ( $N$ ). The solid line is the regression trend line.

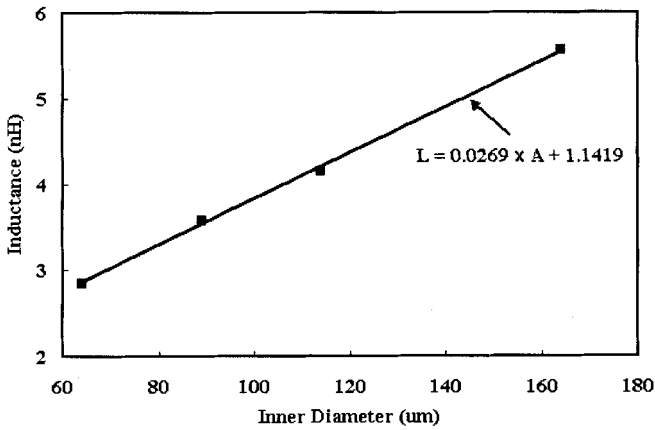


Fig. 4. Measured inductance at 100 MHz (squares) with inner diameters ( $A$ ). The solid line is the linear trend line.

demonstrated by comparing the trend line (trend line calculated by addition or reciprocal addition) with the measured data as shown in Fig. 2(b), giving a root mean square error of 6.1% between measured data and trend line. This allows for designing an inductor using a multiple of available inductors and also allows for constructing a complete inductance library based on a simplified inductor database.

Fig. 3 shows measured inductance at 100 MHz versus the number of turns and an extracted trend line. The equation of trend-line exhibits that inductance of a square spiral inductor is proportional to  $N^{1.76}$ , note that the exponent 1.76 is close to  $5/3$  as suggested by the empirical formula for printed board circuits [14]–[16]. This empirical formula in [14] showed that inductance is proportional to the square root of total area of inductor, implying that the inductance of a square spiral inductor should be linearly proportional to the inner opening diameter ( $A$ ); this agrees well with our experimental data shown in Fig. 4. In order to provide a complete guideline on inductor scaling, a monomial expression [22] based on geometry parameters  $N$ ,  $A$ ,  $W$ , and  $S$  can be obtained as

$$L_{\text{monomial}} \text{ (nH)} = \beta d_{\text{out}}^{\alpha_1} W^{\alpha_2} d_{\text{avg}}^{\alpha_3} N^{\alpha_4} S^{\alpha_5} \quad (3)$$

where, as extracted at 900 MHz,  $\beta = 1.91 \times 10^{-3}$ ,  $\alpha_1 = -1.22$ ,  $\alpha_2 = -0.132$ ,  $\alpha_3 = 2.37$ ,  $\alpha_4 = 1.76$ ,  $\alpha_5 = -0.0443$ , the outer diameter  $d_{\text{out}} = A + 2 \times [N \times W + (N - 1) \times S]$ , the average

diameter (or the full ratio)  $d_{\text{avg}} = 0.5 \times [d_{\text{out}} + A]$  and the unit of  $d_{\text{out}}$ ,  $W$ ,  $d_{\text{avg}}$ , and  $S$  is  $\mu\text{m}$ . The maximum error between (3) and measurement data is 9.4% and the rms error is 7.7%.

2) *Quality Factor, Frequency at  $Q_{\text{max}}$ , and Self-Resonant Frequency*: The quality factor for an on-chip spiral inductor increases as the frequency increases because of increased stored energy and then drops drastically when the frequency closes to the self-resonant frequency ( $f_{\text{SR}}$ ). The quality factor  $Q$  reaches a maximum  $Q_{\text{max}}$  when the frequency approaches to a value that is close to  $f_{\text{SR}}$ , namely,  $f_{Q_{\text{max}}}$ . A spiral inductor must have its  $f_{Q_{\text{max}}}$  higher than its application frequency for RFIC design. High quality factor and good  $f_{Q_{\text{max}}}$  are essential for a spiral inductor.

Fig. 5 shows normalized  $Q$  ( $Q_{\text{nom}}$ , measured at 900 MHz), normalized  $Q_{\text{max}}$  ( $Q_{\text{max,nom}}$ , measured at  $f_{Q_{\text{max}}}$ ), the frequency at  $Q_{\text{max}}$  ( $f_{Q_{\text{max}}}$ ), and the self-resonant frequency for various inductor configurations. The  $Q_{\text{nom}}$  and  $Q_{\text{max,nom}}$  are measured from the inductor with  $N = 4$  and  $A = 164 \mu\text{m}$ ,  $W = 10 \mu\text{m}$ ,  $S = 4 \mu\text{m}$ , and  $D = 20 \mu\text{m}$ , giving  $Q_{\text{nom}} = 1.9$  and  $Q_{\text{max,nom}} = 2.45$ . To consider a 900-MHz application from Fig. 5(c), spiral inductors with  $N \geq 6$  or number in series  $\geq 3$  are not recommended as their  $f_{Q_{\text{max}}}$  are almost lower than 900 MHz. Inductors with  $N \leq 4$  and an inner diameter smaller than  $114 \mu\text{m}$  can be used for the 1.9-GHz design.

When normalized  $Q$  for inductors with  $N \geq 6$  or the number in series  $\geq 3$  are ignored, as shown in Fig. 5(a),  $Q$  increases monotonically with increased  $N$ ,  $A$ ,  $W$ ,  $D$  and with decreased  $S$  and the numbers in parallel. Compared with  $Q$  dependence on dimensions, however,  $Q_{\text{max}}$  shows an opposite dependence on  $N$ ,  $A$ , and the number in parallel, as shown in Fig. 5(b). This is because  $Q_{\text{max}}$  depends strongly on  $f_{\text{SR}}$ . That is,  $Q$  increases until the self-resonant effect is initiated which pushes out the storage energy inside the inductor and pulls the inductor into a self-resonant state with frequency being increased to  $f_{\text{SR}}$ . The initiation of the self-resonant effect is about at a frequency of approximately  $0.3 \times f_{\text{SR}}$ , which also is the frequency  $f_{Q_{\text{max}}}$ . As a result,  $Q_{\text{max}}$  is significantly influenced by  $f_{\text{SR}}$ . To explore the dependence on each design parameter, the following can be observed: i)  $Q$  increases but  $Q_{\text{max}}$  decreases with increased  $N$  [Fig. 5(b)]; this is obviously due to decreased  $f_{\text{SR}}$  [Fig. 5(d)] resulting from increased coil to ground capacitance. ii) An inner opening diameter  $A$  gives a similar dependence as  $N$ . iii) The  $f_{\text{SR}}$  increases with increased  $D$  (coil to  $P+$  guard ring spacing) resulting from increased substrate resistance and reduced substrate parasitic capacitance and hence both  $Q_{\text{max}}$  and  $Q$  increase. Figs. 2(a) and 5 show the reduced inductance, self-resonant frequency, and quality factor with reduced substrate contact guard ring distance ( $D$ ), as discussed in Section II-B. Our results agree well with the claim of [19] in that the guard ring can reduce noise, but mirror effect can reduce the inductance, hurt the self-resonant frequency, and degrade quality factor. (iv) The parallel combination of inductors shows increased  $Q_{\text{max}}$  due to larger effective separation from coils in parallel to the  $P+$  guard ring. On the contrary, inductors in series show decreased  $Q_{\text{max}}$  and  $f_{\text{SR}}$  because of a larger coil-to-substrate capacitance.

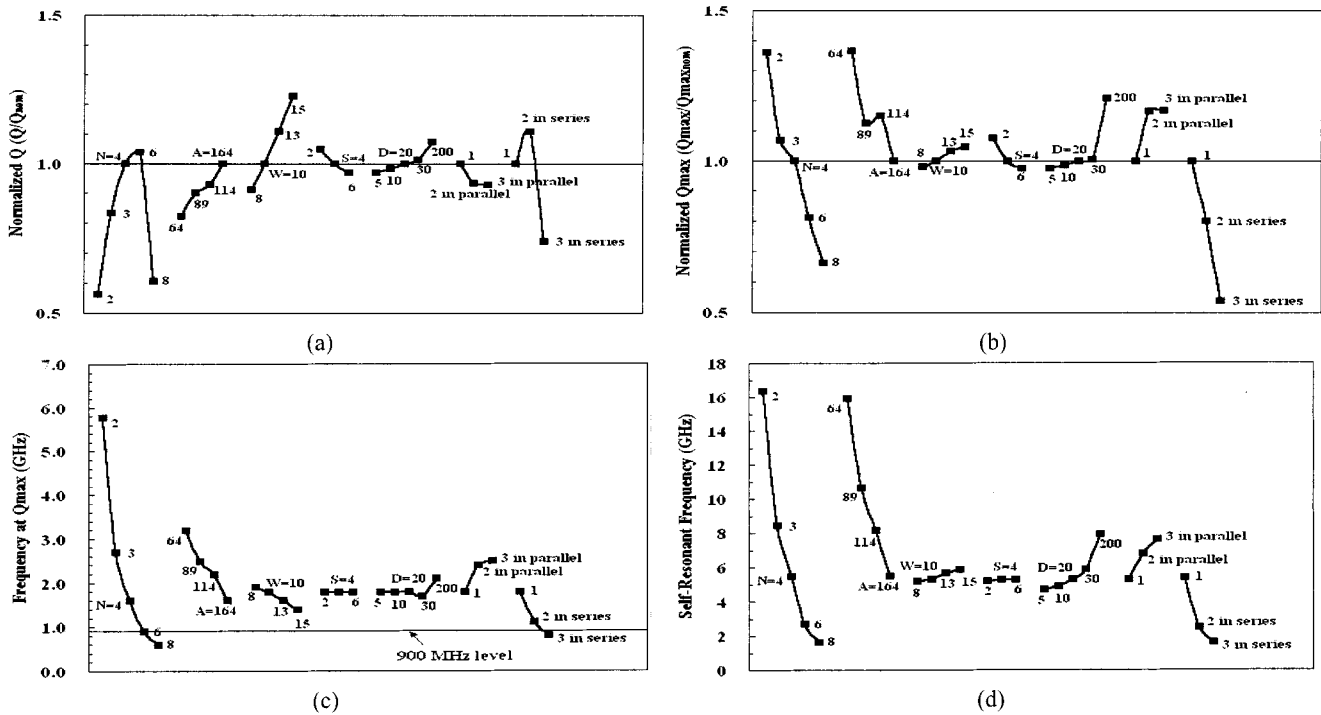


Fig. 5. (a) Normalized  $Q$  at 900 MHz where  $Q_{nom} = 1.9$ , (b) normalized  $Q_{max}$  where  $Q_{max,nom} = 2.45$ , (c) frequency at  $Q_{max}$ , and (d) self-resonant frequency for various inductor configurations.

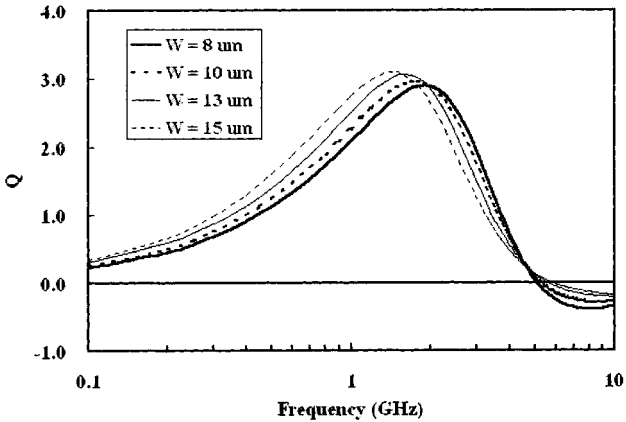


Fig. 6. Measured  $Q$  versus frequency for various metal widths ( $W = 8, 10, 13, 15 \mu\text{m}$ ).

For the optimization of inductor quality factor, the substrate effect on the  $Q$  of the inductor can be derived based on a simplified one-port circuit model shown in Fig. 7. See (4) shown at the bottom of the page. In (4), as  $R_s^2 C_{ox}^2 / L_s$  is much less than 1

for conventional inductor and frequency is low, the  $Q$  is close to  $\omega L_s / R_s$ , which results in  $R_{sub}$ -independent  $Q$  value. The dependence of  $Q$  on  $R_{sub}$  at high frequency is different in a low  $R_{sub}$  region and high  $R_{sub}$  region. As frequency increases in the low  $R_{sub}$  region, the  $Q$  can be simplified to

$$\left( \frac{\omega L_s}{R_s} \right) \left[ 1 - \left( \omega^4 \left( \frac{R_{sub}}{R_s} \right) L_s^2 C_{ox}^2 + \omega^2 R_{sub} R_s C_{ox}^2 + \omega^2 L_s C_{ox} \right) \right]$$

which results in degraded  $Q$  with increased  $R_{sub}$ . In a high  $R_{sub}$  region, where the  $R_{sub}$  is much larger than  $1/\omega C_{ox}$  and  $R_s$ , the  $Q$  approaches  $\omega L_s / R_s [1 - (\omega^2 L_s^2 + R_s^2) / (\omega^2 L_s^2 + R_s R_{sub})]$ , which gives increased  $Q$  with increasing  $R_{sub}$ . In addition, we get smaller  $Q$  degradation versus frequency from the ideal  $Q$  value ( $\omega L_s / R_s$ ) with increasing  $R_{sub}$ . Based on (4), taking the derivative of  $Q$  with respect to  $R_{sub}$ , we can obtain the  $R_{sub}$

$$\begin{aligned} \text{Quality Factor}(Q) &= \frac{\text{imag}(Z_{1port})}{\text{real}(Z_{1port})} \\ &= \frac{\omega L_s}{R_s} \left[ 1 - \frac{\omega^4 \left( \frac{R_{sub}}{R_s} \right) L_s^2 C_{ox}^2 + \omega^2 R_{sub} R_s C_{ox}^2 + \omega^2 L_s C_{ox} + R_s^2 \left( \frac{C_{ox}}{L_s} \right)}{1 + \omega^4 \left( \frac{R_{sub}}{R_s} \right) L_s^2 C_{ox}^2 + \omega^2 R_{sub} R_s C_{ox}^2 + \omega^2 R_{sub}^2 C_{ox}^2} \right] \end{aligned} \quad (4)$$

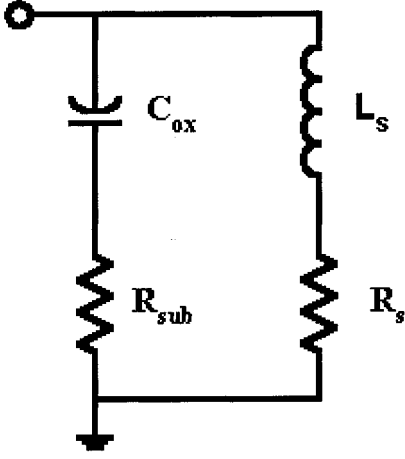


Fig. 7. A simplified one-port physical model of an on-chip spiral inductor. The inductance and series resistance of the spiral is represented by  $L_s$  and  $R_s$ , respectively. The oxide capacitance between the spiral and the substrate is modeled by  $C_{ox}$ . The resistance of the substrate is modeled by  $R_{sub}$ .

giving the worst  $Q$  in (4) by setting the derivative to zero. The  $R_{sub}$  can be solved analytically as follows:

$$R_{sub}^2 (\omega^2 C_{ox}^2) + R_{sub} \left( \frac{2R_s C_{ox}}{L_s} \right) + \left( \omega^2 L_s C_{ox} + \frac{R_s C_{ox}}{L_s} - 1 \right) = 0. \quad (5)$$

The realization of  $Q$  dependence on  $R_{sub}$  is very useful for the optimization of  $Q$  with appropriate substrate engineering.

It is observed that the frequencies  $f_{Q_{max}}$  and  $f_{SR}$  have different dependencies on metal width from Fig. 5(c) and (d). The  $Q$  versus frequency for various metal widths is shown in Fig. 6, which exhibits that larger metal width significantly improves  $Q$  at lower frequency, but also induces lower  $f_{Q_{max}}$ . It is recommended to use  $f_{Q_{max}}$  instead of  $f_{SR}$  as a gauge of evaluating spiral inductor performance.

For the purpose of providing a guideline on scaling  $Q$ , another monomial expression is developed to describe  $Q$  at 900 MHz to be  $Q = \gamma d_{out}^{\eta_1} W^{\eta_2} d_{avg}^{\eta_3} N^{\eta_4} S^{\eta_5}$ , with  $\gamma = 1.88 \times 10^6$ ,  $\eta_1 = -22.8$ ,  $\eta_2 = 4.28$ ,  $\eta_3 = 17.8$ ,  $\eta_4 = 4.93$ ,  $\eta_5 = 0.888$ . The maximum error by comparison with measurement data is 16.0% and the root mean square error is 11.5%. This formula can be used for inductor geometry within the span of the original database.

### III. ISOLATION CHARACTERIZATION AND IMPACT ON INDUCTORS

#### A. $Q$ Improvement With Floating Well

The propagation characteristic of an Si-SiO<sub>2</sub> micro-strip configuration is a primary energy loss element of the planar spiral inductor [17]. This loss is more pronounced for a large inductor hanging over large silicon land. Among various loss mechanisms [18], for silicon technology (which uses moderately conductive substrate and is usually operated at frequency around several GHz) the skin-effect mode is of particular interest. Note that here, for resistivity of 0.1 ohm-cm (with a skin depth  $\delta_s$  of

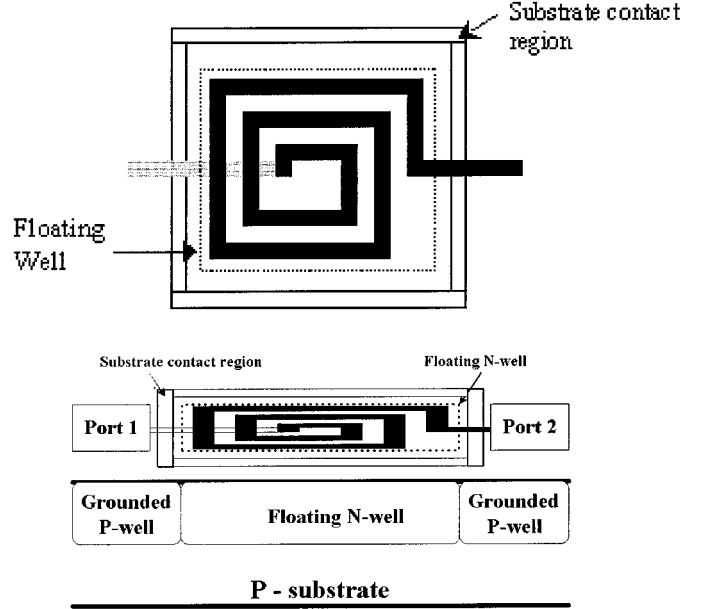


Fig. 8. Schematic view and cross sections of FW-inductor structure.

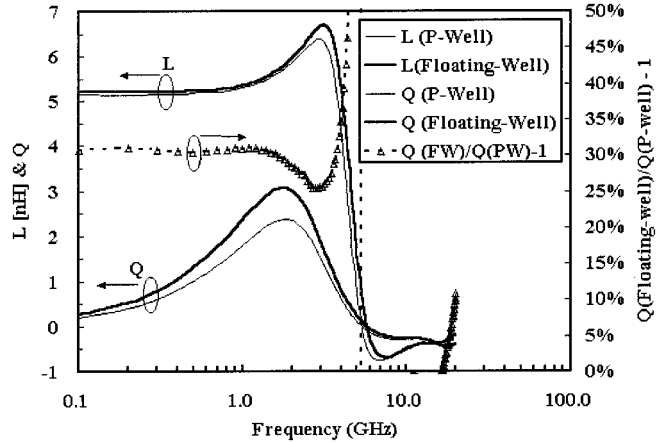


Fig. 9. Inductance and quality factor for inductors on P-well and floating N-well.

$\sqrt{2/(\omega\mu\sigma)} = 503 \mu\text{m}$  at 1 GHz) and substrate thickness of  $1000 \mu\text{m}$ , the boundary frequency for the skin effect mode is  $f \geq 1 \text{ GHz}$ , while for the slow wave mode it is  $f \leq 0.12 \text{ GHz}$  [18]. Under the skin-effect mode, the silicon substrate begins to act as a lossy conductor wall and the longitudinal currents are close to the Si-SiO<sub>2</sub> interface. Therefore, reducing the substrate loss can efficiently enhance the quality factor. In what follows, we propose a novel inductor structure to retard the longitudinal current and reduce the substrate loss by adding a floating-well (FW) to increase substrate ac resistance.

Fig. 8 shows the schematic view of an FW-inductor structure. The FW-inductor is similar to a conventional on-chip planar spiral inductor and the only change is to add a floating well junction layer under the inductor and inside the noise-reduction grounded guard ring wall. The floating well junction layer behaves as a dc-isolation layer with high ac-resistance to reduce the substrate loss; hence, the quality factor is raised.

According to our experimental data, the inductances and quality factors for an inductor on P-well and an FW-inductor with a floating well underlaid are shown in Fig. 9. As observed

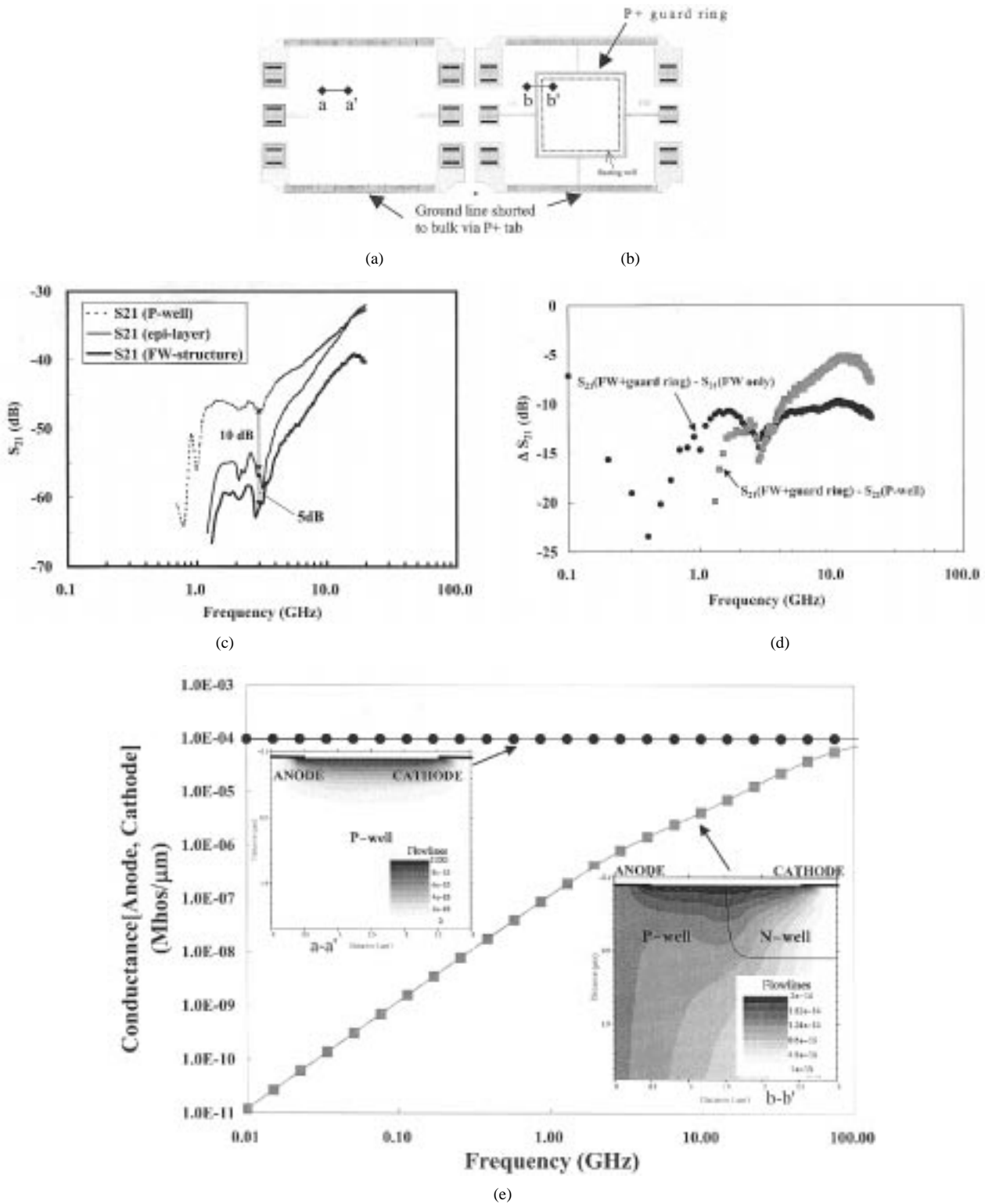


Fig. 10. (a) Layout of an open pattern on P-well layer or epilayer. (b) Layout of an open pattern on FW-structure. (c) Measured  $S_{21}$  with frequency for open patterns on P-well layer, N-epilayer, and FW-structure. (d)  $S_{21}$  reduction compared to open pattern with both FW and guard ring of: 1) solid-squares, on P-well without FW and guard ring, and 2) solid-circles, with FW only. (e) Simulated substrate conductance trend versus frequency on P-well layer and FW-structure by using Medici, where simulated current flow lines at 1 GHz are shown in the insets. The lengths of trajectories  $a$ - $a'$  and  $b$ - $b'$  are not scaled.

from the curve of  $Q(\text{FW})/Q(\text{PW}) - 1$  in Fig. 9, the quality factor is improved about 31% for frequency below 1 GHz and  $Q_{\max}$  increases to 3.07 from 2.37, which is 29% up, at 1.8 GHz. Some improvement is observed for the self-resonant frequency. There is no obvious difference for inductance at

lower frequency. Current flow in the substrate beneath the spiral would cause negative mutual coupling and thus a reduction in the low frequency inductance of the spiral. The unaffected low frequency inductance indicates that the substrate current induced by the magnetic field is small [20]. The improvement

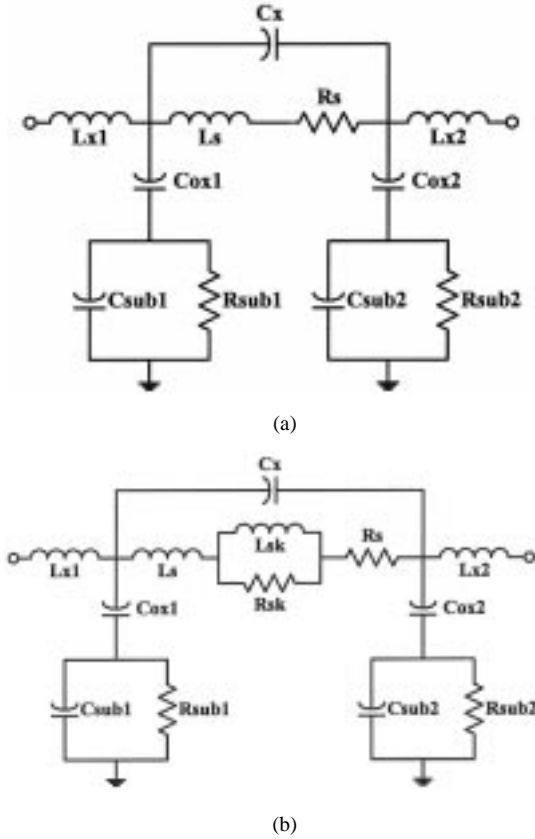


Fig. 11. (a) Conventional inductor lumped model for on-chip spiral inductor and (b) new proposed lumped model with the addition of a combination of  $L_{sk}$  and  $R_{sk}$  in parallel.

in  $Q$  is due to the increased substrate resistivity induced by the floating N-well and associated junction depletion layer. Furthermore, to quantify the increase of the effective substrate resistance by using FW structure, we compare the  $Q$  to that of an inductor on N-epi layer. The  $Q$  of an inductor on the FW is a little higher but very close to that on the N-epi layer with the difference within 2% below 1 GHz. The floating well structure can improve  $Q$  by increasing effective substrate resistance of well layer from 0.1 ohm·cm (P-well resistivity) to equivalently 0.5 ohm·cm (epilayer resistivity). A detailed study of the substrate resistivity enhancement using a floating N-well will be presented in the next subsection. Moreover, to obtain further improvement for other components, a complete study of substrate isolation with floating well, P-well, and N-epitaxial layer will also be presented.

### B. Substrate Isolation Effects

RF signal isolation to prevent coupling noise through substrate is important for spiral inductor in silicon-substrate technology. Improved RF isolation can be achieved by using a grounded substrate guard ring surrounding the inductor [19] or by using higher resistivity ( $\rho \sim 0.5$  ohm·cm) N-epitaxial layer in our experiment [3]. To study the isolation effects, as shown in Fig. 10, three structures are designed: open pads on P-well, open-pads on N-epi wafer without any well [both as shown in Fig. 10(a)], and open pads with a floating N-well (FW), which

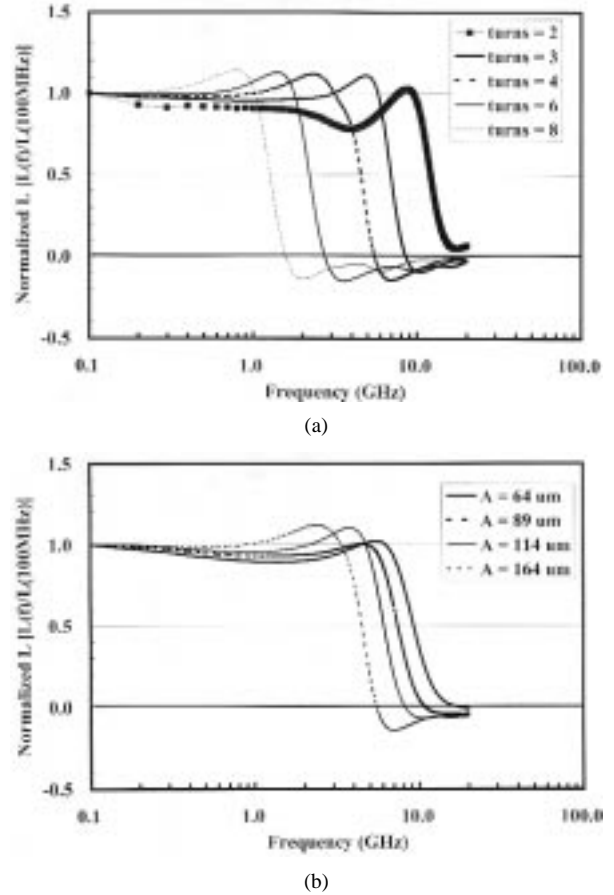


Fig. 12. Normalized inductance versus frequency for inductors with (a) various numbers of turn and (b) various inner diameters.

is surrounded by P-well, between pads [Figs. 10(b) and 8]. The pads are of a dimension of  $80 \mu\text{m} \times 80 \mu\text{m}$ , configured with M2 and M1 stacked together with large vias. The distance between the two open pads is  $574.2 \mu\text{m}$ . Based on scattering parameter measurement with 0-dB input signal level, we obtain 10-dB improvement of  $S_{21}$  at 3 GHz for an open pattern on N-epilayer without well implantation ( $\rho \sim 0.5$  ohm·cm) compared to that on a P-well implantation layer ( $\rho \sim 0.1$  ohm·cm). However, the improvement of using only N-epilayer decreases at a frequency higher than 10 GHz, indicating that the high-frequency harmonics cannot be blocked by bulk with higher resistivity.

Compared to using a higher resistivity substrate, the structure with both a substrate grounded guard ring and a floating N-well inside, as shown in Fig. 10(b), can give a much better isolation characteristic even for frequency above 10 GHz. The  $S_{21}$  at 3 GHz for the open pattern of FW-inductor configuration is 15 dB lower than that on P-well and 5 dB lower than N-epi bulk, as shown in Fig. 10(c). Moreover, the isolation is more improved at a frequency higher than 10 GHz; note that 4-dB improvement at 10 GHz is shown on N-epi layer, even the isolation difference between on N-epi and on P-well vanishes. In Fig. 10(d), the difference of  $S_{21}$  between an open pattern on FW-structure with surrounding guard ring and another one on FW only, marked as the solid-circles, shows the  $S_{21}$  reduction induced by guard ring. The solid-squares show the  $S_{21}$  reduction of the open pattern with FW-structure and guard ring that

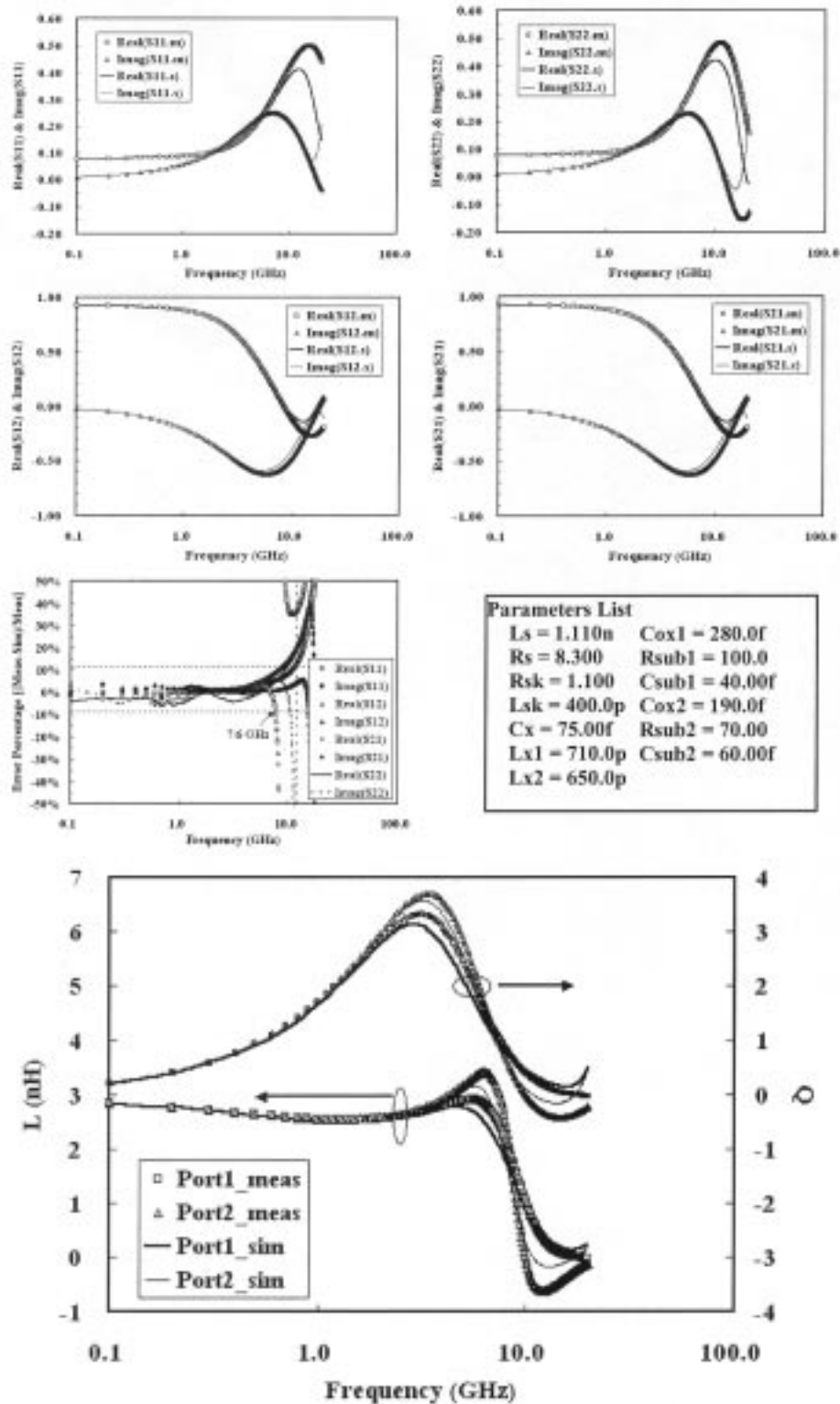


Fig. 13. Measured and simulated  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$ , inductance and quality factor for two port configuration, for inductor with  $N = 4$  and  $A = 64 \mu m$ . All parameters for the lumped model are shown in the parameter list table.

is compared to that on P-well. An open pattern on FW-structure with guard ring shows better noise ( $S_{21}$ ) decrease than that with FW only, though the FW only pattern also shows reduced  $S_{21}$  versus the one on P-well (without FW and guard ring) for a frequency below or close to 3 GHz. Note that the improvement of isolation from FW is because the FW forms a depletion

layer at the sidewall with low conductance to behave as a barrier to eliminate coupling signal and noise dispersion through substrate, which is effective for lower frequency. However, the FW has to be used together with a  $P+$  guard ring surrounding the FW at a frequency higher than 3 GHz for effective noise elimination. In this frequency range, the guard ring is the main cause



of noise elimination because surrounding the  $P+$  guard ring can efficiently absorb the longitudinal currents, which flow along a trajectory close to the silicon surface. It should be noted that an FW without guard ring shows degraded noise isolation because of the reduced noise pickup by ground line ( $p+$  tab) induced by the FW depletion layer at edge. The reduced pickup relatively enhances the noise signal propagated to port-2 ( $S_{21}$ ). Furthermore, an inductor on the FW shows 31% improved quality factor compared to a conventional inductor as mentioned in Section III-A. Based on these two improvements, the FW-inductor is recommended for better RF isolation and performance.

These noise improvements using an FW can be verified using MEDICI [21] simulation as shown in the insets of Fig. 10(e), where at 1 GHz, the peak current density from anode to cathode on a silicon surface decreased by ten orders in the FW (compared to the P-well structure). In these insets, for the P-well structure, the conductance characteristic between two surface nodes  $a-a'$  is simulated; for the FW configuration, the conductance characteristic between one surface node  $b$  outside FW and another node inside FW ( $b'$ ) is simulated. To observe this improvement for various frequencies, note that in Fig. 10(e), the anode-to-cathode conductance of the FW structure decreases significantly under 10 GHz and is still half an order smaller than that of the P-well structure from 10 to 100 GHz. This simulation intends to show the change of substrate conductance's characteristic inducing by FW, but it cannot give the exact variation quantity of the effective substrate resistance.

#### IV. SPIRAL INDUCTOR MODEL FOR SKIN EFFECT

Several equivalent-circuit models have been developed with conventional configurations and successfully used to model most on-chip spiral inductors [6], [13], [20] for designing RF ICs. In Fig. 11(a), the spiral coil structure is represented by an ideal inductance  $L_s$ , external connection wires inductance  $L_{x1}$ , and  $L_{x2}$ , a series resistance  $R_s$  and an interwire capacitance  $C_x$ . The shunt parasitics result from a combination of oxide capacitance ( $C_{ox1}$  and  $C_{ox2}$ ) between spiral coil and substrate and substrate parasitics ( $R_{sub1}$ ,  $R_{sub2}$ ,  $C_{sub1}$ , and  $C_{sub2}$ ). Correlated with previous works [6], [13], [20],  $L_{x1}$  and  $L_{x2}$  are introduced in Fig. 11 to model inevitable external connection wires' inductance in real circuit layout.

Fig. 12(a) and (b) shows the normalized inductance ( $L(\text{frequency})/L(100 \text{ MHz})$ ) versus frequency for inductors with various numbers of turn and various inner diameters. Here, for inductors with fewer numbers of turn and smaller inner diameter, the inductance reduction with frequency becomes more apparent. This phenomenon is induced by the substrate skin effect and increased negative mutual inductance, which form frequency-dependent inductance and resistance [9], [17]. For spirals in CMOS technology, the skin effect mode is the dominating propagation mode near the first resonant frequency [17], [18]. In other words, the substrate begins to behave as a lossy conductor wall. The loss effect can be incorporated into a frequency-dependent series resistance. When frequency increases, under skin-effect mode, the longitudinal current

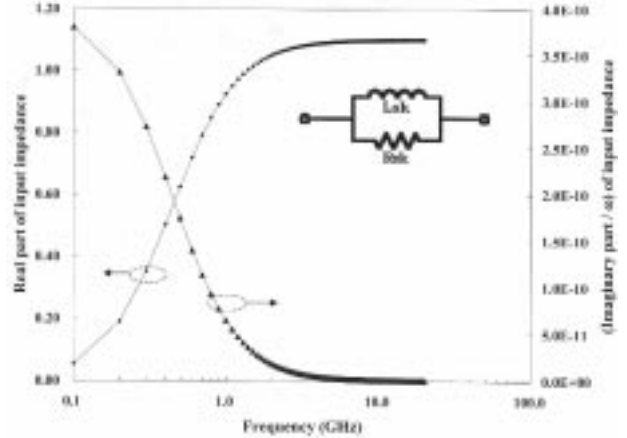


Fig. 14. Simulated frequency dependence of real part and (imaginary part/ $\omega$ ) of input impedance for  $R_{sk}$  and  $L_{sk}$  in parallel, where the  $R_{sk}$  and  $L_{sk}$  values are listed in the table in Fig. 13.

near Si-SiO<sub>2</sub> interface will lower the inductance. Because the skin depth (2.6  $\mu\text{m}$ ) of Al metal layer [15] at 1 GHz is larger than metal-2 thickness, the skin effect in metal layer could be ignored for our experiment. The conventional lumped model in Fig. 11(a) cannot model correctly the inductance reduction and the series resistance increase characteristics with a frequency increase. In previous works [8], [9], a series frequency-dependent resistance was added to describe the resistance change due to the substrate skin effect, but this model is not easily performable into circuit simulator and lacks the eddy current effect and parameter extraction methodology. In this work, a simplified lumped model is presented to address the characteristic of frequency-dependent inductance and resistance simultaneously. Here, one resistance  $R_{sk}$  and inductor  $L_{sk}$  have been adopted into the main inductor current path, with  $R_{sk}$  and  $L_{sk}$  combined in parallel as shown in Fig. 11(b). At low frequency, signal passes through  $L_s$ ,  $L_{sk}$ , and  $R_s$  and propagates between port 1 and port 2. At a higher frequency, the signal will be traveling less through  $L_{sk}$  due to increased impedance, but more through  $R_{sk}$  instead, representing the effect of increased energy loss. The frequency dependences of the real part and the normalized imaginary part (imaginary part/ $\omega$ ) of input impedance for  $R_{sk}$  and  $L_{sk}$  in parallel are shown in Fig. 14, which demonstrates the quantities of the series resistance's increase and the inductance's reduction with increased frequency to model the skin effect and the eddy current effect. Here, the  $R_{sk}$  and  $L_{sk}$  values are from the parameters list table in Fig. 13. The power loss at  $R_{sk}$  is equivalently the power loss in the substrate due to the skin effect. For an inductor with  $T = 4$  and  $A = 64 \mu\text{m}$ , the agreement of inductance and quality factor between measurement and simulation is good, as shown in Fig. 13. The inserted table in Fig. 13 shows all parameters used to form a lumped model for this inductor. The errors of both real part and an imaginary part for four two-port S-parameters are below 10% for frequency lower than 7.6 GHz. This model can be used for various inductor configurations. Furthermore, from the aspect of device modeling, this model is easy to be extracted and implemented into circuit simulators.

## V. CONCLUSION

A complete characterization of an on-chip inductor has been presented. Scaling of inductors with geometry and configuration factors has been investigated. The quality factor and noise isolation improvement using a floating N-well in the substrate has been verified. The floating well can improve coupling noise under 3 GHz, but has to be accompanied by a  $P+$  guard ring above 3 GHz for noise improvement. Noise propagation and isolation effects in various substrate types are also investigated including P-well, N-epitaxial layer, and floating well. Finally, a circuit simulation model has been developed to consider the frequency-dependent series resistance and inductance induced by the skin effect and eddy current effect.

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