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Analysis of Application of the IDDQ Technique to the Deep Sub-Micron VLSI Testing

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Abstract. In this work, IDDQ current for the deep sub-micron VLSI in year 2011 is estimated with a statistical approach according to the International Technology Roadmap for Semiconductors 1999 Edition considering process variations and different input vectors. The estimated results show that the standard deviation of the IDDQ current is proportional to the square root of the circuit size and the IDDQ currents of the defect-free and the defective devices, which are of the size up to 1×10^7 gates, are still differentiable under the condition of random process deviations and input vectors. Two new IDDQ testing schemes, which detect the defective current based on the two separate IDDQ distributions, are proposed. From the study, it is concluded that IDDQ testing is still applicable for the deep sub-micron VLSI for the next ten years.

Keywords: IDDQ testing, deep sub-micron, VLSI

1. Introduction

IDDQ testing is an effective testing technique to detect many non-stuck-at fault defects, such as gate oxide defects and bridging faults, which are likely to become more important due to the continued shrinking of device dimensions [2, 3]. However, recently, a work by Williams et al. [10] reported that it will be difficult to apply the IDDQ testing to the deep sub-micron VLSI due to the increased sub-threshold current of the MOS transistor which makes the IDDQ for the defective devices be difficult to be differentiated from that of the

good devices. This is especially true if the distribution of the IDDQ current due to the process variation and different input vectors, which cause different magnitude of IDDQ current, is considered.

The IDDQ current of VLSI devices is intrinsically statistical, i.e., it falls into a distribution, usually normal distribution. The "mean" and "standard deviation" are two important parameters to be considered when a line is to be drawn between the IDDQ currents of good devices and defective devices. Recently, Lu et al. proposed a new current difference testing scheme which, instead to measure the "mean", i.e., the absolute values of IDDQ currents, compares the IDDQ currents of a single defective chip under different input vectors [4]. If the additional defective current exceeds six times of the "standard deviation" of the IDDQ current distribution of good devices, the defective device is considered "detected". This greatly increases the resolution of differentiation of the good device and the defective device for the IDDQ testing.

In this work, the distributions of the IDDQ currents for the deep sub-micron CMOS in the year of 2011, which has a feature size of 50 nm, are studied considering both the process variation and the random input vectors. It is found that although the mean of the distribution of the IDDQ current is almost linearly proportional to the size of circuit, the standard deviation of the IDDQ distribution is proportional to the square root of the circuit size. For the worst case estimation for the VLSI of year 2011, the standard deviation is only approximately 5.67 μA for a circuit of the size of 1×10^7 gates while the minimum additional defect current is 34.1 μA. That means that the IDDQ currents of the good and defective devices are still differentiable. Based on the estimated results, two IDDQ testing schemes which can detect the defects in a deep sub-micron VLSI are proposed. Through this study, it is concluded that the IDDQ testing is still applicable to deep sub-micron CMOS VLSI for the next ten years.

2. Estimation of Defect-Free and Defective IDDQ

The IDDQ current is caused by several kinds of leakage currents which are sub-threshold current, reverse-biased p-n junction leakage current, gate-induced drain leakage current, bulk punch-through current and tunneling current [1]. All the leakage currents are affected by the process variation, the states of the circuit [9], and the input vector. In this section, the distributions of the IDDQ currents of the defect-free and defective CMOS devices will be analyzed considering the above factors. The analysis is of a hierarchical approach, i.e., starting from the transistor device level considering the process variation, to the circuit level considering the states of gates.

2.1. Estimation of Defect-Free IDDQ

In the deep sub-micron region, the sub-threshold current grows exponentially due to the scaled down of the threshold voltage. Hence, only the sub-threshold current of the MOS transistor is considered.

The sub-threshold current of a MOS is given by [6]:

$$I_s = \mu_0 \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L} V_t^2 \exp\left[\frac{V_{GS} - V_T + \eta V_{DS}}{nV_t}\right] \quad (1)$$

where μ_0 is the carrier surface mobility, ϵ_{ox} is the dielectric permitivity of oxide, T_{ox} is the oxide thickness, W is the channel width, L is the channel length, V_t is the thermal voltage, V_T is the threshold voltage, n is a technology dependent parameter and η models the drain induced barrier lowering (DIBL). The variation of the sub-threshold current is mainly caused by the variations of W, L, T_{ox} and V_T. Assuming that the process variation of W, L, T_{ox} and V_T are normal distributions, we can calculate the expected value and variance of sub-threshold current in a NMOS or PMOS transistor, $E[I_S]$ and $VAR[I_S]$, by [5]

$$\begin{aligned} E[I_s] = & \int_{\mu_W-3\sigma_W}^{\mu_W+3\sigma_W} \int_{\mu_L-3\sigma_L}^{\mu_L+3\sigma_L} \int_{\mu_{T_{ox}}-3\sigma_{T_{ox}}}^{\mu_{T_{ox}}+3\sigma_{T_{ox}}} \int_{\mu_{V_T}-3\sigma_{V_T}}^{\mu_{V_T}+3\sigma_{V_T}} I_s \\ & \times \frac{1}{\sqrt{2\pi}\sigma_W} \exp\left(-\frac{(W-\mu_W)^2}{2\sigma_W^2}\right) \\ & \times \frac{1}{\sqrt{2\pi}\sigma_L} \exp\left(-\frac{(L-\mu_L)^2}{2\sigma_L^2}\right) \times \frac{1}{\sqrt{2\pi}\sigma_{Tox}} \\ & \times \exp\left(-\frac{(T_{ox}-\mu_{T\,ox})^2}{2\sigma_{T_{ox}}^2}\right) \times \frac{1}{\sqrt{2\pi}\sigma_{V_T}} \\ & \times \exp\left(-\frac{(V_T-\mu_{V_T})^2}{2\sigma_{V_T}^2}\right) dW dL dT_{ox} dV_T \end{aligned} \quad (2)$$

$$\begin{aligned} E\left[I_s^2\right] = & \int_{\mu_W-3\sigma_W}^{\mu_W+3\sigma_W} \int_{\mu_L-3\sigma_L}^{\mu_L+3\sigma_L} \int_{\mu_{T_{ox}}-3\sigma_{T_{ox}}}^{\mu_{T_{ox}}+3\sigma_{T_{ox}}} \int_{\mu_{V_T}-3\sigma_{V_T}}^{\mu_{V_T}+3\sigma_{V_T}} I_s^2 \\ & \times \frac{1}{\sqrt{2\pi}\sigma_W} \exp\left(-\frac{(W-\mu_W)^2}{2\sigma_W^2}\right) \end{aligned}$$

$$\times \frac{1}{\sqrt{2\pi}\sigma_L} \exp\left(-\frac{(L-\mu_L)^2}{2\sigma_L^2}\right) \times \frac{1}{\sqrt{2\pi}\sigma_{T_{ox}}} \times \exp\left(-\frac{\left(T_{ox}-\mu_{T_{ox}}\right)^2}{2\sigma_{T_{ox}}^2}\right) \times \frac{1}{\sqrt{2\pi}\sigma_{V_T}} \times \exp\left(-\frac{\left(V_T-\mu_{V_T}\right)^2}{2\sigma_{V_T}^2}\right) dW dL dT_{ox} dV_T \tag{3}$$

$$VAR[I_s] = E^2[I_s] - E\left[I_s^2\right] \tag{4}$$

$$STD[I_s] = \sqrt{VAR[I_s]} \tag{5}$$

where μ_W, μ_L, $\mu_{T_{ox}}$, μ_{V_T}, and σ_W, σ_L, $\sigma_{T_{ox}}$, σ_{V_T} are the mean and the standard deviation of W, L, T_{ox} and V_T respectively.

For a CMOS logic gate, the subthreshold current is caused from the off-state MOS transistor(s) which is(are) either NMOS or PMOS transistors. The involved MOS transistors are determined by each state of the gate. Hence, the expected value and variance are state-dependent. They can be calculated from Eqs. (2)–(5) for each state.

For the circuit level, we start from the process variation. Under one input vector, the IDDQ of a circuit is a function of process variation. The logic simulator can determine all the states of the logic gates for a given input vector. Since the leakage distribution and the states of all CMOS gates are known, the total IDDQ of a circuit can be obtained by summing the currents of all gates. According to the central limited theorem [5], the defect-free IDDQ is a normal distribution. The mean is the summation of the means of all gates. Since the states of all gates have been determined, the leakage currents of all gates are mutually independent. The variance of a circuit is the summation of the variances of all gates. The standard deviation is the square root of the variation. Its expected value, $E[I_{DDQ}(p)]$, variance, $VAR[I_{DDQ}(p)]$, and standard deviation, $STD[I_{DDQ}(p)]$, are expressed as follows:

$$I_{DDQ}(p) = \sum_{i=1}^{N_g} I_{gate,i} \tag{6}$$

$$E[I_{DDQ}(p)] = \sum_{i=1}^{N_g} E[I_{gate,i}] \tag{7}$$

$$VAR[I_{DDQ}(p)] = \sum_{i=1}^{N_g} VAR[I_{gate,i}] \tag{8}$$

$$STD[I_{DDQ}(p)] = \sqrt{VAR[I_{DDQ}(p)]} \tag{9}$$

where $I_{gate,i}$ is the leakage of the ith gate. N_g is the gate number. $E[I_{gate,i}]$ and $VAR[I_{gate,i}]$ are the expected value and variance of the ith gate respectively.

Finally, the IDDQ distribution, which is not only a function of process variation but also input vector, can be obtained by simulating the logic simulator for a set of random vectors. From the conditional expectation [5], the expected value, $E[I_{DDQ}(p, v)]$, variance, $VAR[I_{DDQ}(p, v)]$, and standard deviation, $STD[I_{DDQ}(p, v)]$, of IDDQ for a set of N_v random vectors are expressed as follows:

$$E[I_{DDQ}(p, v)] = \frac{1}{N_v} \sum_{j=1}^{N_v} E_j[I_{DDQ}(p)] \tag{10}$$

$$VAR[I_{DDQ}(p, v)] = \frac{1}{N_v} \sum_{j=1}^{N_v} (E_j[I_{DDQ}(p)] - E_j[E[I_{DDQ}(p, v)]])^2 + \frac{1}{N_v} \sum_{j=1}^{N_v} Var_j[I_{DDQ}(p)] \tag{11}$$

$$STD[I_{DDQ}(p, v)] = \sqrt{VAR[I_{DDQ}(p, v)]} \tag{12}$$

The defect-free IDDQ of a circuit can then be obtained by this hierarchical approach. However, sometimes we need a simple formula to calculate the standard deviation for a defect-free circuit. The variance of a circuit is the summation of the variances of all gates (Eq. (8)). The standard deviation is the square root of the variation. Hence, for the worst case, the maximum standard deviation, $STD_{\max}[I_{DDQ}]$, of a circuit can be expressed as:

$$STD_{\max}[I_{DDQ}] = \text{Max}\sqrt{N_g} STD[I_{gate}] \tag{13}$$

2.2. *Estimation of Defective IDDQ*

For the defective circuit, the activated defect draws an excessive current. The additional current is added to the total current. The total IDDQ current can be expressed as follows:

$$I_{defective} = \sum_{i=1}^{N_g} I_{gate,i} + I_d \tag{14}$$

where I_d is the additional defective current.

3. Estimated Results

3.1. Defect-Free IDDQ

In order to estimate the subthreshold current for the feature technology, the values of technology parameters are given and shown in Table 1. The values of T_{ox}, L and V_{DD} are predicted by the International Technology Roadmap for Semiconductors (ITRS) 1999 Edition for the year 2011 [8]. From Eq. (1) and Table 1, the subthreshold currents per unit channel width are 81.3 nA/μm and 37.9 nA/μm for NMOS and PMOS respectively. These estimated values are in the same order as the values predicted by the Roadmap. For the estimation of IDDQ in CMOS gates, the values of width for inverter, 2-input NAND and 2-input NOR are shown in Table 2. The minimum width is assumed 0.1 μm. The process variation within a single chip is expected smaller then the variation between different chips. The values of process variations between different chips (called off-chip here) and within a single chip (called on-chip) are shown in Table 3, where the values of 3_{σ_L} and $3_{\sigma_{VT}}$ for off-chip ICs are predicted by the Roadmap. The values for on-chip ICs are assumed as half of the values for off-chip ICs.

From Eqs. (2)–(5) and Tables 1–3, the IDDQ distribution of CMOS gates for each state can be estimated. Table 4 shows the expected values and standard deviation of inverter, 2-input NAND and 2-input NOR for each state for off-chip and on-chip ICs respectively, where the first value is the expected value and the second one is the standard deviation. The maximum standard deviations of the gates are 3.692 nA and 1.793 nA for off-chip and on-chip ICs respectively. The maximum standard deviations of the gates for other W/L ratios can be obtained by the same procedure and they are shown in Table 5.

The magnitude of IDDQ of a CMOS circuit can be calculated by Eq. (6). Fig. 1 shows the simulated result on the sample histogram of the defect-free IDDQ current for the same circuit under 2000 random input vectors. From this figure, it can be seen that the defect-free IDDQ is a normal distribution. The standard deviation is only 24.65 nA, which is small as compared with the expected value of 39.13 μA.

The expected value and standard deviation of a CMOS circuit can be obtained by Eqs. (6)–(12). Fig. 2 shows the expected values versus the gate number for 2000 random input vectors for off-chip and on-chip c6288 circuits. Here the gate number means the partitioned size of circuit. The solid line is for the off-chip IC and the dash line is for the on-chip IC. From this

Table 1. Values of technology parameters for the year 2011.

μ_n	μ_p	T_{ox}	L	V_t
750 cm/v-s	350 cm/v-s	0.7 nm	50 nm	25 mV
V_T	V_{DD}	$W_{\min}$	n	η
0.15 V	0.6 V	0.1 μm	1.03	0.01

Table 2. Values of width for inverter, 2-input NAND and 2-input NOR.

	INVERTER	NAND	NOR
PMOS	0.2 μm	0.2 μm	0.4 μm
NMOS	0.1 μm	0.2 μm	0.1 μm

Table 3. Values of process variations for off-chip and on-chip ICs.

	$3\sigma_W$	$3\sigma_L$	$3\sigma_{T_{ox}}$	$3\sigma_{V_t}$
Off-chip	10 nm	3.2 nm	0.07 nm	17 mV
On-chip	5 nm	1.6 nm	0.035 nm	8.5 mV

Table 4. Expected values and standard deviation of inverter, 2-input NAND and 2-input NOR for off-chip ICs and on-chip ICs.

	INVERTER	NAND	NOR
off-chip			
00	8.130, 1.862 nA	14.472, 3.286 nA	16.260, 2.633 nA
01	7.588, 1.723 nA	16.260, 3.692 nA	15.176, 3.439 nA
10		16.260, 3.692 nA	15.176, 3.439 nA
11		15.176, 2.437 nA	13.507, 3.061 nA
on-chip			
00	7.974, 0.904 nA	14.195, 1.596 nA	15.948, 1.278 nA
01	7.443, 0.837 nA	15.948, 1.793 nA	14.885, 1.670 nA
10		15.948, 1.793 nA	14.885, 1.670 nA
11		14.885, 1.183 nA	13.248, 1.486 nA

The first value is the expected value and the second one is the standard deviation.

Table 5. The maximum standard deviation, σ_g, among all gates for different W/L ratios for the year of 2011.

W/L	20	15	10	5	3	2
σ_g nA (off chip)	38.82	27.62	18.41	9.210	5.530	3.692
σ_g nA (on chip)	17.88	13.41	8.941	4.472	2.685	1.793

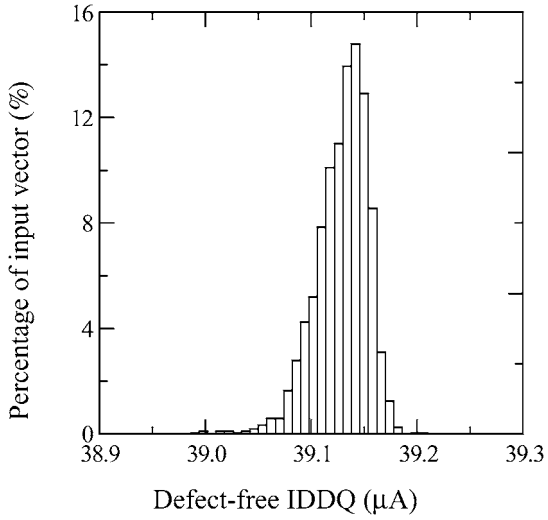


Fig. 1. The simulated result on the sample histogram of the defect-free IDDQ current for the ISCAS'85 circuit c6288 under 2000 random input vectors.

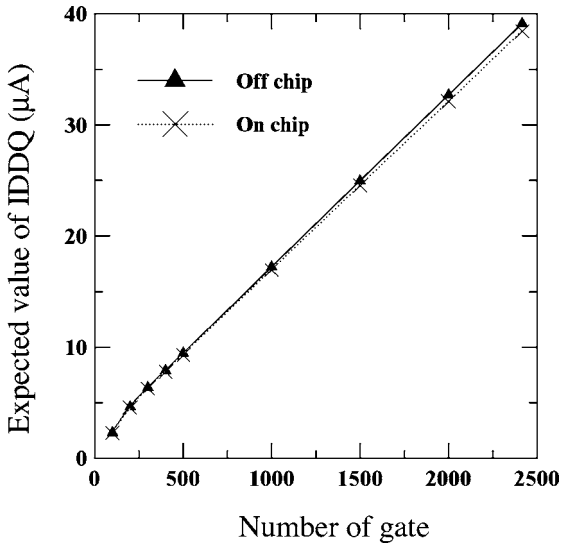
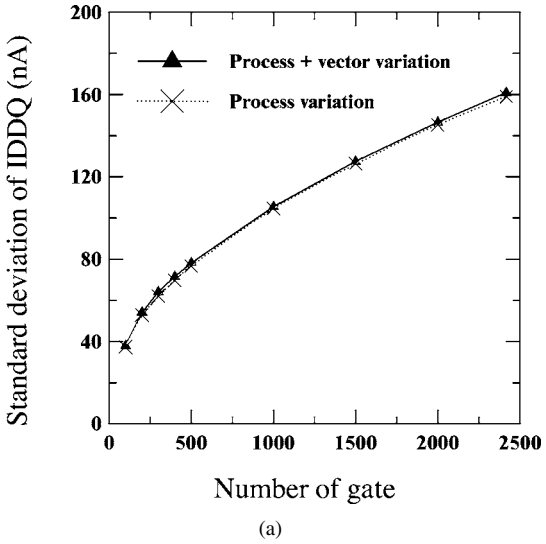


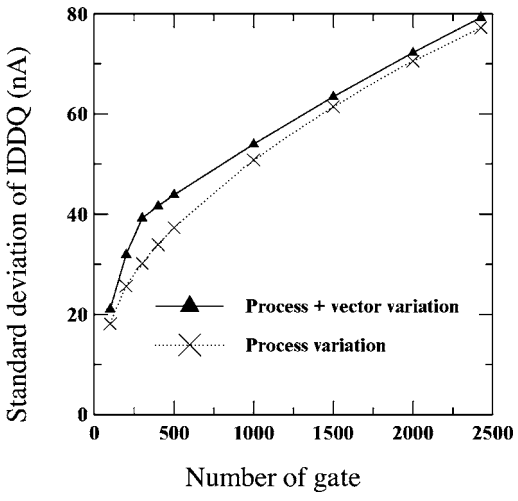
Fig. 2. The expected values of IDDQ versus the gate number for 2000 random input vectors for off-chip and on-chip c6288 circuits.

figure, it can be seen that the defect-free IDDQ is almost linearly proportional to the size of the circuit. Simulation for other benchmark circuits shows the similar result.

The IDDQ of a circuit is a function of process variation and input vector. The standard deviation due to the process variation can be obtained from Eqs. (8) and (9)



(a)



(b)

Fig. 3. (a) The standard deviations of defect-free IDDQ versus the gate number for off-chip c6288 circuit. The dash line is the standard deviation due to the process variation and the solid line is the standard deviation due to the process variation and different input vectors. (b) The standard deviations of defect-free IDDQ versus the gate number for on-chip c6288 circuit. The dash line is the standard deviation due to the process variation and the solid line is the standard deviation due to the process variation and different input vectors.

while the standard deviation due to the process variation and input vector can be obtained from Eqs. (11) and (12). Fig. 3(a) and (b) shows the standard deviations of defect-free IDDQ versus the gate number for off-chip and on-chip c6288 circuits respectively. The

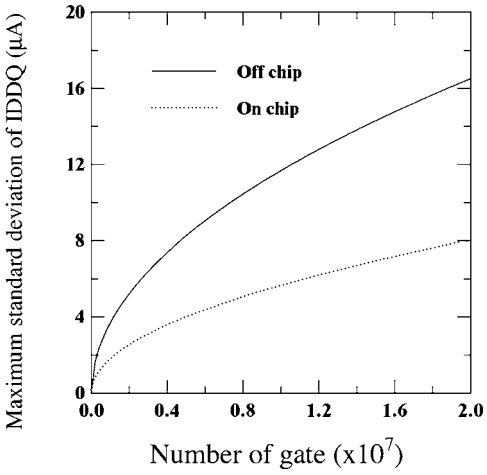


Fig. 4. The simulation result of maximum standard deviation for off-chip and on-chip ICs for the technology of the year 2011. The solid line is for off-chip ICs and the dash line is for on-chip ICs.

dash lines are the standard deviation due to the process variation while the solid lines are the standard deviation due to the process variation and different input vectors. From these two figures, they can be seen that the solid lines approach to the dash lines as the size of circuit increases. That is: the process variation dominates the IDDQ variation of a large circuit. From Eqs. (8) and (9), the standard deviation is proportional to the square root of the circuit size.

For the worst case, the maximum standard deviation of a circuit can be obtained from Eq. (13). Fig. 4 shows the simulated results of maximum standard deviation for W/L ratio of 2 for off-chip and on-chip ICs. The solid line is for off-chip ICs and the dash line is for on-chip ICs. The maximum standard deviation is only 16.5 μA for off-chip ICs and 8.02 μA for on-chip ICs even the gate number is up to 2×10^7. Simulation for other W/L ratios shows the similar results.

3.2. *Defective IDDQ*

Bridging defect resistances have been measured using a process defect monitor for CMOS technology [8]. The majority of the bridges were found to have low resistances (below 500 Ω). However, a small percentage was found in the range of 500 Ω to 20 KΩ. Spectroscopic analysis of these high resistive bridges showed that the material of the defects could not cause the high resistances. They could be the geometry of the defects resulting in one or two poor contacts. The low resistance is expected to have a smaller value in the future due to the smaller space between two bridging nodes. Experiments have shown that more than 95% of the bridging defect resistance values are equal to or less than 1 kΩ. In this work, the value of 1 kΩ is used to estimate the excess defect current. For the estimation of minimum defect current, it is assumed that the defect is located between the output of a two-input NOR gate and the output of a two-input NAND gate. The on currents of PMOS and NMOS, which are predicted by 1999 ITRS Roadmap for year of 2011, are 750 μA/μm and 350 μA/μm respectively. V_{DD} is 0.6 V. Then, the values of on resistance for PMOS and NMOS are 1.714 KΩ-μm and 0.8 KΩ-μm respectively. Hence the minimum defect current is as:

$$I_{d,\min} = \frac{V_{DD}}{2R_{on,PMOS} + R_{defect,\max} + 2R_{on,NMOS}} = 34.1\ \mu\text{A} \quad (15)$$

The minimum defective current, $I_{d,\min}$, which are shown in Table 6, for different minimum W/L ratios for the year of 2011 are also calculated.

Table 6. The minimum defective current for different W/L ratios for the year of 2011.

W/L	20	15	10	5	3	2
I_d μA	226	187	139	78.7	49.8	34.1

4. The Maximum Circuit Size for Partitioning

We have shown that the standard deviation is proportional to the square root of circuit size. As the size of CUT is increased to a very large value, 6σ of the CUT will be larger than the additional defective current. That is: the two distributions of defect-free and defective IDDQ will be partially overlapped. Fig. 5(a) depicts this situation where 6σ of the CUT is larger than the additional defective current. In order to separate the two distributions, the CUT should be partitioned into several sub-circuits. The 6σ of sub-circuits should be smaller than the additional defective current, $I_{d,\min}$. The IDDQ testable scheme is shown in Fig. 5(b) in which the 6σ of sub-circuits is smaller than the additional defective current so that the two distributions are differentiable. From Eq. (13) and Table 5, the maximum partition size for different W/L ratios for the year of 2011 are shown in Table 7.

Table 7. The maximum partition size (gate number) for different W/L ratios for the year of 2011.

W/L	20	15	10	5	3	2
Size (off chip)	1×10^6	1.2×10^6	1.5×10^6	2×10^6	2.2×10^6	2.3×10^6
Size (on chip)	4.4×10^6	5.4×10^6	6.7×10^6	8.6×10^6	9.5×10^6	1×10^7

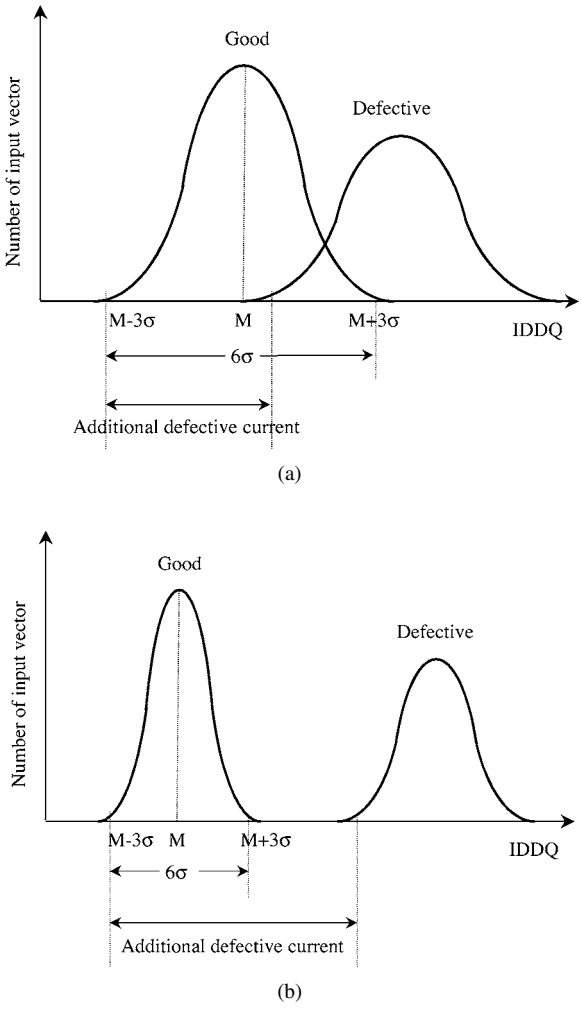


Fig. 5. (a) 6σ of the CUT is larger than the additional defective current so that the two distributions of defect-free and defective IDDQ overlap partially. (b) 6σ of sub-circuits smaller than the additional defective current so that the two distributions are separated.

5. Testing Schemes Based on Estimated IDDQ

In order to distinguish the non-overlapped distributions, we propose two IDDQ testing schemes to detect the current difference of the deep sub-micron VLSI.

5.1. *Current Difference Scheme I*

Fig. 6 shows the first testing scheme. The IDDQ currents of the CUT are measured by applied several vectors. If the defect is activated by some one vector, it will draws an additional current in the IDDQ. If the IDDQ difference between two vectors is greater than 6 times of standard deviation, $6\sigma_{\text{on-chip}}$, the CUT is declared as a faulty circuit. The standard deviation of the CUT should be estimated before IDDQ testing. The measurement of IDDQ of this scheme can be either measured by external current sensors or built-in current sensors (BICSs).

5.2. *Current Difference Scheme II*

Fig. 7 shows the second testing scheme which compares the IDDQ currents between two chips under the same vector. If the IDDQ difference is greater than $6\sigma_{\text{off-chip}}$, the chip, which draws a larger IDDQ, exists at least one defect. The IDDQ measurement of this scheme can only be measured by external current sensors.

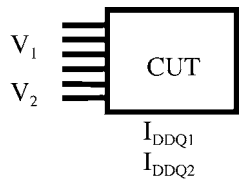


Fig. 6. Current difference scheme I. The IDDQ currents of CUT are measured for several testing vectors.

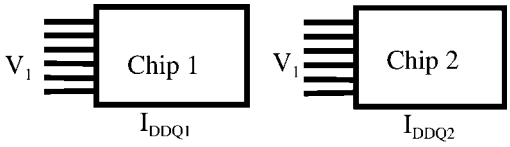


Fig. 7. Current difference scheme II. The IDDQ currents of two chips are measured under the same input vector.

Table 8. The maximum partition size of the proposed two IDDQ testing schemes for $W/L = 2$ for the CMOS technology of year 2011.

	Scheme I	Scheme II
maximum partition size	1×10^7	2.3×10^6

The IDDQ distributions have been simulated by considering the process variation and different input vectors. The simulated results show that the process variation dominates the IDDQ variation. For testing scheme I, IDDQ currents are measured on-chip (for the same chip) while for testing scheme II, they are measured off-chip (for different chips). The variance of an on-chip ICs is expected to be smaller than that of off-chip ICs. Hence, the IDDQ testing scheme I is expected to have a better resolution. The maximum partition size of the above two schemes for $W/L = 2$ for the year of 2011 are shown in Table 8. For a CUT containing 1×10^8 gates as an example, the minimum numbers of sub-circuits for on-chip testing (scheme I) and off-chip testing (scheme II) are 10 and 44 respectively for the year 2011. If the partition is based on the estimation of the above procedure rather than based on the worst case, the partition number can be further reduced. Hence, in this work, we conclude that IDDQ testing, which is based on the current difference scheme, is still applicable for the next ten years.

6. Conclusion

The distribution of defect-free IDDQ of a CMOS deep submicron VLSI circuit for the year of 2011 has been estimated. The estimation considers the process variation and different input vectors. The estimated results show that the process variation dominates the IDDQ variation in a VLSI circuit. The expected value is almost linearly proportional to the size of the circuit. However, the standard deviation is proportional to the square root of the circuit size.

In this work, the model of the subthreshold current is based upon the present day deep sub-micron VLSI device, and the parameter values were from the International Technology Roadmap for Semiconductors 1999 Edition. The models and parameter values for estimating IDDQ currents may be modified for the year of 2011. However, the methodology used can be still applicable to estimate the IDDQ currents.

The defect-free and defective IDDQ distributions of a CMOS VLSI containing 1×10^7 gates are still differentiable for the year of 2011. Two IDDQ testing schemes, which detect the defective current of the defective distribution from the good distribution, have been proposed. The scheme which compares IDDQ currents on the same chip ICs has a better resolution than the scheme which measures IDDQ currents for different chips. We conclude that the IDDQ testing still applicable for CMOS VLSI for the next ten years.

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