Arsenic/Phosphorus LDD Optimization by Taking Advantage of Phosphorus Transient Enhanced Diffusion for High Voltage Input/Output CMOS Devices

Howard Chih-Hao Wang, Chih-Chiang Wang, Carlos H. Diaz, *Senior Member, IEEE*, Boon-Khim Liew, Jack Yuan-Chen Sun, *Fellow, IEEE*, and Tahui Wang, *Senior Member, IEEE*

***Abstract*—Optimization of a LDD doping profile to enhance hot carrier resistance in 3.3 V input/output CMOS devices has been performed by utilizing phosphorus transient enhanced diffusion (TED). Hot carrier effects in hybrid arsenic/phosphorus LDD nMOSFET's with and without TED are characterized comprehensively. Our result shows that the substrate current in a nMOSFET with phosphorus TED can be substantially reduced, as compared to the one without TED. The reason is that the TED effect can yield a more graded n^- LDD doping profile and thus a smaller lateral electric field. Further improvement of hot carrier reliability can be achieved by optimizing arsenic implant energy. Secondary ion mass spectrometry analysis for TED effect and two-dimensional (2-D) device simulation for electric field and current flow distributions have been conducted. The phosphorus TED effects on transistor driving current and off-state leakage current are also investigated.**

***Index Terms*—Hot carriers, MOS devices, transient enhanced diffusion.**

I. INTRODUCTION

INPUT/OUTPUT (I/O) devices with higher operation voltage are demanded along with high-performance and low-voltage core devices in today's CMOS technology. This requirement has stimulated considerable efforts toward the development of dual gate-oxide process, i.e., thinner gate oxide for core devices and thicker gate oxide for I/O devices. To minimize processing cost, I/O devices and core devices usually share the same substrate architecture, thus eliminating the need for extra well photo mask. Short channel effect (SCE) has been a major limiting factor for core device design. Super-steep retrograde channel, shallow source/drain junction, and pocket implants are necessitated to achieve better control of short channel effect [1]–[3]. These process schemes, however, are detrimental to device hot carrier reliability [4]. In core devices, hot carrier effects can be relieved by using reduced supply voltage ($<$2.0 V) whereas hot carrier reliability in I/O devices becomes a major challenge in dual gate-oxide process.

The design and the fabrication procedure of a lightly doped drain (LDD) are important to I/O device reliability. A hybrid arsenic/phosphorus (As/P) LDD structure is currently adopted for high voltage I/O transistors [5]. Due to the low diffusivity, arsenic is preferred in forming shallow junctions with a steep doping distribution. On the other side, the abruptness of the arsenic junction increases the peak electric field in the channel and deteriorates hot carrier resistance. The use of phosphorus in LDD implant can help grading the n^- LDD doping profile and results in a smaller electric field. By modifying the phosphorus diffusion behavior, one can further improve device hot carrier reliability. In this paper, it is our intention to optimize the arsenic/phosphorus LDD doping profiles by utilizing an enhanced phosphorus diffusion mechanism.

It has been reported that supersaturated silicon interstitials can be introduced during source/drain extension and pocket implants, which give rise to anomalous transient enhanced diffusion (TED) in the early stage of the subsequent thermal cycle [6]. The diffusivity enhancement can be orders of magnitude higher than the intrinsic value [7]. In order to ensure a desired dopant profile in pocket and S/D extension regions in core devices, rapid thermal anneal (RTA) prior to sidewall spacer formation is necessary to suppress the TED effects [8], [9]. On the contrary, phosphorus TED effect [10], [11] is advantageous in certain aspects in I/O devices since it can grade the n^- LDD doping profile and improves hot carrier reliability [12]. A comprehensive study of the phosphorus TED effects on the n^- junction profile, hot carrier reliability, driving current and off-state leakage current in I/O devices will be performed. Various As/P LDD nMOSFET's with and without TED are fabricated. Effects of arsenic LDD implant energy are investigated. SIMS analysis and two-dimensional (2-D) device simulation are also conducted.

Manuscript received May 17, 2001; revised August 27, 2001. H. C.-H. Wang and T. Wang were supported by the National Science Council, Taiwan, R.O.C., under Contract NSC89-2215-E009-034.

H. C.-H. Wang is with the Device Technology and Modeling Department, R&D, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C. and also with the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: chwang@tsmc.com.tw).

C.-C. Wang, C. H. Diaz, and B.-K. Liew are with the Device Technology and Modeling Department, R&D, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C. (e-mail: chwang@tsmc.com.tw).

J. Y.-C. Sun is with the Logic Technology Division, R&D, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C.

T. Wang is with the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(02)00219-8.

0018–9383/02$17.00 © 2002 IEEE

TABLE I
THE MAJOR STEPS IN TWO CMOS PROCESSES

Process A	Process B
Poly gate definition	Poly gate definition
S/D extension and pocket implants for core device and I/O PMOS	S/D extension and pocket implants for core device and I/O PMOS
As/P nLDD implants for I/O NMOS	***RTA***
RTA	***As/P nLDD implants for I/O NMOS***
Nitride spacer deposition	Nitride spacer deposition
Source/Drain Formation	Source/Drain Formation

II. DEVICE FABRICATION

To explore the phosphorus TED effect, two process sequences are employed for a deep submicron dual gate-oxide CMOS technology (Table I). In process A, RTA is applied after S/D extension and pocket implants for core devices and the As/P LDD implant for I/O devices. In process B, the sequence of the As/P LDD implant and RTA is reversed and other steps are the same. It should be noted that the I/O devices in process B will have phosphorus TED during subsequent nitride spacer deposition but core devices in process A and B have exactly the same fabrication procedures. The nitride spacer deposition temperature and time are 750 °C and 2 hours respectively. Four kinds of I/O devices are fabricated with the two processes. Device A1 is made with process A and device B1 is with process B. Device A2 is the same as device A1 except that the phosphorus dosage is increased by 20%. Device B2 is the same as device B1 except for arsenic implant energy being two times higher. All the samples have a gate oxide thickness of 70 Å. The gate length is from 0.26 μm to 0.5 μm. The supply voltage for the I/O devices is 3.3 V.

III. RESULTS & DISCUSSION

A. Effects of Phosphorus TED

The SIMS result of the phosphorus doping profiles after all of processes in A1, A2, and B1 devices are drawn in Fig. 1. The x-axis in the figure denotes the depth in substrate. Device B1 apparently has a more graded phosphorus doping profile than A1 and A2 due to TED. Note that adding phosphorus dose (device A2) simply increases the doping level, but does not affect the slope of the profile. The phosphorus TED effect on substrate current (I_{sub}) in a 0.35 μm gate-length device is shown in Fig. 2. The measurement drain bias is 3.6 V (10% above the supply voltage for over-stress). Devices A1 and A2 (without TED) have nearly the same substrate current while device B1 (with TED) has a smaller substrate current. The substrate current reduction is nearly 30%. This remarkable reduction is in agreement with the SIMS profile in Fig. 1. The simulation result from MEDICI [13] in the inset of Fig. 2 also confirms a smaller lateral electric field in device B1. From the result, it can be concluded

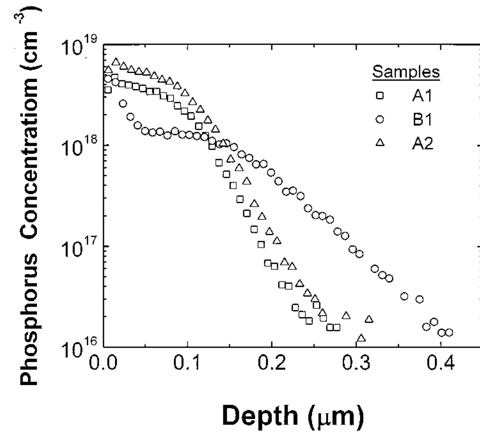

Fig. 1. Phosphorus SIMS profiles after all of processes. The x-axis denotes the depth in substrate.

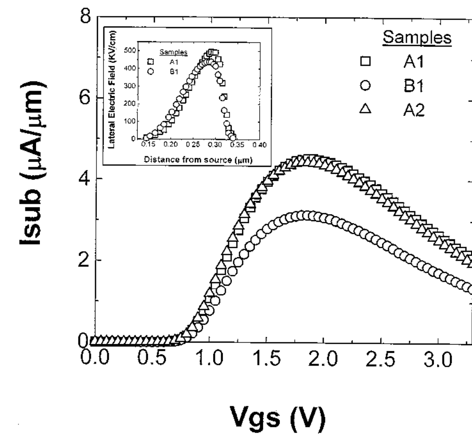

Fig. 2. Substrate current versus gate bias in 0.35 μm gate length devices. $V_{\mathrm{ds}} = 3.6$ V. Simulated lateral electric field at $V_{\mathrm{ds}} = 3.6$ V and $V_{\mathrm{gs}} = 1.8$ V is shown in the inset.

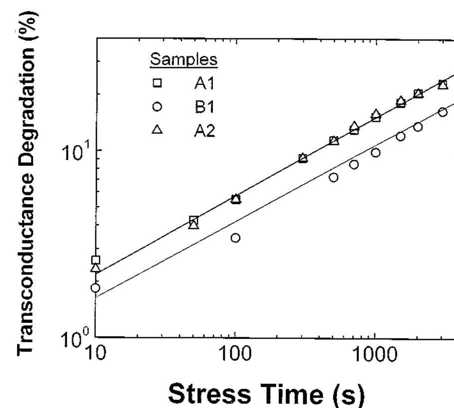

Fig. 3. Maximum transconductance degradation versus stress time. The stress drain bias is 4.5 V and gate bias is 2.1 V.

that phosphorus TED can be utilized as a more effective approach to improving hot carrier resistance, as compared to other methods such as a straight phosphorus dose change. In Fig. 3, we present the stress-time dependence of hot carrier transconductance (G_{m}) degradation in the three devices. The stress is performed in a maximum I_{sub} condition, i.e., $V_{\mathrm{ds}} = 4.5$ V and

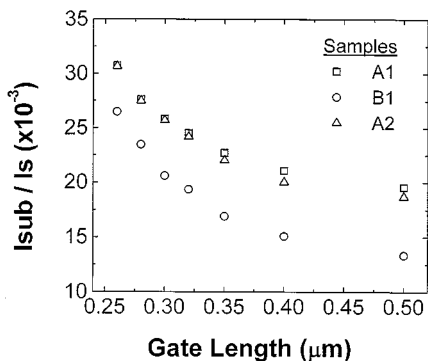

Fig. 4. Normalized maximum substrate current $(I_{\rm sub}/I_{\rm s})$ plotted against gate length.

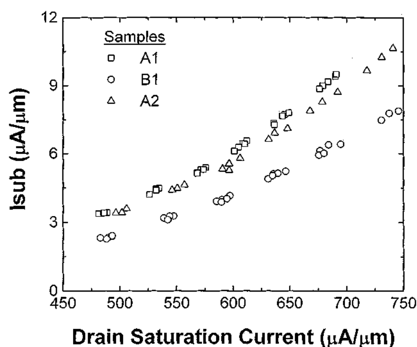

Fig. 5. Maximum substrate current versus drain saturation current.

$V_{\rm gs} = 2.1$ V for accelerated degradation. All the devices exhibit a power-law degradation rate. The power factor is about 0.4. The hot carrier lifetime, defined as 10% $G_{\rm m}$ degradation, is 360 s for device A1 and 1000 s for device B1. Thus, an improvement of hot carrier lifetime by three times is obtained in device B1 owing to the phosphorus TED.

The phosphorus TED effect in different gate length devices is examined in Fig. 4. $I_{\rm sub}$ is normalized to the source current in the figure. Evidently, device B exhibits smaller $I_{\rm sub}/I_{\rm s}$ for gate lengths from 0.26 μm to 0.5 μm. The current driving capability of the three devices is also compared. For a 0.35 μm device, the drain saturation current $(I_{\rm dsat})$ in device B1 is slightly larger than in device A1 for two reasons; First, the effective channel length in device B1 is shorter due to TED. The extracted effective channel length is 0.289 μm and 0.267 μm for device A1 and B1 respectively. Secondly, the LDD series resistance is dominated by arsenic implant condition and is therefore not affected by the phosphorus doping profile. In Fig. 5, maximum $I_{\rm sub}$ is plotted against $I_{\rm dsat}$ for various gate lengths.

It should be mentioned that phosphorus TED has minimal adverse effect on off-state drain leakage current $(I_{\rm off})$. For example, the measured drain leakage current in a 0.35 μm device at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 3.6$ V is 0.23 pA/μm in device A1, 0.26 pA/μm in device B1 and 0.29 pA/μm in device A2. $I_{\rm off}$ versus $I_{\rm dsat}$ characteristics for the three devices of various gate lengths is plotted in Fig. 6. Threshold voltage $(V_{\rm t})$ roll-off characteristics is also examined in Fig. 7. No significant difference is observed for a gate length down to 0.3 μm.

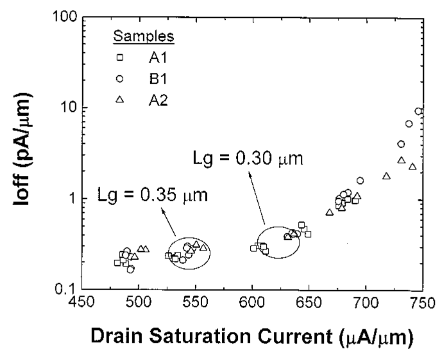

Fig. 6. $I_{\rm off}$ versus $I_{\rm dsat}$ characteristics for devices of various gate lengths. $I_{\rm off}$ is measured at $V_{\rm ds} = 3.6$ V and $V_{\rm gs} = 0$ V.

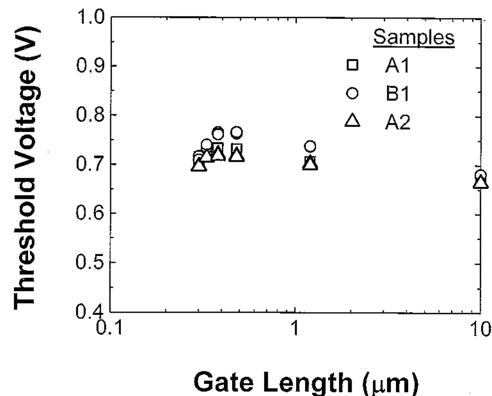

Fig. 7. Threshold voltage rolloff characteristics for the three devices.

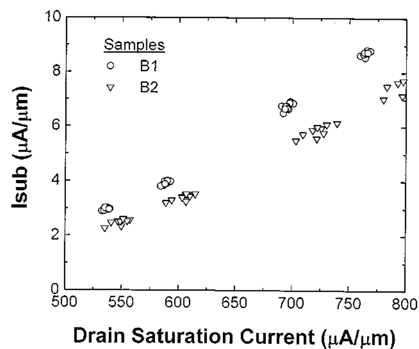

Fig. 8. Maximum substrate current versus drain saturation current. B1 and B2 both have phosphorus TED but have different arsenic implant energy.

B. Optimization of Arsenic Implant

Based on prior work [5], increasing the arsenic dose in hybrid LDD aggravates hot carrier reliability because of a more abrupt junction. In this work, due to a deeper phosphorus junction caused by phosphorus TED, we can increase arsenic implant energy for further optimization. Device B2 is fabricated with two times higher arsenic implant energy than B1. Further reduction of $I_{\rm sub}$ is demonstrated in Fig. 8. Fig. 9 compares the current path and the electric field contours in B1 and B2 obtained from a 2-D simulation. The shaded area represents an avalanche region with impact ionization rate $R_{\rm G} > 10^{28}$ cm^{-3} s^{-1}. In Device B2, the high field region moves deeper into the substrate. The current path is therefore separated from the high field region, thus leading to a smaller

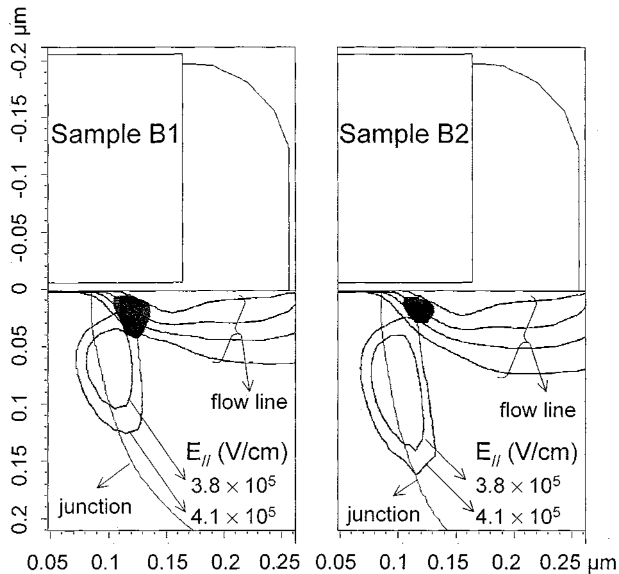

Fig. 9. Simulated lateral electric field contours and current path near the drain at $V_{ds}/V_{gs} = 3.6$ V/1.8 V for device B1 and B2. Shadowed area indicates an avalanche region with impact ionization rate $R_G > 10^{28}$ cm^{-3} s^{-1}.

avalanche region than in device B1. As a result, better hot carrier reliability can be obtained by higher arsenic implant energy. The hybrid LDD junction depth is still determined by the phosphorus profile although arsenic implant energy is higher. No obvious degradation of V_t roll-off characteristics is found down to gate length of 0.3 μm.

IV. Conclusion

We have proposed a process flow to take advantage of phosphorus TED to form a more graded LDD junction in I/O CMOS devices. By using this approach, substantial improvement of hot carrier resistance has been achieved. This process can effectively widen the performance-reliability window for I/O device design while maintaining suitability for core device development. With phosphorus TED and thus a deeper LDD junction, arsenic implant energy can be increased to further improve hot carrier reliability.

Acknowledgment

The SIMS measurement by TSMC's Failure Analysis Laboratory is greatly acknowledged.

References

[1] M. Rodder, S. Aur, and I.-C. Chen, "A scaled 1.8 V, 0.18 μm gate length CMOS technology: Device design and reliability considerations," in *IEDM Tech. Dig.*, 1995, pp. 415–418.

[2] H. Wakabayashi, M. Ueki, M. Narihiro, T. Fukai, N. Ikezawa, T. Matsuda, K. Yoshida, K. Takeuchi, Y. Ochiai, T. Mogami, and T. Kunio, "45-nm gate length CMOS technology and beyond using steep halo," in *IEDM Tech. Dig.*, 2000, pp. 49–52.

[3] K. Miyashita, H. Yoshimura, M. Takayanagi, M. Fujiwara, K. Adachi, T. Nakayama, and Y. Toyoshima, "Optimized halo structure for 80 nm physical gate CMOS technology with indium and antimony highly angled ion implantation," in *IEDM Tech. Dig.*, 1999, pp. 645–648.

[4] N. Bhat, P. Chen, P. Tsui, A. Das, M. Foisy, Y. Shiho, J. Higman, J.-Y. Nguyen, S. Gonzales, S. Collins, and D. Workman, "Hot carrier reliability consideration in the integration of dual gate oxide transistor process on a sub-0.25 m CMOS technology for embedded application," in *IEDM Tech. Dig.*, 1999, pp. 427–430.

[5] D. K. Nayak, M. Y. Hao, J. Umali, and R. Rakkhit, "A comprehensive study of performance and reliability of P, As, and Hybrid As/P nLDD junctions for deep-submicron CMOS logic technology," *IEEE Electron Device Lett.*, vol. 18, pp. 281–283, June 1997.

[6] A. E. Michel, W. Rausch, P. A. Ronsheim, and R. H. Kastl, "Rapid annealing and anomalous diffusion of ion implanted boron into silicon," *Appl. Phys. Lett.*, vol. 50, no. 7, pp. 416–418, 1987.

[7] S. S. Yu, H. W. Kennel, M. D. Giles, and P. A. Packan, "Simulation of transient enhanced diffusion using computationally efficient models," in *IEDM Tech. Dig.*, 1997, pp. 509–512.

[8] S. W. Crowder, P. M. Rousseau, J. P. Snyder, J. A. Scott, P. B. Griffin, and J. D. Plummer, "The effect of source/drain processing on the reverse short channel effect of deep sub-micron bulk and SOI NMOSFET's," in *IEDM Tech. Dig.*, 1995, pp. 427–430.

[9] H. Abiko, A. Ono, R. Ueno, S. Masuoka, S. Shishiguchi, K. Nakajima, and I. Sakai, "A channel engineering combined with channel epitaxy optimization and TED suppression for 0.15 μm n–n gate CMOS technology," in *VLSI Tech. Symp. Dig.*, 1995, pp. 23–24.

[10] M. D. Giles, "Transient phosphorus diffusion below the amorphization threshold," *J. Electrochem. Soc.*, vol. 138, no. 4, pp. 1160–1165, 1991.

[11] H. R. Soleimani, "An investigation of phosphorus transient diffusion in silicon below the solid solubility limit and at a low implant energy," *J. Electrochem. Soc.*, vol. 141, no. 8, pp. 2182–2187, 1994.

[12] H. C.-H. Wang, C. H. Diaz, B.-K. Liew, J. S.-C. Sun, and T. Wang, "Hot carrier reliability improvement by utilizing phosphorus transient enhanced diffusion for input/output devices of deep submicron CMOS technology," *IEEE Electron Device Lett.*, vol. 21, pp. 598–600, Dec. 2000.

[13] *Avanti Medici 2000.2 Manual*, ch. 2.

Howard Chih-Hao Wang was born in Taipei, Taiwan, R.O.C., in 1969. He received the B.S. degree in electronic engineering from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1992. Since 1997, he has been pursuing the Ph.D. degree in the Department of Electronic Engineering, NCTU.

In 1995, he joined Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, where he was initially responsible for the process integration and yield enhancement of 0.6 μm and 0.5 μm logic technology. Since 1997, he was involved in the device design in the Device Technology and Modeling Department at TSMC. He is currently working on the development of high-speed 0.1 μm CMOS device technology. His research interests involve device design and characterization for high-performance VLSI logic.

Chih-Chiang Wang received B.S. degree in physics science from catholic Fu-Jen University, Taiwan, R.O.C., and the M.S. degree in electro-optical engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1989 and 1991, respectively. In 1991, he joined Electronics Research and Service Organization (ERSO/ITRI) and worked for DRAM device design. Since 1998, he has worked at R&D group, Taiwan Semiconductor Manufacturing Company, Hsinchu. He has been engaged in process and device calibration/simulation for deep submicron technology.

Carlos H. Diaz (SM'98) received the M.S. and B.S. degrees in electrical engineering and physics from Universidad de Los Andes, Bogota D.C., Colombia, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign.

He joined the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C., in 1998 as a project manager for FEOL integration in 0.18 μm technology. Since 1999 he has been the program manager for Advanced Device Technology and TCAD responsible for design/integration of TSMC's logic transistor technology. Before joining TSMC, he was Member of Technical Staff, ULSI Laboratory, Hewlett-Packard Laboratories, Palo Alto, CA, working on process integration and device design since 1995. Before this, he was with Integrated Circuits Business Division at Hewlett-Packard working on physics reliability. He holds six U.S. patents, has published more than 40 papers in technical journals and international conferences, and has co-authored one book.

Dr. Diaz has been member of the Technical Program Committees for VLSI Technology Symposium, IEEE International Reliability Physics Symposium, and EOS/ESD Symposium.

Boon-Khim Liew received the B.S. degree from the California Institute of Technology, Pasadena, in 1985 and the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, in 1990.

From 1990 to 1993, he worked at Cypress Semiconductor as a Senior Technology Engineer in device engineering, responsible for MOS transistor design, device reliability, ESD and latch-up. From 1993 to 1995, he founded BTA Technology, Inc. and served as the President and CEO. At BTA, he was responsible for the development, marketing of simulation and SPICE modeling softwares. In December, 1995, he joined Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C., as the department manager for device technology and modeling. His responsibility includes advanced transistor design, SPICE modeling and TCAD simulation.

Jack Yuan-Chen Sun (S'79–M'83–SM'91–F'00) received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 1983.

He is presently Senior Director of Logic Technology Division at Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C. In the last three years, he has led the successful expansion and acceleration of TSMC low-voltage, high-performance, and low-power logic technology roadmap, e.g. cutting edge 0.18, 0.15, 0.13, and 0.1 μm logic families. He has 23 years of experience in Si IC technology, including R&D, technology transfer, and product qualification. He led many successful R&D projects that set world records and/or shape industry trends in CMOS, SOI, low-power CMOS, low temperature CMOS, bipolar, and SiGe HBT. He has authored and co-authored over 200 papers and many invited papers in technical journals and conferences. He holds eight U.S. patents and four IBM invention achievement awards.

Dr. Sun is an IEEE Fellow in recognition of his significant contribution to CMOS technology. He served as mentors of several SRC projects. He was an SRC PID TAB alternate member for IBM. He was a member (1995, 1996) and the chair (1997) of the CMOS subcommittee for IEDM. He is the chair of the PIDS TWG of TSIA and the TSIA representative in the ITRS PIDS TWG. He was a lecturer for a hot carrier reliability course at UC Berkeley Extension. He has authored and co-authored over 200 papers and many invited papers in technical journals and conferences. His latest invited papers are "Foundry Technology for the Next Decade" at 1998 IEDM, "CMOS Technology for 1.8 V and Beyond" at the 1997 International Symposium on VLSI Technology, Systems, and Applications.

Tahui Wang (M'85–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, in 1980 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot carrier phenomena characterization and reliability physics in VLSI devices, RF CMOS devices and nonvolatile semiconductor devices.

Dr. Wang was granted the Best Teacher Award by the Ministry of Education, R.O.C. He has served as technical committee member of many international conferences, among them IEDM and IRPS. His name was listed in *Who's Who in the World* in 2001.