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Performance Assessment of Processing and Delivery Times for Very Large Scale Integration Using Process Capability Indices

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Process quality and delivery time have received increasing attention in the highly competitive electronics industry. Many studies have proposed process capability indices (PCIs) to assess process effectiveness. However, methods to assess the performance in terms of processing and delivery times of products have seldom been discussed. The conventional PCIs can no longer assess the processing time (PT) and delivery time (DT) performance objectively or identify the relationship between PCIs and the non-conformance rate of PT or the conformance rate of DT. Lacking an effective performance index or an objective testing procedure to assess process/product performance will lead to inefficiency or a high manufacturing management overhead cost. Therefore, this study offers effective performance indices (i.e., PCIs) to assess the PT and DT performance for very large scale integration (VLSI). The uniformly minimum variance unbiased (UMVU) estimators of the proposed PCIs are derived under the assumption of a normal process distribution. The PCI estimators are then employed to construct a one-to-one relationship between the PCIs and the conformance rate of DT or non-conformance rate of PT, respectively. Finally, hypothesis testing procedures for the proposed PCIs are also developed. The testing procedure can be used to determine whether DT or PT can satisfy a customer's requirements.

Keywords: Delivery time; Normal distribution; Process capability index; Processing time; Uniformly minimum; Variance unbiased estimator; Very large scale integration

1. Introduction

As the global trends of dividing production work and reducing product life cycles continue, the build to order (BTO) model is gradually replacing the build to forecast (BTF) model, and is being used by direct-sale computer companies such as Dell and Gateway 2000. According to the investigations of Dickson [1] and Weber et al. [2], process quality and delivery time have been increasingly emphasised in the highly competitive electronics industry. Enhancing the quality and yield of the products, to satisfy customers' requirements, and delivering those products to the customers on time, are becoming the primary factors in enhancing manufacturers' marketing competitiveness. Lacking an effective performance index and a statistical testing procedure to assess process/product performance leads to inefficiency and a high manufacturing management overhead cost. Furthermore, manufacturers lose their market competitiveness if they do not perform well in product quality and delivery because the manufacturers' production schedule is delayed, and the customers' profits may even be damaged.

Process capability analysis is a convenient and powerful tool for measuring process performance and capability. Hence, process capability indices (PCIs) have been much studied. Many quality engineers and statisticians (e.g. [3–7]) have proposed methodologies for assessing product/process quality. Although this work has received considerable attention and related evaluation methods have been developed, the processing time (PT) and delivery time (DT) performance of products/processes has seldom been discussed. The importance of PT and DT of products is increased under the BTO model. Conventional PCIs can no longer assess the PT and DT performance objectively or identify the relationship between PCIs and the non-conformance rate of PT or the conformance rate of DT.

Figure 1 shows the stages from accepting orders to delivering products for the manufacture of very large scale integration (VLSI). These stages can be grouped into two phases:

1 The design phase.
2 The fabrication phase.

In the former, the desired functions and required operating specifications of the circuits are initially decided upon. The chip is then designed from the "top down". That is, the required large functional blocks are first identified. Next, their sub-blocks are selected, and then the logic gates required to

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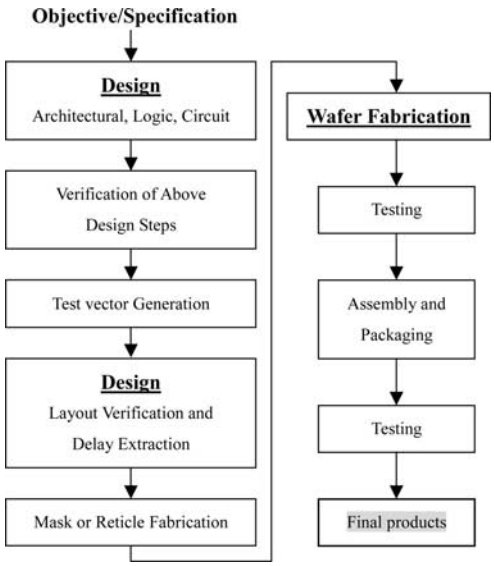

Fig. 1. Stages required for the manufacture of VLSI.

implement the sub-blocks are chosen. Each logic gate is designed by connecting devices that are ultimately used for fabrication on the wafers. Upon completing these various design levels, each is checked to ensure that correct functionality obtains. Then, the layout of the VLSI is recognised. Research and development time (i.e., the design phase) must be reduced for products/processes with a shorter life cycle to increase the market share.

Some physical and chemical technologies are employed in the fabrication of the VLSI. These are used in the oxidation, deposition, implantation, diffusion, evaporation, etc. The chip layout is miniaturised and manufactured on the wafers by sequential photolithography, mask and etching stages [8, 9]. The finished wafers are tested. Conformance chips are assembled, packaged and re-tested. Conforming products are called final products, and are shipped.

The VLSI process includes a design phase and a fabrication phase, each of which can be divided into stages. Each stage may also include several processing steps with similar features. Therefore, the PT of the design phase and each processing stage directly influences the DT of final products. This study offers an efficient hypothetical testing procedure for PCIs, capable of assessing the PT and DT performance of the VLSI. The PCIs of PT and DT are initially defined, and the uniformly minimum variance unbiased (UMVU) estimators of the studied PCIs are derived under the assumption of a normal distribution. The above estimators are then used to construct a the one-to-one relationship between the PCIs and the conformance rate of DT (or the non-conformance rate of PT). Finally, a hypothesis testing procedure for PCIs is established. The hypothesis testing procedure allows manufacturers to assess the PT performance of an individual processing stage for the manufacture of VLSI, and to determine whether the DT performance satisfies customers' requirements, thereby increasing the competitiveness of suppliers. Corresponding tables of non-conformance rate of PT performance and the conformance rate of DT performance are also provided to verify the required performance index value for manufacturers.

The rest of this paper is organised as follows. Section 2 defines and introduces the PT and DT performance indices. Section 3 derives the estimators of PT and DT performance indices. Section 4 constructs the practically applicable hypothesis-testing procedures. Conclusions are drawn in Section 5.

2. The PT and DT Performance Indices

This section defines the PT performance index of each stage for processing VLSI. The DT performance index is then given to assess the DT capability of the final products.

2.1 The PT Performance Index (Q_i)

PT represents the time of processing a stage for VLSI. Each stage of processing VLSI has a corresponding PT, that directly affects manufacturers' DTs. Therefore, efficiently monitoring and improving the process is a valuable exercise for manufacturers. Suppose k stages must be processed in a complete manufacturing process of VLSI to create the final products. Let k stages of processing VLSI have upper time limits, U_1, U_2 ,…, U_k (where $\sum_{i=1}^{k} U_i \leq U_T$, U_T is the upper time limit of DT). Assume that X_1, X_2, …, X_k represent the actual PTs of k stages for processing VLSI (perhaps including assembly, testing stages, and design phase), then $T = \sum_{i=1}^{k} X_i$ is the DT. The unit time may be stated in seconds, minutes, hours, days, or some other unit. Generally, the PT of each stage for processing VLSI varies, such that, X_1, X_2 …, X_k are k normally distributed random variables.

Generally, a shorter PT implies a better performance. Hence, the PT of VLSI exhibits smallest-the-best type quality characteristic. Suppose $(\mu_1,\sigma_1),(\mu_2,\sigma_2),(\mu_k,\sigma_k)$ represent the mean and standard deviation of PT for k stages of processing VLSI, respectively, then the PT performance index of the ith stage can be defined as follows:

$$Q_i = \frac{U_i - \mu_i}{\sigma_i} \tag{1}$$

where $i = 1,2\ldots,k$. The numerator of index Q_i, $(U_i - \mu_i)$, represents the upper time limit U_i of PT of the ith stage, and differs from the actual mean PT, μ_i, which is employed to assess the mean performance of the ith PT. Q_i and thus the performance of the ith PT, increases with $(U_i - \mu_i)$. The denominator of index , Q_i, σ_i, is the standard deviation of the ith PT. A smaller σ_i ndicates a more stable PT at the ith stage and a superior VLSI processing performance, yielding a larger Q_i. Hence, Q_i can reasonably reflect the PT performance for the ith stage of processing VLSI.

In practice $X_i \leq U_i$, is desired, such that the ith PT conforms to the upper specification limit, and the PT of the ith stage is defined as a conformance PT; otherwise, PT is defined as a non-conformance PT (i.e., $X_i > U_i$). The ratio of the non-conformance PT is known as the non-conformance rate. Assuming

a normal distribution, the relationship between the non-conformance rate of the ith PT, P_i, and the index Q_i, can be expressed as follows:

$$\begin{aligned} P_i &= Pr(X_i > U_i) \\ &= 1 - Pr(X_i \leqslant U_i) \\ &= 1 - Pr\left(\frac{X_i-\mu_i}{\sigma_i} \leqslant \frac{U_i-\mu_i}{\sigma_i}\right) \\ &= 1 - \Pr(Z_i \leqslant Q_i) \\ &= 1 - \Phi(Q_i) \end{aligned} \tag{2}$$

where $i = 1,2\ldots,k$, Z_i is a standard normal distribution, and Φ is the cumulative function of the standard normal distribution. Clearly, a larger Q_i corresponds to a smaller non-conformance rate of PT, and is a superior process performance. Consequently, the PT performance index for k stages adequately reflects the non-conformance rate of each processing stage, and a one-to-one mathematical relationship exists between Q_i and non-conformance rate, P_i. Consequently, Table 1 can be used precisely and quickly to estimate the non-conformance rate of PT, P_i using the performance index, Q_i.

For instance, $Q_i = 1$ gives $P_i = 1-\Phi(Q_i) = 1-\Phi(1) = 15.86\%$ from Table 1; $Q_i = 2$ gives $P_i = 2.28\%$, and so on. For the Q_i values which are not listed in Table 1, the non-conformance rate, P_i, can be determined by interpolation, or by checking a standard normal probability distribution table.

P_i can be computed by dividing the non-conformance number of the ith PT by the total sampling number of VLSI. A smaller P_i requires a larger sample size to estimate precisely its value (see [10] for details). Therefore, using the one-to-one relationship between Q_i and P_i, the PT (Q_i) index can be a very convenient and effective tool not only for evaluating the performance of an individual PT, but also for accurately estimating the non-conformance rate, P_i.

Table 2 summarises the actual PT, mean time, standard deviation time, upper limit of PT, index and corresponding non-conformance rate for k processing stages. The table can be employed not only to assess the performance of the ith PT, but also as a reference for enhancing performance.

As the DT performance proposed in the following subsection is poor, the higher non-conformance rates P_i among k processing stages are investigated and improved, reducing the non-conformance PTs to meet the target value of DT. Theoretically, the final products can be delivered on time if the k PTs (X_i) for processing VLSI are all less than the corresponding upper limit U_i. (i.e. $T = \sum_{i=1}^{k} X_i \leqslant \sum_{i=1}^{k} U_i \leqslant U_T$ where U_T represents the upper limit of DT).

Table 1. Q_i = 1.0 (1.0)6.0 *vs.* P_i.

PT performance index Q_i	Non-conformance rate of PT, P_i
1.0	0.158655254
2.0	0.022750132
3.0	0.001349898
4.0	0.000031671
5.0	0.000000287
6.0	0.000000001

Table 2. Actual PT, mean time, standard deviation time, upper limit, index and non-conformance rate for k processing stages

Processing stage rate (P_i)	Actual	Mean PT	Standard	Upper limit	Performance deviation	Non-conformance of PT index
Stage 1	X_1	μ_1	σ_1	U_1	Q_1	$1-\Phi(Q_1)$
Stage 2	X_2	μ_2	σ_2	U_2	Q_2	$1-\Phi(Q_2)$
.	.	.	.	.	.	.
Stage i	X_i	μ_i	σ_i	U_i	Q_i	$1-\Phi(Q_i)$
.	.	.	.	.	.	.
Stage k	X_k	μ_k	σ_k	U_k	Q_k	$1-\Phi(Q_k)$

2.2. The DT Performance Index (Q_T)

The DT $T = \sum_{i=1}^{k} X_i$ is a random variable possessing a normal distribution with mean, $\mu = \sum_{i=1}^{k} \mu_i$ and variance, $\sigma^2 = \sum_{i=1}^{k} \sigma_{i2}$ as X_1, $X_2,\ldots,X_k$ represent the actual PTs for processing k stages of VLSI. A shorter DT corresponds to a superior process performance. That is, DT possesses a so-called smallest-the-best type quality characteristic. For the same reason as mentioned above with respect to the PT performance index, if the upper time limit of DT is U_T (i.e., $T \leqslant U_T$), then the DT performance index, Q_T can be defined as follows:

$$Q_T = \frac{U_T-\mu}{\sigma} \tag{3}$$

Suppose DT does not exceed U_T, then the process is defined as a conformance process. The ratio of the processes conforming to U_T is known as the conformance rate of DT, and can be expressed as

$$P_T = Pr(T \leqslant U_T) = Pr\left(Z \leqslant \frac{U_T-\mu}{\sigma}\right) = \Phi(Q_T) \tag{4}$$

Equation (4) shows that a one-to-one mathematical relationship exists between Q_T and P_T. Table 3 summarises the DT performance index values for VLSI, Q_T, versus corresponding conformance rates, P_T. If P_T is known, Q_T can be obtained from Table 3. The testing procedure described in Section 4

Table 3. Q_T = 1.0 (1.0)6.0 *vs.* P_T.

DT performance index Q_T	*Conformance rate of DT,* P_T
1.0	0.841344746
2.0	0.977249868
3.0	0.998650102
4.0	0.999968329
5.0	0.999999713
6.0	0.999999999

can then be used to check whether a manufacturer's DT performance meets the required target value, Q_T. For values not listed in Table 3, the conformance rate P_T can be obtained by interpolation or can be checked from a standard normal probability distribution table.

A larger Q_T value corresponds to a higher DT conformance rate, P_T. Not only can the DT performance index P_T correctly reflect a manufacturer's ability to deliver on time but it can also evaluate the stability and conformance rate of DT. Therefore, the performance index Q_T is a rational, convenient, and efficient tool for assessing DT performance of VLSI manufacturers.

3. Estimating PT and DT performance indices

This section describes only the estimation of the DT performance index, since the estimated methods and procedures concerning both DT and PT performance indices are the same. Table 4 summarises the estimators.

In practice, the mean μ and standard deviation σ of the true DT are unknown. Therefore, a sample of size n is taken to estimate these values. Let T_i be the actual delivery time of the ith lot of VLSI. $(T_1,T_2,\ldots,T_n)$ then represents a random sample drawn from a normal population with mean μ and standard deviation σ. Suppose the sample mean $\bar{T}=\sum_{n=1}^{n} T_i/n$ and standard deviation $S=\sqrt{\sum_{i=1}^{n}(T_i-\bar{T})^2/(n-1)}$ are used to estimate the population mean μ and standard deviation σ. The intuitive estimator of the DT performance index, Q_T, can be expressed as follows:

$$\tilde{Q}_T = \frac{U_T - \bar{T}}{S} \tag{5}$$

Similarly, the intuitive estimator of the PT performance index (Q_i) for the ith stage can be written as $\tilde{Q}_i=\frac{U_i-\bar{X}_i}{S_i}$, $i=1,2,\ldots,k$, where $\bar{X}_i = \sum_{j=1}^{n} X_{ij}/n$, $S_j^2=\sum_{j=1}^{n}(X_{ij}-\bar{X}_i)^2/(n-1)$.

Assuming a normal population, the expectation of $\tilde{Q}_l$ is

$$E(\tilde{Q}_l)=(A_n^{-1})Q_l \tag{6}$$

(see Appendix A for details), where l = 1, 2,…,k, T, and

$$A_n = \sqrt{\left(\frac{2}{n-1}\right)} \times \left[\frac{\Gamma((n-1)/2)}{\Gamma((n-2)/2)}\right] (n>2)$$

Clearly, A_n is a function of sample size n and is difficult to compute. Consequently,

$$B_n = \sqrt{\left(\frac{n-2}{n-1}\right)\left(1-\frac{1}{4(n-2)}\right)+\left(\frac{1}{32(n-2)^2}\right)} + \left(\frac{5}{128(n-2)^3}\right)(n>2)$$

can be employed to approximate A_n (i.e., $A_n \cong B_n$). As n increases, A_n becomes very close to 1. That is, $\tilde{Q}_l$ is an approximate unbiased estimator of Q_l, implying that, although $\tilde{Q}_l$ is a biased estimator of Q_l, it can easily be modified to be an unbiased estimator of Q_l from Eq. (6) as follows:

$$\hat{Q}_l=A_n\times\tilde{Q}_l \text{ where } l = 1,2,\ldots k,T \tag{7}$$

since $A_n < 1$, and $\hat{Q}_l$ is an unbiased estimator of Q_l. Therefore, $Var(\hat{Q}_l)<Var\hat{(}\tilde{Q}_l)$ and $MSE(\hat{Q}_l)<MSE\hat{(}\tilde{Q}_l)$ can be found, where l = 1, 2,…,k, T. Similarly, for a DT performance index, Q_T, $\hat{Q}_T$ is not only an unbiased estimator of Q_T (i.e., $E(\hat{Q}_T)=Q_T$)), but is also a function of the complete and sufficient statistic $\bar{T},S^2$. Consequently, $\hat{Q}_T$ is the best estimator (i.e., UMVU estimator) of Q_T. For the same reason, $\hat{Q}_l$ is the best estimator of Q_i for the ith stage of processing VLSI. The variance of Q_l can be derived as follows (see Appendix B for details).

$$Var(\hat{Q}_l)=\left(\frac{\Gamma[(n-1)/2]\ \Gamma n-3)/2]}{n\times\Gamma^{-2}\ [(n-2)/2]}\right)(1+nQ_l^2) - Q_l^2 \text{ where } l = 1,2,\ldots k,T \tag{8}$$

Let $t' = \sqrt{\hat{Q}_l/A_n}$. Then, t is a non-central t distribution with n−1 degrees of freedom and a non-central parameter, $\delta=\sqrt{(n)Q_l}$. The probability density function of the best estimator of $\hat{Q}_l$ can be derived as follows (see Appendix C for details).

$$f_{\hat{Q}_l}(x) = \left\{\frac{A_n^{-1}\times\sqrt{n\times 2^{-(n/2)}}}{\Gamma[(n-1)/2]\sqrt{\pi(n-1)}}\right\}\int_0^{\infty} y^{\left(\frac{n-2}{2}\right)} \exp\left\{ -0.5\left[y+\left(\frac{\sqrt{ny}}{(n-1)A_n}x-\delta\right)^2\right]\right\}dy \tag{9}$$

where $x \in R$.

4. Testing Procedure for PT and DT Performance Indices

The point estimators of DT and PT performance indices cannot be used directly to determine whether the DT and PT performances of VLSI meet the manufacturer's requirements, due to sampling error. Thus, a statistical testing procedure is required to assess objectively whether the proposed indices maintain the required values. Assuming that the required DT (or PT) performance index value exceeds or is equal to c, where c is the target value, then the testing procedure for H_0:$Q_l \le c$ (the performance index is incapable) *vs.* H_a:$Q_l < c$ (the performance index is capable) can be determined, where l = 1, 2,…, k, T. Assuming U_l is known, and using $\hat{Q}_l$, the best estimator of Q_l, as the test statistic, then the sample mean $\bar{T} = \sum_{i=1}^{n} T_i/n)$ (or

$\overline{X}_i = \sum_{j=1}^{n} X_{ij}/n)$ and sample standard deviation $S = \left(\sqrt{\sum_{i=1}^{n} (T_i - \overline{T})^2/(n-1)}\right)$ or $S_i^2 = \sum_{j=1}^{n} (X_{ij} - \overline{X}_i)^2/(n-1))$ can be calculated from n sample observations. Hence, the estimated value of $\hat{Q}_l$, q, can be obtained. The *p-value* of the test statistic, $\hat{Q}_l$, can be obtained:

$$p\text{-}value = PR\{\hat{Q}_l > Q | Q_l = C\} = P_R\left\{T' < \frac{\sqrt{N \times Q}}{A_n} | \delta - C\sqrt{N}\right\} \quad (10)$$

t' is a non-central t distribution with $n-1$ degrees of freedom and a non-central parameter, $\delta = c\sqrt{n}$ in Eq. (10). A statistical software package, statistical analysis system (SAS), can be used to calculate the $p\text{-}value = \Pr\{t' > T_0 | \delta = c\sqrt{n}\} = 1 - \Pr\{t' \leqslant T_0 | \delta = c\sqrt{n}\} = 1 - \text{PROBT}(T_0; n-1; \delta = c\sqrt{n})$, where $T_0 = (\sqrt{n} \times q)/A_n$, and $PROBT(T_0; n-1; \delta = c\sqrt{n})$, which is lower cumulated *by* T_0, is the cumulative probability of a non-central t distribution with $n-1$ degrees of freedom and a non-central parameter, $\delta = c\sqrt{n}$ in SAS. The *p-value* can be calculated easily as c, n and q are known.

The proposed testing procedure can be organised as follows [11] to enable manufacturers to assess conveniently whether the DT or PT performance of VLSI meets the targets.

Step 1. Determine the upper limit of DT or PT, U_l, the performance index value c, and the sample size, n.
Step 2. Specify a significance level, α.
Step 3. Take a sample of size n and calculate the sample mean, and the standard deviation. Using B_n to approximate A_n, and calculate the value of the test statistic, $\hat{Q}_l$, denoted by q.
Step 4. Determine the *p-value* using SAS, according to c, q, and sample size, n.
Step 5. Compare the *p-value* with α. The decision rules are

1. If $p\text{-}value \leq \alpha$, conclude that the DT or PT performance index meets the target value (or the performance index is capable).
2. If $p\text{-}value > \alpha$, conclude that the DT or PT performance index does not meet the target value (or the performance index is incapable).

The DT or PT performance for processing VLSI is assessed easily by using the proposed testing procedure. The following example demonstrates the use of the procedure. Suppose the conformance rate, P_T, of DT on time must exceed 97%. Referring to Table 3, a Q_T value of 2.0 is obtained. Thus, in step 1, the DT performance index is set at $c = 2.0$. Assume that a sample of size $n = 20$ is obtained and U_T is known. By specifying the significance level, $\alpha = 0.01$ in step 2, the value, q, of test statistic, $\hat{Q}_T$, can be calculated from the sample data in step 3. In step 4, the *p-value* is obtained using SAS with specified n, c and q. Finally, step 5 compares the *p-value* with 0.01 and draws a conclusion about the hypothesis. If $p\text{-}value > \alpha$, the true DT performance index meets the required level, and the performance of DT is satisfactory. Otherwise, the DT performance is unsatisfactory. Table 4 gives the results of the testing procedure for the performance index, Q_i , of the ith PT, and uses the following notation.

The notation '○' indicates that the PT of the ith stage for processing VLSI does not exceed the upper limit time, U_i, set by the manufacturers, and that the performance meets the requirement at the ith stage. Otherwise, '×' indicates that the PT of the ith stage for processing VLSI, exceeds the upper limit time set by the manufacturers, and the performance does not meet the requirement at the ith stage. In such a case, the manufacturers must assess whether the ith stage delays the DT of VLSI.

5. Conclusion

This study derives the best estimators of PT and DT performance indices for the manufacture of VLSI, and offers a testing procedure for PT and DT PCIs. The proposed testing procedure can be applied easily by an engineer and can effectively clarify the PT performance for an individual manufacturing stage of VLSI. Additionally, the testing procedure can be employed to assess whether the DT schedule can satisfy the customers, thereby increasing the competitiveness of the suppliers. The corresponding tables of the non-conformance rate of PT are also provided for processing VLSI based on the PT performance indices. The conformance rate of DT is based on the supplier's schedule. Hence, for any specified conformance rate,

Table 4. The best estimators of PT and DT performance indices

Processing stage	PT	Sample mean	Sample variance	Best estimator $\tilde{Q}_i$	Non-conformance rate (P_i)	Result note
Stage 1	$X_{11}, X_{12},\ldots, X_{1n}$	$\overline{X}_1$	S_1^2	$\hat{Q}_1 = A_n \times \tilde{Q}_1$	$1 - \Phi(\hat{Q}_1)$	○
Stage 2	$X_{21}, X_{22},\ldots, X_{2n}$	$\overline{X}_2$	S_2^2	$\hat{Q}_2 = A_n \times \tilde{Q}_2$	$1 - \Phi(\hat{Q}_2)$	×
.	.	.	.	.	.	.
Stage i	$X_{i1}, X_{i2},\ldots, X_{in}$	$\overline{X}_i$	S_i^2	$\hat{Q}_i = A_n \times \tilde{Q}_i$	$1 - \Phi(\hat{Q}_i)$	×
.	.	.	.	.	.	.
Stage k	$X_{k1}, X_{k2},\ldots, X_{kn}$	$\overline{X}_k$	S_k^2	$\hat{Q}_k = A_n \times \tilde{Q}_k$	$1 - \Phi(\hat{Q}_k)$	JI
DT	$T_1, T_2,\ldots, T_n$	$\overline{T}$	S^2	$\hat{Q}_T = A_n \times \tilde{Q}_T$	$P_T = \Phi(\hat{Q}_T)$	(Conformance rate)

P_T, or non-conformance rate, P_i, a corresponding performance index value, Q_T or Q_i, can be obtained. The proposed testing procedure can also be expressed in terms of the conformance rate.

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References

1. G. W. Dickson, "An analysis of vendor selection systems and decisions", Journal of Purchasing, 2(1), pp. 5–17, 1996.
2. C. A. Weber, J. R. Current and W. C. Benton, "Vender selection criteria and methods", European Journal of Operational Research, 50, pp. 2–18, 1991.
3. V. E. Kane, "Process capability indices", Journal Quality Technology, 18, pp. 41–52, 1986.
4. L. K. Chan, S. W. Chang and F. A. Spiring, "A new measure of process capability: C_{pm}", Journal of Quality Technology, 20(3), pp. 162–175, July 1988.
5. R. A. Boyles, "The Taguchi capability index", Journal of Quality Technology, 23, pp. 17–26, 1991.
6. W. L. Pearn, S. Kotz and N. L. Johnson, "Distributional and inferential properties of process capability indices", Journal of Quality Technology, 24, pp. 216–231, 1992.
7. K. Vännman, "A unified approach to capability indices", Statistica. Sinica, 5, pp. 805–820, 1995.
8. S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, Process Technology, 2000.
9. C. Mead and L. Conway, Introduction to VLSI Systems, Addison–Wesley, Reading, MA, 1980.
10. D. C. Montgomery, Introduction to Statistical Quality Control, John Wiley, New York, 1985.
11. S. W. Cheng, "Practical implementation of the process capability indices", Quality Engineering, 7(2), pp. 239–259, 1994.

Appendix A

$$\tilde{Q}_T=\frac{U_T-\overline{T}}{S}=\sqrt{\left(\frac{n-1}{n}\right)}\times Z\times C^{\frac{-1}{2}}$$

where $Z=\sqrt{n}(U_T-\overline{T})/\sigma\sim N(\sqrt{n}Q_T,1)$, $C=(n-1)S^2/\sigma^2\sim\chi^2_{n-1}$

Because $\overline{T}$ and S^2 are mutually independent, so Z and C are also independent under the assumption of normal distribution, hence,

$$E[\tilde{Q}_T]=\sqrt{\left(\frac{n-1}{n}\right)}\times E[Z]\times E[C^{(-1/2)}]=\sqrt{\left(\frac{n-1}{n}\right)}\times(\sqrt{n}\,Q_T)\times\left(\frac{\Gamma[(n-2)/2]}{\sqrt{2}\Gamma[n-1)/2]}\right)=(A_n^{-1})Q_T$$

Similarly,

$$E[\tilde{Q}_i]=(A_n^{-1})Q_i$$

Therefore,

$$E[\tilde{Q}_l]=(A_n^{-1})Q_i,l=1,2,\ldots k,T$$

where

$$A_n=\sqrt{\left(\frac{2}{n-1}\right)}\times\left[\frac{\Gamma((n-1)/2)}{\Gamma((n-2)/2)}\right]\quad\left(n<2\right).$$

Appendix B

Before deriving the variance of $\tilde{Q}_T$, the second moment of $\hat{Q}_T$ is derived first, as follows. Because,

$$\tilde{Q}_T=A_n\times\tilde{Q}_T=A_n\times\sqrt{\left(\frac{n-1}{n}\right)}\times Z\times C^{\frac{-1}{2}}$$

hence,

$$E[\hat{Q}_T^2]=A_n^2\times E[Z^2]\times E[C^{-1}]\times\left(\frac{n-1}{n}\right)=\frac{2}{n-1}\times\left(\frac{\Gamma[(n-1)/2)]}{\Gamma[(n-2)/2)]}\right)^2\times[1+nQ^2]\times\frac{\Gamma[(n-3)/2)]}{\Gamma[(n-1)/2)]}\times\frac{n-1}{n}=\frac{\Gamma[(n-1)/2]\Gamma[(n-3)/2]}{n\Gamma^2[(n-2)/2]}\times(1+nQ_T^2)$$

Therefore,

$$Var\,(\hat{Q}_T)=\left(\frac{\Gamma[(n-1)/2]\Gamma[(n-3)/2]}{n\times\Gamma^2[(n-2)/2]}\right)(1+nQ_T^2)Q_T^2$$

Similarly,

$$Var\,(\hat{Q}_l)=\left(\frac{\Gamma[(n-1)/2]\Gamma[(n-3)/2]}{n\times\Gamma^2[(n-2)/2]}\right)(1+nQ_l^2)Q_l^2$$

where $l = 1, 2,\ldots,k, T$.

Appendix C

$$\hat{Q}_T=A_n\tilde{Q}_T=A_n\sqrt{\left(\frac{n-1}{n}\right)}\times Z\times C^{(-1/2)}=\frac{A_n}{\sqrt{n}}\times T$$

where, $T=\dfrac{Z}{\sqrt{C/(n-1)}}\sim t_{n-1}(\delta=\sqrt{n}Q_T)$. Let $X=\tilde{Q}_T=\dfrac{A_n}{\sqrt{n}}\times T$

and there is one-to-one mathematical relationship between X and T, hence,

$$f_{\tilde{Q}_T}(x)=f_T(t)\left|\frac{dT}{dX}\right|=f_T\left(\frac{\sqrt{n}}{A_n}x\right)\times\frac{\sqrt{n}}{A_n}=f_{\tilde{Q}_i}(x)$$

$$=\left\{\frac{A_n^{-1}\times\sqrt{n}\times 2^{-(n/2)}}{\Gamma[(n\text{-}1)/2]\sqrt{\pi(n\text{-}1)}}\right\}\int_0^\infty y^{\left(\frac{n-2}{2}\right)}exp\left\{-0.5\left[y+\left(\frac{\sqrt{n}y}{(n-1(A_n}x-\delta\right)^2\right]\right\}dy$$

where $x\in R$.