



Characterization of the low temperature dopant activation behavior at NiSi/silicon interface formed by implant into silicide method

Kow-Ming Chang^{*}, Jian-Hong Lin, Cheng-Yen Sun

Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, 1001 Ta Hsueh Road, Hsinchu 30050, Taiwan, ROC

ARTICLE INFO

Article history:

Available online 18 March 2008

PACS:

61.72.Tt

81.20.-n

Keywords:

Nickel silicide

Implant into silicide

Solid phase epitaxial regrowth

Rapid thermal anneal

ABSTRACT

Process temperature and thermal budget control are very important for high-*k* dielectric device manufacturing. This work focuses on the characteristics of low temperature activated nickel silicide/silicon (M/S) interface formed by implant into silicide (IIS) method. By combining SIMS, *C*-*V*, *I*-*V*, and AFM measurements in this work, it provides a clear picture that the high dopant activation ratio can be achieved at low temperature (below 600 °C) by IIS method. From SIMS and *C*-*V* measurements, high dopant activation behavior is exhibited, and from *I*-*V* measurement, the ohmic contact behavior at the M/S junction is showed. AFM inspection displays that under 2nd RTA 700 °C 30 s no agglomeration occurs. These results suggest that IIS method has the potential to integrate with high-*k* dielectric due to its low process temperature. It gives an alternate for future device integration.

© 2008 Elsevier B.V. All rights reserved.

1. Introduction

Both shallow junction and high-*k* dielectric formation are important issues for manufacture of CMOS devices beyond the 45 nm generation [1]. For ohmic contact consideration, traditional junction formation technology requires high-temperature annealing (i.e. RTA 1000 °C 30 s), but this high-temperature process will affect not only the original dopant concentration profile but also make some high-*k* dielectric crystallized [2,3]. For device integration consideration, low temperature activation technique provides an alternative possibility to give solutions to these two difficulties.

Solid phase epitaxial regrowth (SPER) [4,5] is the main idea to achieve the low temperature activation. However, preamorphized layer, especially for implantation formed amorphous layer, still needs well thickness control to achieve the goal of the shallow junction formation. On the other hand, IIS method [6] can take the advantages of both SPER (a thin amorphous Si layer will be formed at the silicide/silicon interface during silicidation process) and fine junction depth control (determined by silicide thickness). In addition, dopant segregation [7] phenomenon can pile up the dopant concentration at the silicide/silicon (M/S) interface, and thus has a potential to form a better ohmic contact. SIMS has frequently been adapted to show the dopant segregation phenomena at the silicide/silicon interface and the spreading resistance profiling (SRP) method has been used to analysis the dopant concentration at

the bulk activated region [4,5,8]. However, few literatures have discussed the dopant activation behavior at the silicide/silicon interface. In this work, we use the metal/semiconductor (MS) diode structure combined with *I*-*V* (current-voltage), *C*-*V* (capacitance-voltage), and SIMS measurements to explore the high activation ability at the silicide/silicon interface made by the IIS method.

2. Device fabrication

Stating material is (100) n-type (1–10 Ω cm, phosphorous doped) and (100) p-type (1–10 Ω cm, boron doped) wafer. A 200 nm thick silicon dioxide was thermally grown for isolation. Nickel silicide was formed by two-step rapid thermal annealing (RTA) process. A 20 nm thick nickel film was deposited by sputter system. All samples were under first step RTA at the condition 400 °C 30 s. After removing the unreacted Ni, p-type substrate samples were implanted with BF₂ (1 × 10¹³ cm⁻², 20 keV) and n-type substrate samples were implanted with arsenic (1 × 10¹³ cm⁻², 10 keV). Before thermal coated Al as the back contact, samples were treated with 2nd RTA step 30 s at different temperatures from 400 to 650 °C, 50 °C per step (400, 450, 500, 550, 600, and 650 °C).

3. Results and discussions

3.1. SIMS measurement

SIMS profile of the BF₂ doped sample with 2nd RTA 400 °C 30 s is shown in Fig. 1, and it provides two messages. First, the peak boron concentration is appeared inside the nickel silicide film

^{*} Corresponding author. Tel.: +886 3 5712121x54205; fax: +886 3 5724361.
E-mail address: kmchang@faculty.nctu.edu.tw (K.-M. Chang).

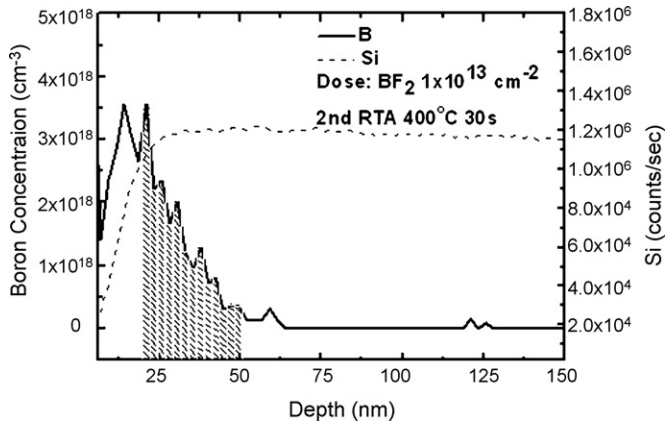


Fig. 1. SIMS profile of the BF₂ doped p-type substrate, with 2nd RTA 400 °C 30 s. The dopant segregation phenomenon can be found at about 23 nm from surface. The shadow area from 23 nm to about 50 nm is about $5 \times 10^{12} \text{ cm}^{-2}$, which is defined as dopant implanted in Fig. 3.

suggesting that the projected range at this study is in the silicide, which implies the implantation damage in the silicon is depressed. And secondly, dopant segregation phenomenon can be found at the silicide/silicon interface even at the short period with low temperature annealing (2nd RTA 400 °C 30 s). The silicide thickness from SIMS measurement is about 23 nm, and this value is confirmed by the SEM inspection.

3.2. C–V measurement

At this study, we adapted the capacitance–voltage measurement [9] to analysis the silicide/silicon interface. With depletion approximation, depletion width (W) in the silicon is estimated by

$$W = \frac{K_s \epsilon_0 A}{C} \quad (3.1)$$

where K_s is dielectric constant of silicon and A is the MS diode’s contact area. And the effective doping density at depth W is given by

$$N_A(W) = \frac{2}{qK_s \epsilon_0 A^2 d(1/C^2)/dV} \quad (3.2)$$

Averaged boron doping density within the depletion region extracted from C–V measurement is illustrated in Fig. 2. It shows that with higher 2nd RTA temperature, higher doping density is obtained. From C–V measurement results, two observations can be

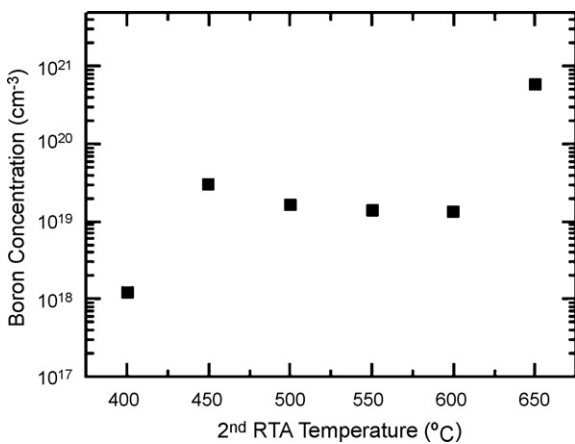


Fig. 2. Boron concentrations at different 2nd RTA temperatures extracted by C–V method.

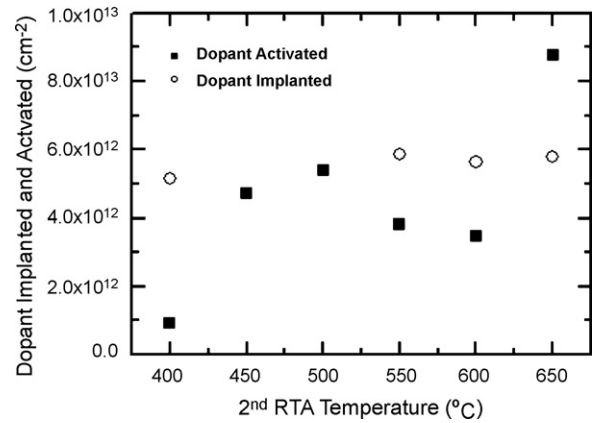


Fig. 3. Dopant (cm^{-2}) as the integral of the concentration over depths from C–V and SIMS profile (dopant activated and dopant implanted) versus different 2nd RTA temperatures.

found. First, even at the lowest activation temperature (400 °C), the effective doping density (N_{eff}) is higher than 10^{18} cm^{-3} , this convinces that IIS is an effective method to achieve low temperature activation. And secondly, at higher temperature annealing, N_{eff} becomes higher than 10^{19} cm^{-3} . Silicon begins to become the degenerate substance at this high doping level, and this property is good for silicide/silicon interface to form an ohmic contact. Furthermore, we compared the integral of the dopant concentration over depths from SIMS and C–V measurement results (n_{CV} and n_{SIMS}) in Fig. 3. It shows that the activation percentage ($n_{\text{CV}}/n_{\text{SIMS}}$) is very high. Over 50% dopant was activated over 2nd RTA 450 °C. The summation process was taken from $V_r = 0$ to 0.2 V and dopant within the depletion region at $V = 0$ was not summed in the C–V measured data. Samples with high N_{eff} might not be fully depleted in this voltage range; as a result, underestimated n_{CV} might occur in these high N_{eff} samples. There exist an abnormal activation calculation occurred at 2nd RTA 650 °C sample. This may be due to the incorrect high doping density obtained from Eqs. (3.1) and (3.2) that using Maxwell–Boltzmann distribution. The Maxwell–Boltzmann distribution will over-estimate the N_{eff} when the material becomes degenerate [10] and as the consequence, the activated dopant obtained using N_{eff} will also be over-estimate. At this study, we only use the Maxwell–Boltzmann distribution to estimate the doping density. Although it may not good enough to extract the real concentration of the sample, it does reflect the high activation ability at the silicide/silicon interface, and shows that near the M/S interface, silicon is undoubtedly turning into the degenerate material.

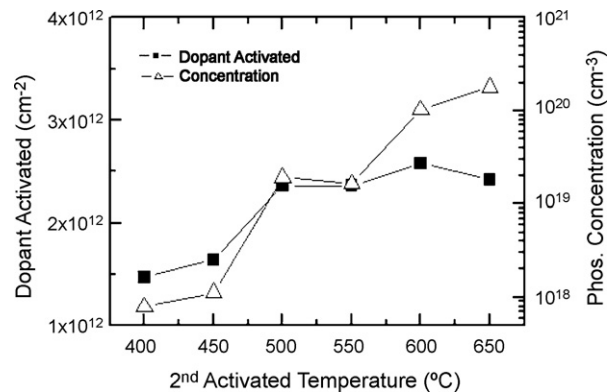


Fig. 4. Phosphorous concentration (cm^{-3}) calculated from C–V measurement, and activated dopant (cm^{-2}) as the integral of the concentration over depths from C–V measurement at different 2nd RTA temperatures.

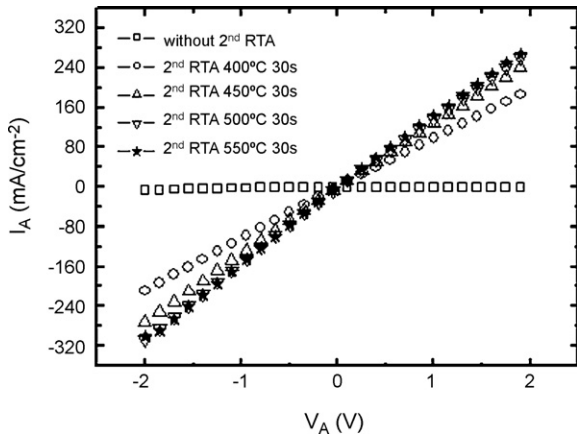


Fig. 5. *I*–*V* characteristics of boron doped samples. All samples with 2nd RTA behave more likely to ohmic contacts than Schottky contacts.

Similarly, phosphorous doped samples exhibit the high activation ability. It can be found in Fig. 4 that with above 500 °C 2nd RTA, phosphorous doped samples also achieve high effective doping densities more than $1 \times 10^{19} \text{ cm}^{-3}$, which make the silicon at the M/S interface to become ohmic contact.

3.3. *I*–*V* measurement

For direct determine if the M/S junction is ohmic contact or not, *I*–*V* measurement can be a good reference. The corresponding *I*–*V* characteristics of boron doped samples are illustrated in Fig. 5 all

samples with 2nd RTA have linear *I*–*V* characteristics instead of Schottky diodes regulation characteristics, which means that all samples behave more likely to be ohmic contacts than Schottky contacts. In addition, the slopes of the *I*–*V* curves are increasing when raising the 2nd RTA temperature from 400 to 550 °C. Since the silicide after 2nd RTA temperatures at the range between 400 and 650 °C is at the nickel mono silicide phase [11], the sheet resistance is the same at these temperatures. The different characteristics of *I*–*V* curves with different 2nd RTA temperatures should be contributed to the differences in contact resistance. This indicates that the contact resistance is decreasing with increasing 2nd RTA temperature. This is in good agreement to *C*–*V* measurement result that more boron is activated at higher 2nd RTA temperature and higher 2nd RTA temperature can form better ohmic contact. Phosphorous doped samples have similar *I*–*V* behaviors. Both BF₂ doped p-type substrate and P doped n-type substrate show ohmic contact behavior at low temperature activation with nickel silicide as the contact metal using IIS method.

3.4. AFM inspection

Morphology inspection is required to further to clarify that previous *C*–*V* and *I*–*V* measurement results are not biased by silicide deformation. Samples (n-type substrate, phosphorous doped) without 2nd RTA and with 2nd RTA 30 s at different temperatures (400, 500, 600, and 700 °C) are prepared. Fig. 6 shows the AFM inspection results for these samples (area: 10 μm × 10 μm), and all RMS values are around 1 nm. No agglomerations are discovered in these samples even at RTA 700 °C 30 s, which are similar to other groups' results [11,12]. Since fluorine can retard nickel silicide film's

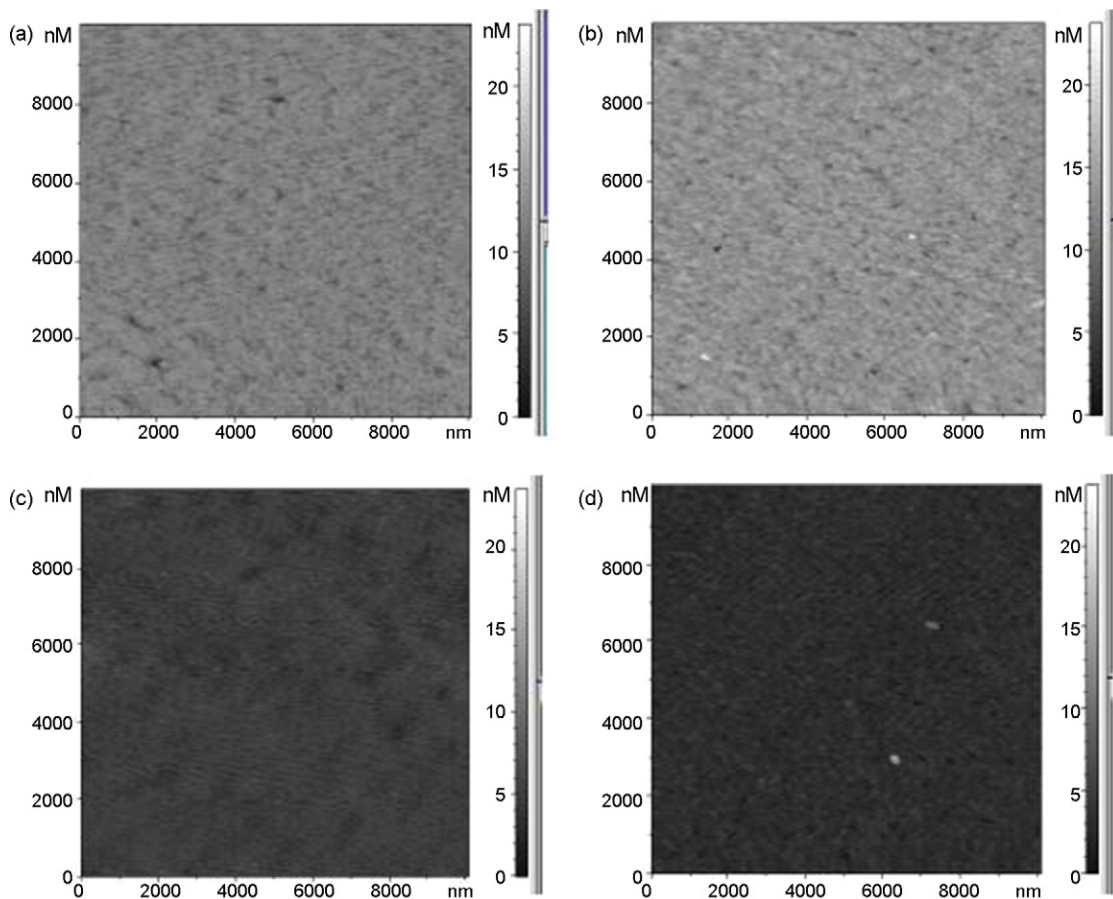


Fig. 6. AFM images show NiSi surface morphology with 30 s 2nd RTA at (a) 400 °C, (b) 500 °C, (c) 600 °C and (d) 700 °C.

agglomeration [13], it is believed that BF_2 doped samples can also sustain RTA 700 °C 30 s without agglomeration occur. Since the experiments from 3.1 to 3.3 are taken under 700 °C, it is believed that these results are not biased by silicide agglomeration effect.

4. Conclusion

From SIMS measurement, it exhibits that there are high dopant dosages pill up at the M/S interface by dopant segregation phenomenon even under low thermal budget 2nd RTA control. This can limit the implantation damage mainly occurred in the silicide layer and provide a better M/S interface. $C-V$ measurement shows that with higher 2nd RTA temperatures at the range 400–650 °C, higher activation can be achieved at the M/S interface for both boron and phosphorous doped samples. Ohmic contact property can be found in $I-V$ measurements, with higher 2nd RTA temperatures between 400 and 550 °C, lower contact resistances are present. AFM inspections show that no agglomeration of silicide film is occurred under 700 °C 30 s. From these results, 2nd RTA 500 to 600 °C 30 s may be a good process window for IIS method to future integration with high- k dielectric device.

References

- [1] ITRS Roadmap 2006 update.
- [2] G.D. Wilk, R.M. Wallace, J.M. Anthony, *J. Appl. Phys.* 89 (2001) 5243.
- [3] C.S. Kang, H.J. Cho, R. Choi, Y.H. Kim, C.Y. Kang, S.J. Rhee, C. Choi, M.S. Akbar, J.C. Lee, *Electron Dev., IEEE Trans.* 51 (February (2)) (2004) 220.
- [4] B.J. Pawlak, R. Lindsay, R. Surdeanu, P.A. Stolk, K. Maex, in: *Proceedings of the 14th International Conference on Ion Implantation Technology, 2002*, p. X.
- [5] M.J.P. Hopstakena, Y. Tamminga, M.A. Verheijen, R. Duffy, V.C. Venezia, A. Heringa, *Appl. Surf. Sci.* 231–232 (2004) 688.
- [6] D.L. Kwong, T.H. Ku, S.K. Lee, E. Louis, N.S. Alvi, P. Chou, *J. Appl. Phys.* 61 (1987) 5084.
- [7] J. Kedzierski, D. Boyd, C. Cabral Jr., P. Ronsheim, S. Zafar, P.M. Kozlowski, J.A. Ott, M. Jeong, *Electron Dev., IEEE Trans.* 52 (January (1)) (2005) 220.
- [8] R. Lindsay, K. Henson, W. Vandervorst, K. Maex, B.J. Pawlak, R. Duffy, R. Surdeanu, P. Stolk, J.A. Kittl, S. Giangrandi, X. Pages, K. van der Jeugd, *J. Vac. Sci. Technol. B* 22 (January/February (1)) (2004) 306.
- [9] Dieter K. Schroder, *Semiconductor material and device characterization*, second edition, John Wiley & Sons, Inc., 1998 (chapter 2).
- [10] J.S. Blakemore, *Solid-State Electron.* 25 (1982) 1067.
- [11] Lauwer Anne, Jorge A. Kittl, Mark J.H. Van Dal, Oxana Chamirian, Malgorzata A. Pawlak, Muriel de Potter, Richard Lindsay, Toon Raymakers, Xavier Pages, Bencherki Mebarki, Tushar Mandrekar, Karen Maex, *Mater. Sci. Eng. B* 114–115 (2004) 29.
- [12] Chao-Chun Wang, Mao-Chieh Chen, *Jpn. J. Appl. Phys.* 45 (2006) 1582.
- [13] A.S. Wong, D.Z. Chi, M. Loomans, D. Ma, M.Y. Lai, W.C. Tjiu, S.T. Chua, C.W. Lim, J.E. Greene, *Appl. Phys. Lett.* 81 (2002) 5138.