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Characterization of the low temperature activated N^+/P junction formed by implant into silicide method

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ABSTRACT

Shallow junction formation and low thermal budget control are important for advanced device manufacturing. Implant into silicide (IIS) method is a candidate to achieve both requirements. In this work we show that the high activation ability of the implant into nickel silicide method at low activated temperature is strongly related to the solid phase epitaxial regrowth (SPER) process. The SIMS, capacitance–voltage (*C–V*), four points probe (FPP), and current–voltage (*I–V*) measurements are combined to demonstrate that the SPER process of the IIS method is starting from the silicide/silicon (M/S) interface. The best N^+/P interface is formed when SPER is complete. After SPER process finished, additional thermal budget may cause junction performance degradation at the temperature higher than 550 °C.

1. Introduction

For future MOS device fabrication, shallow junction is a necessary requirement. The shallow junction formed by the implant into silicide (IIS) method has been discussed in many researchers using SIMS, current–voltage (*I–V*) methods [1,2], and most results show that the junction formed by IIS method is suitable for nano-scaled devices manufacturing. However, few literatures have mentioned the inner process of the junction formation about the IIS method. There are two possibilities may explain why IIS method can provide high activation ability at low activation temperature. First, the silicidation process (first RTA) will create a thin amorphous silicon layer below silicide/silicon due to the process-induced stress [3]. This thin layer may just play the role which like the implanted induced amorphous layer in the traditional solid phase epitaxial regrowth (SPER) [4,5] process. An important concept of the SPER process is that dopant activated in amorphous silicon can be activated at a quantity higher than their thermal solubility in crystal silicon at same activation temperature [6]. This factor may provide a good explaining about the high activation ability of SPER method and so as IIS method. And secondly, nickel silicide can reduce the energy required for amorphous silicon to regrowth to crystal silicon [7], this phenomenon is what the so-called metal-induced crystallization [8], which is famous in TFT industry. The second factor provides lower temperature requirement to active dopant than traditional SPER process. In this work, we follow these two assumptions and combine the SIMS, *I–V*, *C–V*, and four points probe measurements to study the junction formation behavior of the IIS method.

2. Device fabrication

Thirty-nanometer silicon dioxide was thermally grown on (1 0 0) p-type silicon wafer as the isolation oxide, after defining the active region, a 20-nm nickel film was then deposited by E-gun evaporation system. All samples were treated with first RTA 350 °C 30 s, after un-reacted Ni was removed, all samples were ion implanted with phosphorous (doping density: $5 \times 10^{15}\,cm^{-2}$), followed different second RTA temperature treatments 60 s from 400 °C to 650 °C, 50 °C per step. At the final step, Al was thermally coated as back contact. No post-metal annealing was treated for thermal budget control consideration.

3. Results and discussions

3.1. C–V measurement

The effective phosphorous concentration (N_{eff}) estimated from *C–V* measurement [9] is demonstrated in Fig. 1. The measured capacitance is composed by of three different capacitances in

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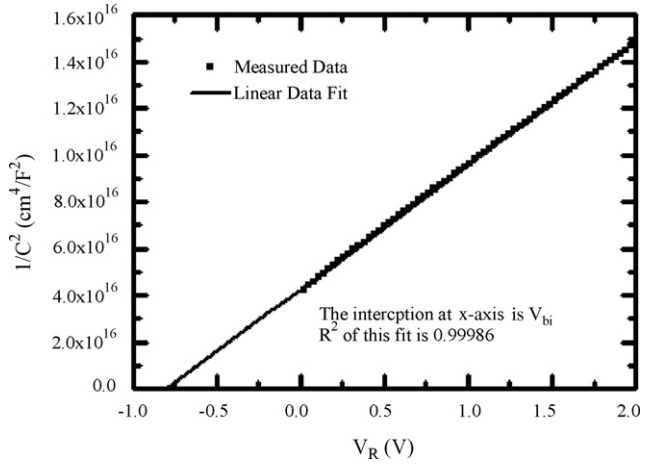

Fig. 1. An example of the measured $1/C^2$–V curve, the sample was treated with second RTA 650 °C 60 s.

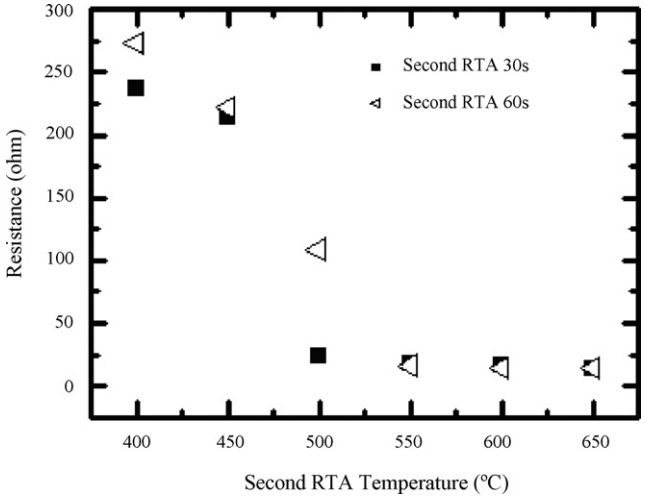

Fig. 3. Resistance measured by four points probe method.

series, silicide/silicon (M/S) junction capacitance, N^+/P junction capacitance, and back contact capacitance. Based on the results in Ref. [10], it shows that there present high dopant activation level at the M/S interface formed by IIS method, either it will become an ohmic contact or exits a relative large capacitance compared to the N^+/P junction capacitance where the lightly doped substrate dominate the small capacitance value. The M/S capacitance term could be neglect with little influence in the analysis. On the other hand, the area of the back contact is about the full wafer size, which is several orders of magnitude larger than the area of N^+/P junction, so the capacitance at the back contact can also not take into consideration. As the result, the measured capacitance was mainly contributed due to p-subdepletion junction at the N^+/P junction. From analyzing the C–V data, the p-subdoping density can be obtained from the differential capacitance–voltage profiling technique [9]. Fig. 1 shows the relationship between the depletion capacitance and the applied reverse voltage, the building voltage of the N^+/P junction can be obtained from the projection of the $1/C^2$–V curve to where $1/C^2 = 0$. The high linearity of the $1/C^2$–V curve implies that the abruptness of the N^+/P junction is good and using abrupt junction formula to express the experimental results is suitable. The N_{eff} is then calculated from the averaged substrate doping density and the building voltage. The relation of N_{eff} to the second RTA temperature is shown in Fig. 2, it seems that the N_{eff} presents at the N^+/P interface is negatively related to the second RTA temperature. The lowest N_{eff} extracted at this study is above 10^{19} cm^{-3}, which is four order larger than the substrate doping density. This supports the assumption that the capacitance measured is mainly due to the depletion in substrate at the N^+/P junction.

3.2. FPP and SIMS measurements

Some papers appointed that defects might cause dopant deactivated [11,12] at higher RTA temperature. However, from the study about the M/S junction [10], we did not find significant deactivation to take place at the silicide/silicon interface at the same process window in this study. In order to make sure the origin of the decreased N_{eff}, a test structure designed for FPP measurement is used. By removing NiSi using silicide etch solution (the etch selectivity of NiSi to bare Si is larger than 50), the results of measured resistance are displayed in Fig. 3. It shows that the resistances become smaller with higher second RTA temperatures, which means that either doping concentration or the junction depth is extended at higher second RTA temperature. With the assistance of SIMS profile in Fig. 4, suggesting that the lower N_{eff}

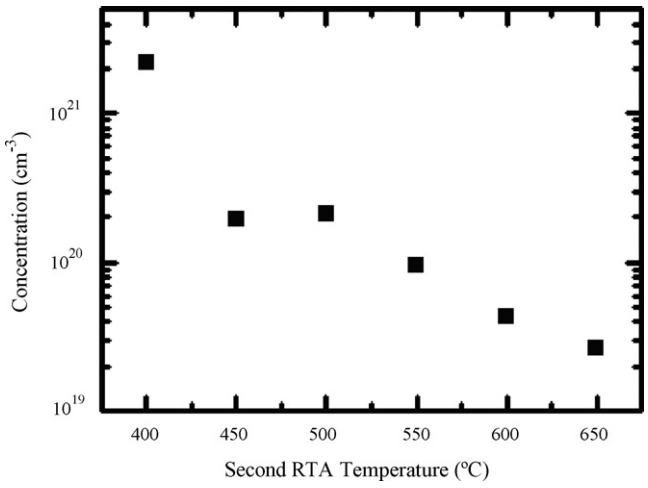

Fig. 2. Phosphorous doping density estimated from C–V measurement with different second RTA temperatures.

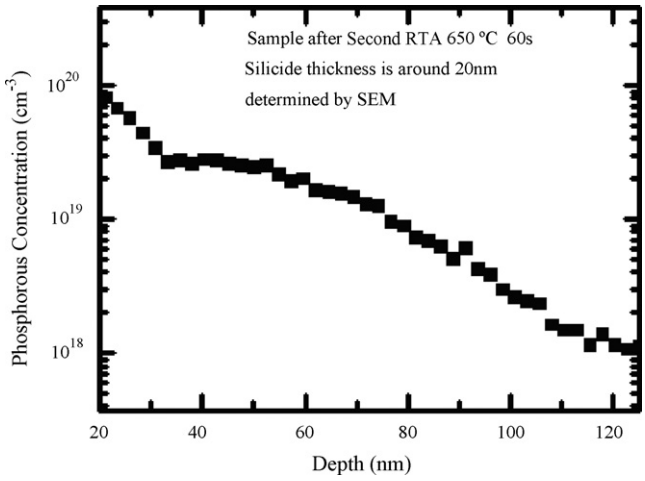

Fig. 4. SIMS profile of phosphorous-doped sample treated with second RTA 650 °C 60 s.

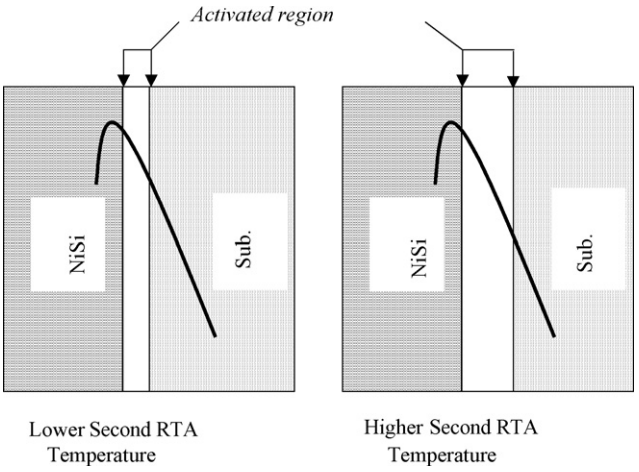

Fig. 5. The behavior of phosphorous activation is shown schematically. The P/N junction interface becomes deeper away from M/S interface with higher second RTA temperature.

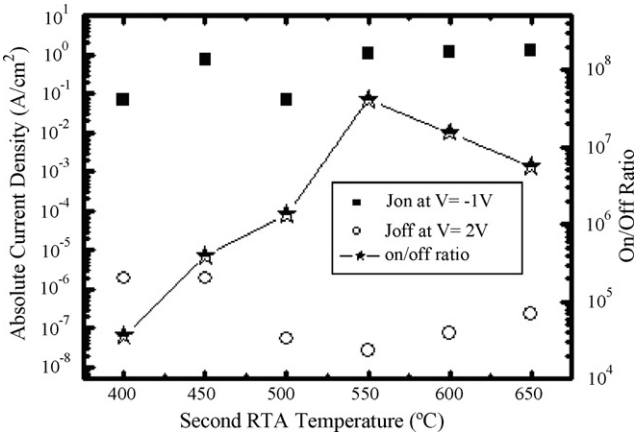

Fig. 6. Absolute J_{on}, J_{off}, current density and on/off ratio measured at different second RTA temperatures.

measured at higher temperature is mainly due to that where the N^+/P interface presented are at the deeper position away from the M/S interface. The result implies that the dopant activation behavior is starting from the NiSi/Si interface extended to the silicon substrate. If the high activated doping concentration is related to the SRER process as we assumed, it is recommended that the SPER process is starting from the M/S interface. As a consequence of *C–V*, FPP, and SIMS measurements, the suggested phosphorous activation behavior of the IIS method is illustrated in Fig. 5.

3.3. *I–V* measurement

In addition to analyze the junction forming behavior, *I–V* measurement are adapted. The N^+/P diode *I–V* measurement results are summarized as J_{on} (at $V_A = -1$ V) and J_{off} (at $V_A = 2$ V) exhibited in Fig. 6. The sample with second RTA 550 °C 60 s treatment has the lowest J_{off} value among all samples. The high J_{off} current densities presented at second RTA temperature below 500 °C are explained as that there may exist high defect densities at the P/N junction interface. The defects may originate from the remained amorphous region where is still not recrystallized due to the short activation time or the low activation temperature. As the result, with increasing second RTA temperatures, the SPER process continuous going, and the J_{off} currents decreased. At second RTA 550 °C 60 s, the SPER process seen to be completed (this can be observed by the relative consistent resistances measured in FPP method, see Fig. 3), the sample exhibits the maximum on/off ratio. However, the on/off ratios (Fig. 5) and N_{eff} (Fig. 2) diminish at second RTA higher than 550 °C 60 s. Since the SPER process looks like completed above second RTA 550 °C 60 s, the facts described above may originated by defect (dislocations start to form at the temperature range from 500 °C to 600 °C [13]) itself or by some defect-induced dopant deactivation at the P^+/N interface. In addition, deactivation from phosphorous super-saturated solubility to thermal equilibrium solubility in silicon [14] might also play an important role when the thermal budget is higher than which required for SPER process completion. (The experiments of thermal stability about dopant super-saturated will be given in future publication.)

4. Conclusion

With the starting idea that SPER is the main response to the high activation ability with IIS method in low activation temperature, we combine the SIMS, *C–V*, FPP, and *I–V* measurements to construct the doping activation behavior of the IIS method. All experiment results suggested that SPER process is starting from the M/S interface and extend into the silicon substrate. The best N^+/P interface is formed when SPER process is complete. After SPER process finished, samples with additional thermal budget treatment above 550 °C cause the defect formation at the bulk silicon and the dopant deactivation phenomenon may occur, both factors will decay the N^+/P junction's performance. Sample treated with second RTA 550 °C 60 s forms the best N^+/P junction among all controls in this study.

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