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Nitrogen Implantation and *In Situ* HF Vapor Clean for Deep Submicrometer n-MOSFETs

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This work describes a high performance and reliable deep submicrometer n-channel metal oxide semiconductor field effect transistor (n-MOSFET) with ultrathin gate oxide prepared by combining nitrogen gate electrode implantation and native-oxide-free *in situ* HF vapor preoxidation cleaning. The results herein reveal that the performance and reliability, including the leakage current of the ultrathin gate oxide, charge-to-breakdown, drain current, transconductance, charge pumping current, stress induced leakage current, and hot carrier reliability of n-MOSFETs are all significantly improved. The enhanced reliability and performance are attributed to the native-oxide-free process, smooth interface, and reduced incorporation of As in the gate oxide which results from HF vapor cleaning and nitrogen implantation.
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The reliability challenges of ultrathin gate oxide are becoming increasingly greater for deep submicrometer complementary metal oxide semiconductors (CMOS) devices.[1,2] As the gate oxide thickness scales down, causing soft breakdown and direct tunneling effects, removal of the native oxide prior to gate oxidation becomes critical. Hence, the HF vapor clean and *in situ* native oxide desorption process have been investigated extensive.[3,4] The postoxidation anneal (POA) and/or oxynitridation process may enhance the trapping and hot carrier immunity properties of gate oxides by improving interface smoothness and/or increasing interfacial nitrogen concentration.[5,6] Nitrogen implantation has recently received increasing attention in the fabrication of deep submicrometer devices.[7] Nitrogen was implanted (*i*) into poly-Si gates to suppress boron penetration,[8-11] (*ii*) into junctions to improve the junction leakage,[12,13] and (*iii*) into substrates to enhance n-channel metal oxide semiconductor field effect transistor (n-MOSFET) device performance.[12-15] The hot carrier resistance of both n- and p-MOSFETs was also found to be capable of substantial improvement by incorporating nitrogen in the gate oxide by implanting it through a polysilicon gate.[11]

This work describes a high performance and reliable deep submicrometer n-MOSFET with ultrathin gate oxide prepared by combining nitrogen gate electrode implantation and native-oxide-free *in situ* HF vapor preoxidation cleaning. Additional *in situ* HF vapor cleaning and the transfer of wafers in the closed ambient can reduce the regrowth of native oxide and improve surface roughness. Furthermore, the device will benefit from low arsenic incorporation at the oxide/silicon interface in the nitrogen implantation samples. Consequently, the performance and reliability is significantly improved, including the leakage current of ultrathin gate oxide, charge-to-breakdown (Q_{bd}), the drain current (I_d), transconductance (G_m), charge pumping current (I_{cp}), stress induced leakage current (SILC), and hot carrier reliability of n-MOSFETs with 4 nm thin gate oxides.

Experimental

The gate oxidations and polysilicon deposition were performed in the Advance 400 (ASM A400/3), a clustered system with three vertical furnaces. This clustered system was designed for continuous processes in a high purity nitrogen ambient such as *in situ* HF vapor cleaning, gate oxidation, and polysilicon deposition. Wafers are processed sequentially through these three modules, without exposure to air, thus obtaining native-oxide-free poly-Si/SiO_2/Si MOS capacitors.[16] The effects of *in situ* HF vapor cleaning and N_2^+ implantation on n-MOSFET performance are discussed herein.

Before gate oxidation, the samples were cleaned using conventional RCA solutions, and then split to receive either a conventional wet HF dip (control) or an additional *in situ* HF vapor clean (HFV). During the HF vapor cleaning, the chamber is first pumped down to $<10^{-2}$ Torr. Next, H_2O and HF (~10:1, 1 min for the first step and ~100:1, 2 min for the second step) vapors flow into the chamber and form a mixture with a pressure of around 18 Torr. Following the vapor cleaning, an H_2O vapor purge and a N_2 purge are carrier out, to reduce the fluorine on the bare silicon surface. For the dry dilute O_2 samples (ox), gate oxide, T_{ox} = 4 nm, was grown in dilute O_2 (N_2:O_2 = 6:1) at 800°C and annealed in N_2 at 850°C. Meanwhile, for the N_2O postoxidation annealed samples (oxno), gate oxide, T_{ox} = 3.9 nm, was grown in dilute O_2 (N_2:O_2 = 6:1) at 800°C and annealed in N_2O at 850°C. Nitrogen (N_2^+) was then implanted in the polysilicon gate (50 keV, 2×10^{15}) for the implantation (Imp) samples. The nitrogen was implanted into undoped polysilicon prior to gate electrode dopant implantation (arsenic, 30 keV, 3×10^{15} cm^{-2}). Afterward, a high temperature furnace annealing (850°C for 30 min) was performed to drive the nitrogen (together with the arsenic) to the gate oxide interface, which reduced the concentration of nitrogen (and the arsenic) within the bulk of polysilicon. The standard 0.35 μm CMOS processes are used to fabricate the devices herein. The gate length/width of the test n-MOSFETs are 0.35/20 μm and the area of the MOS capacitor is 10^{-4} cm^2. Oxide thickness was determined using an *n* and *k* analyzer and was consistent with the thickness deduced from capacitance-voltage measurements. Finally, electrical characteristics and hot carrier stress were performed using an HP4156 semiconductor parameter analyzer.

Results and Discussion

Figure 1a displays the atomic force microscope (AFM) surface image of a fresh bare Si wafer. The surface roughness, root mean square (rms), is around ~0.06 nm. Figure 1b shows the AFM surface image of Si wafers after conventional RCA cleaning and wet HF-dipping (Control) while Fig. 1c shows the image after the additional new *in situ* HF vapor cleaning (HFV). The surface of the control sample (rms ≈ 0.15 nm) is rougher than that of the HFV sample (rms ≈ 0.1 nm). This resembles the results reported in Ref. 4, which states that the oxide/Si interface is smoother for the same oxide thickness when grown with *in situ* native oxide removal.

The poly-Si/Si structures were fabricated to monitor the relative quantity of native oxide for the samples herein. Following conven-

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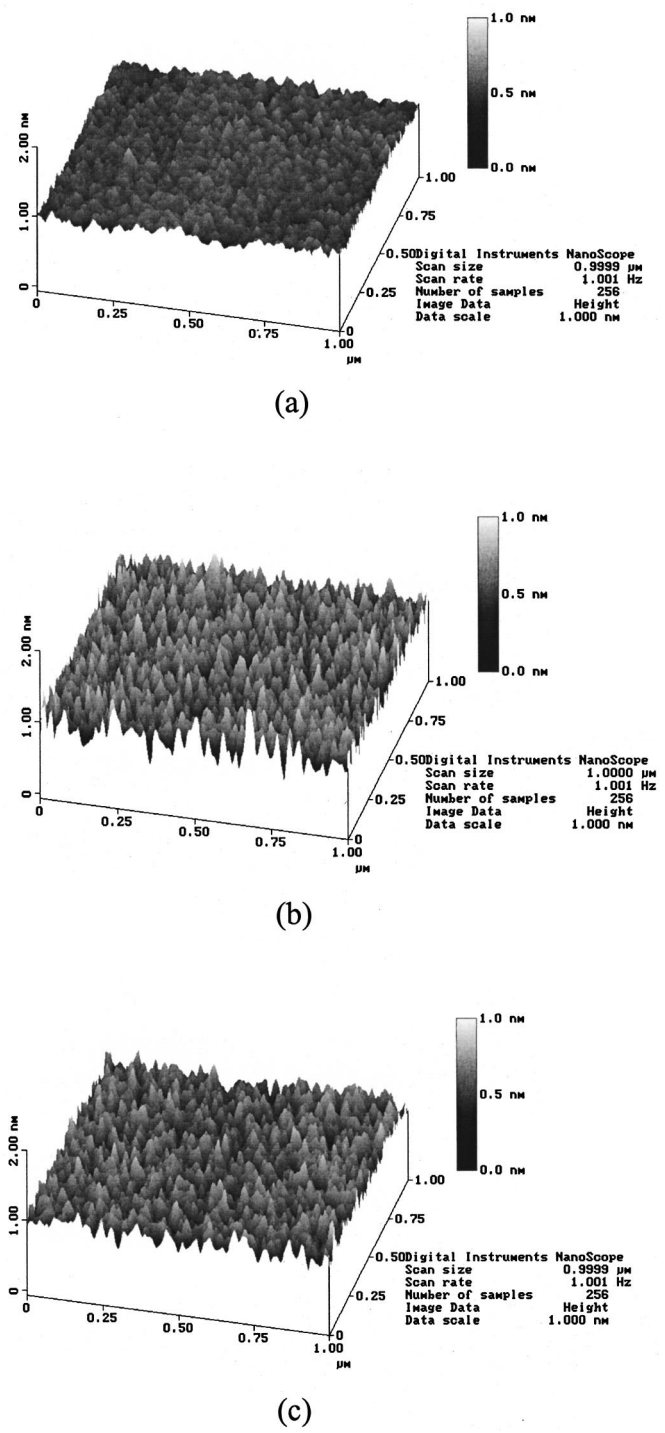

Figure 1. (a) The AFM surface image of fresh bare Si wafer. (b) The AFM surface image of Si wafers after conventional RCA clean and wet HF dip (Control) and (c) conventional RCA clean and *in situ* HFV.

tional RCA cleaning, the samples were divided into one without a conventional wet HF dip (Native), one with a conventional wet HF dip (Control), one with an additional *in situ* HFV, and the poly-Si deposited sequentially without gate oxidation. Figure 2 presents secondary ion mass spectrometry (SIMS) measurements of the depth profiles of interfacial oxygen for the samples. The oxygen peak indicates the relative quantity of native oxide. Clearly, wafers processed through the HF vapor cleaning and poly-Si modules in sequence without exposure to the ambient have a very low oxygen interface (a native-oxide-free interface).

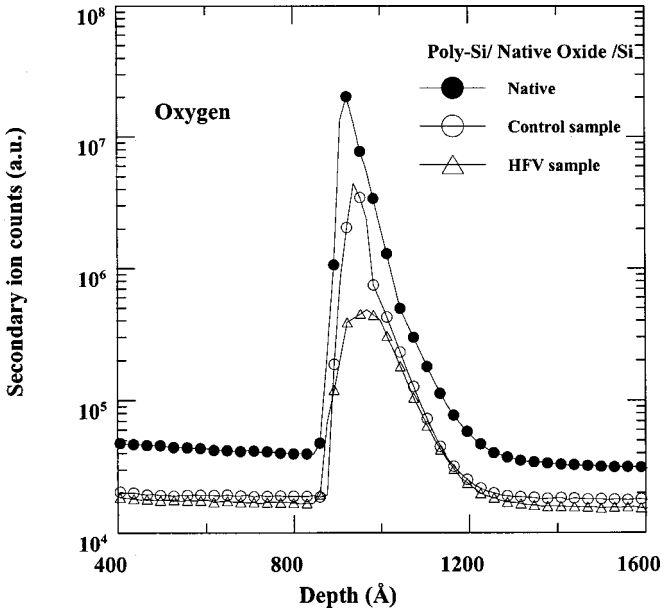

Figure 2. The SIMS depth profile of residual oxygen at the poly-Si/Si interface.

Figure 3a-c shows the leakage current (J-E) characteristics of gate oxides under $-V_g$ injection. HFV treated samples exhibited lower leakage current values than did their counterparts. The excessive leakage current in the other samples is attributed to the presence of intrinsic traps that exist before the oxide is stressed. These intrinsic traps are process-dependent, and thus, are strongly related to the presence of residual native oxide and local thinning in oxide.[17,18] After *in situ* HF vapor cleaning, the native oxide is efficiently removed and a uniform gate oxide thickness can be obtained. Furthermore, in the low field region, the slope of J-E curve differs significantly for the control and HFV samples when compared to the dilute dry O_2 gate oxide, that is, HFV samples exhibit a lower slope than the control sample. Besides, as Fig. 3b and c shows, samples with gate nitrogen implantation exhibit a lower leakage current than do their counterparts. In the low field region, as displayed in Fig. 3c, the slope of the J-E curve is still different for implanted samples and control samples after HFV cleaning. The improvement and the difference of J-E curves are attributed to the incorporation of nitrogen into the gate oxide when nitrogen is implanted in the polysilicon gate.

The subthreshold swing of the HFV-ox (~80 mV/decade) is better than that of the control-ox (~90 mV/decade). Consequently, the interface trap density can be reduced, thus improving the carrier mobility of the deep submicrometer n-MOSFETs by an additional HF vapor cleaning before gate oxidation. Furthermore, the subthreshold swing of the Imp-ox (~74 mV/decade) is better than that of the control-ox (~90 mV/decade). Meanwhile, the subthreshold swing of the HFV-Imp-ox is also ~74 mV/decade. The interface trap density can be reduced and the carrier mobility of deep submicrometer n-MOSFETs improved by combining *in situ* HF vapor cleaning and gate nitrogen implantation.

Figure 4a and b illustrates the Q_{bd} characterization of samples under -1 mA/cm^2 injection. The capacitor area is 50×50 μm. The Q_{bd} value is calculated by counting stress time before soft breakdown of the gate oxide begins. Q_{bd} is clearly improved by HF vapor cleaning. This improvement is attributed to the removal of native oxide and dramatic reduction of the intrinsic trap[17] in the gate oxide. Besides, Q_{bd} is also improved by nitrogen implantation. The samples combining HF vapor clean and nitrogen implantation have the best Q_{bd} values.

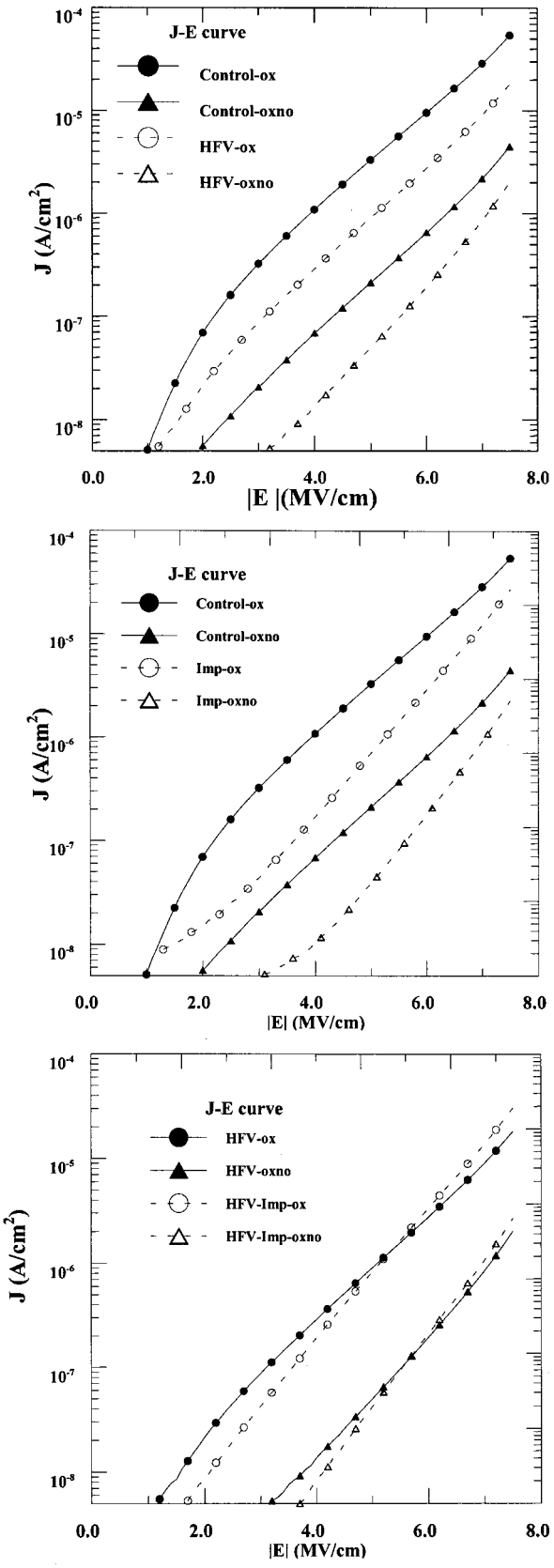

Figure 3. The J-E characteristics of gate oxides grown in dilute dry O_2(T_{ox} = 4 nm) and with N_2O postoxidation annealing (T_{ox} = 3.9 nm) under-V_g injection of (a, top) control and HF vapor samples, (b, center) control and implanted samples, (c, bottom) HF vapor clean and implanted samples.

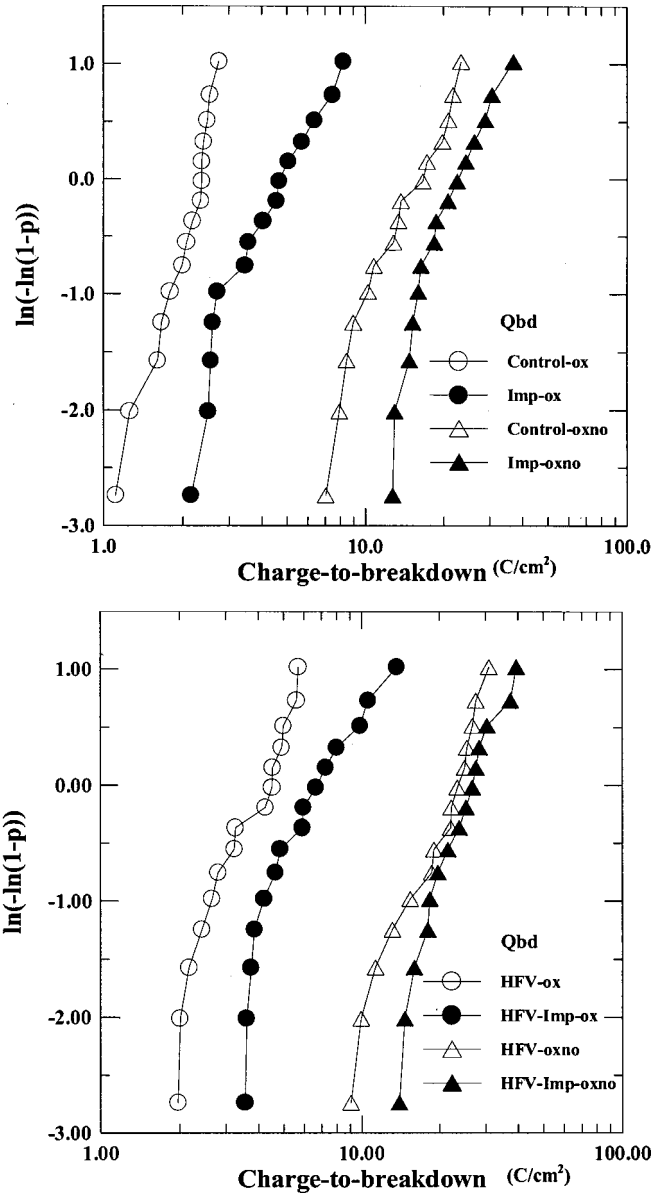

Figure 4. Q_{bd} distributions of (a, top) control and implanted samples (b, bottom) HF vapor clean and implanted samples under −1 mA/cm^2 injection.

Figure 5a-c presents drain current *vs.* drain voltage curves of n-MOSFETs with different gate oxide preparations, while Fig. 6a-c depicts the corresponded transconductance characteristics at V_d = 0.1 V. Notably, both the drain current and transconductance of the HFV samples are higher than those of the control samples. Furthermore, the carrier mobility in the channel of MOSFET is well known to be governed by individual contributions from phonons, channel doping impurities, and interface roughness. Coulomb scattering is dominated by doping impurities in low-field areas and dominated by interface roughness in high-field areas.[4,16,19] In a deep submicrometer n-MOSFET, the transverse electric field (that is, the field orthogonal to the gate oxide interface) attains values higher than 1 MV/cm, and the energy levels of the channel electrons are strongly quantized even at room temperature, while scattering with surface imperfections degrades electron mobility. Since the typical effective electric field at the threshold is close to or higher than 0.5 MV/cm, the mobility of today's MOSFET is always surface roughness-limited.[19] For the control samples, as gate oxide is grown native oxide residues will introduce nonuniform oxide thickness and

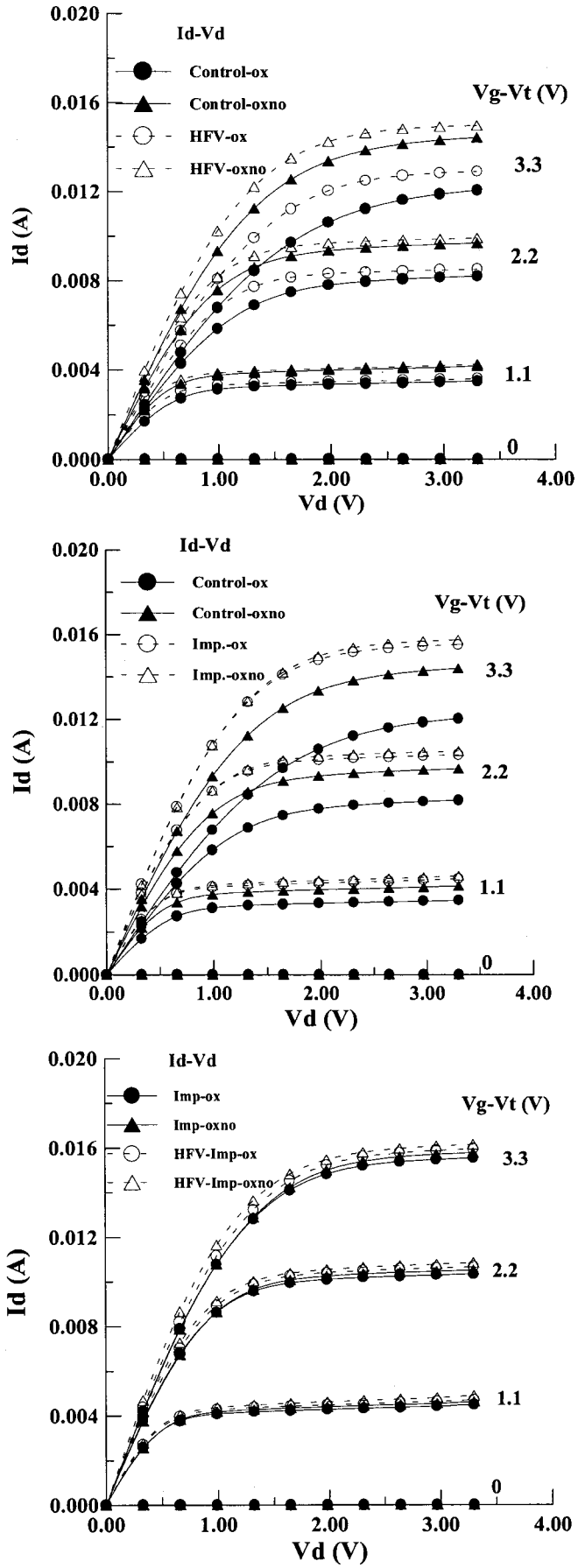

Figure 5. Drain current curves of (a) Control and HF vapor samples, (b) Control and implanted samples, (c) HF vapor clean and implanted samples.

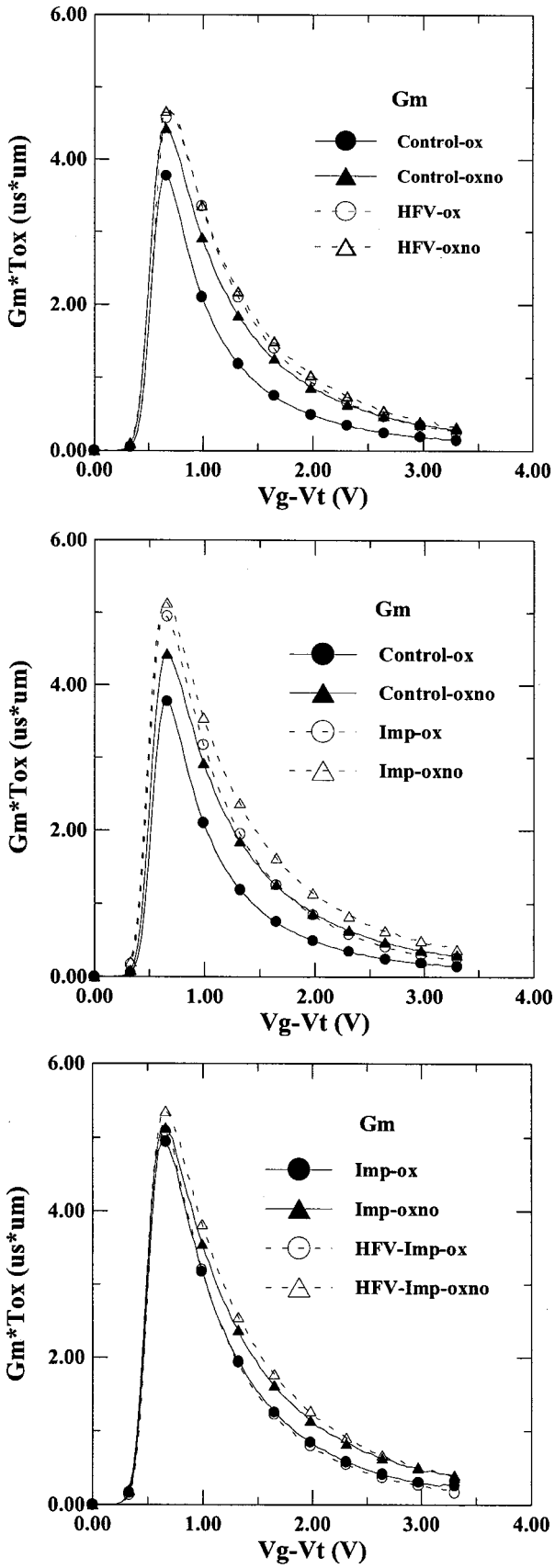

Figure 6. The G_m characteristics at $V_d = 0.1$ V of (a, top) Control and HF vapor samples, (b, center) Control and implanted samples, (c, bottom) HF vapor clean and implanted samples.

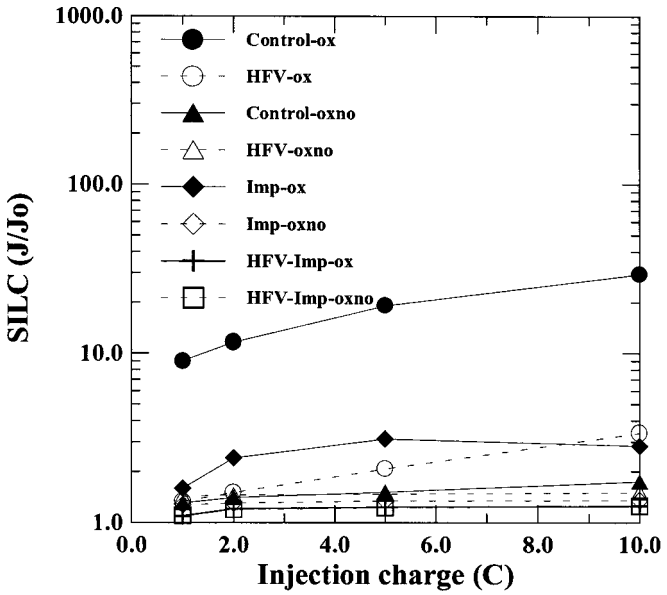

Figure 7. The stress induced leakage current (SILC) of MOS capacitors under -5 mA/cm^2 injection (F-N stressing).

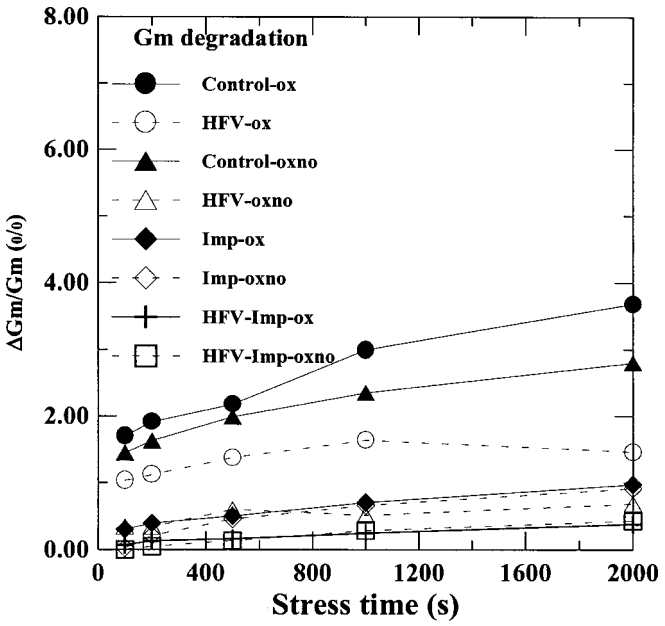

Figure 8. The G_m degradation in 0.35 μm n-MOSFET devices under channel hot carrier stress; V_{ds} = 3.3 V, V_{gs} = 1.15 V.

increase interface roughness, sacrificing the mobility of modern deep submicrometer devices.[18] Consequently, the drain current and transconductance are both degraded, and thus an additional *in situ* HF vapor cleaning and transferring of wafers in the closed ambient can reduce native oxide regrowth and possibly enhance surface roughness. This change will significantly improve the performance of the device. Notably, both the drain current and transconductance of the implanted samples are higher than those of the control samples, a feature that is attributed to the incorporation of nitrogen in the implanted samples.[7-10]

Figure 7 shows the SILC of MOS capacitors under -5 mA/cm^2 injection (Fowler-Nordheim, F-N, stressing). F-N stressing will lead to trap generation, causing reliability problems in the device.[20] Additionally, during F-N stressing, a conductive filament forms locally and is grown in the oxide causing SILC conduction.[21,22] The SILC is lower for samples with nitrogen implantation. Furthermore, for HF vapor cleaned samples, since the native oxide and the associated intrinsic traps contained in the oxide before stress are efficiently removed smooth interface and uniform oxide can be obtained. The stress induced leakage current of those samples is reduced dramatically, and combination of HF vapor cleaning and nitrogen implantation significantly reduces the SILC.

Figure 8 illustrates G_m degradation in 0.35 μm n-MOSFET devices under drain avalanche hot carrier stress at V_{ds} = 3.3 V, V_{gs} = 1.15 V. G_m degradation is significantly improved with the nitrogen implantation, consistent with previous reports.[9,10] Figure 8 also reveals that HF vapor cleaning can improve the hot carrier immunity of n-MOSFET, an improvement that is attributed to the efficient native oxide removal with the subsequent growth of a high quality and reliable ultrathin gate oxide. The combination of HF vapor clean and nitrogen implantation will achieve the best hot carrier immunity.

Figure 9 presents the I_{cp} of devices studied herein. The gate length/width of the n-MOSFET used herein was 5/20 μm, while the measurement frequency was 1 MHz, the amplitude 1.5 V, and source and drain were ground during measurement. The magnitude of the charge pumping current is directly correlated to interface state density (N_{it}) in the fresh (nonstress devices). Meanwhile, the pumping current for the HF vapor cleaned sample is lower than that of the HF dip. Consequently, the interface state density is reduced after HF vapor cleaning, and the interface state density is further reduced by nitrogen implantation. Nitrogen implantation thus suppresses interface generation. This result can be explained by a reduction of highly strained bonds in the oxide films, which can be accomplished owing to the different bonding requirements of segregated nitrogen, as reported by other nitridation techniques.[10] The existence of native oxide in very thin gate oxide causes integrity degradation because the thickness ratio of the native oxide to net thermal oxide increases as the gate oxide becomes thinner. The thickness of the preoxide in the net thermal oxide must be minimized.[23] In the case of control-ox, the thickness ratio of native oxide to net thermal oxide significantly exceeds than that of HFV-ox, as displayed in Fig. 2. This phenomenon degrades the interface of the gate oxide. If nitrogen implantation is applied without the combination of HF vapor cleaning (Imp-ox), the integrity of the gate oxide will still be degraded because of the existence of native oxide in the thin gate oxide. As

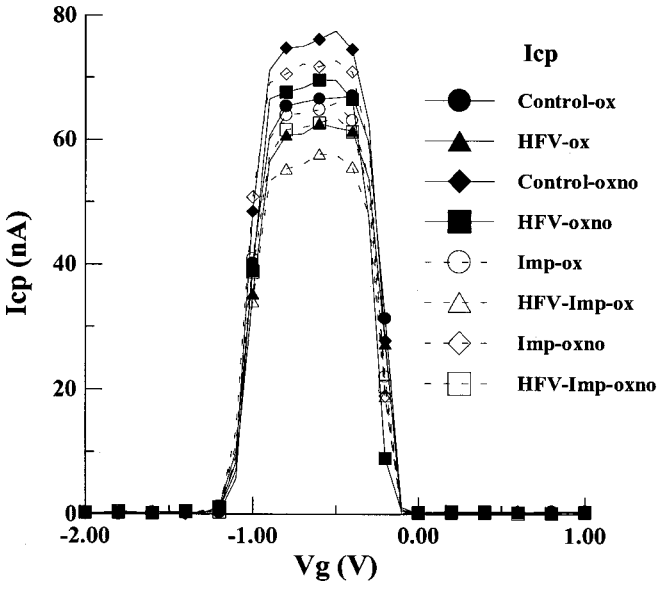

Figure 9. I_{cp} of samples in this experiment.

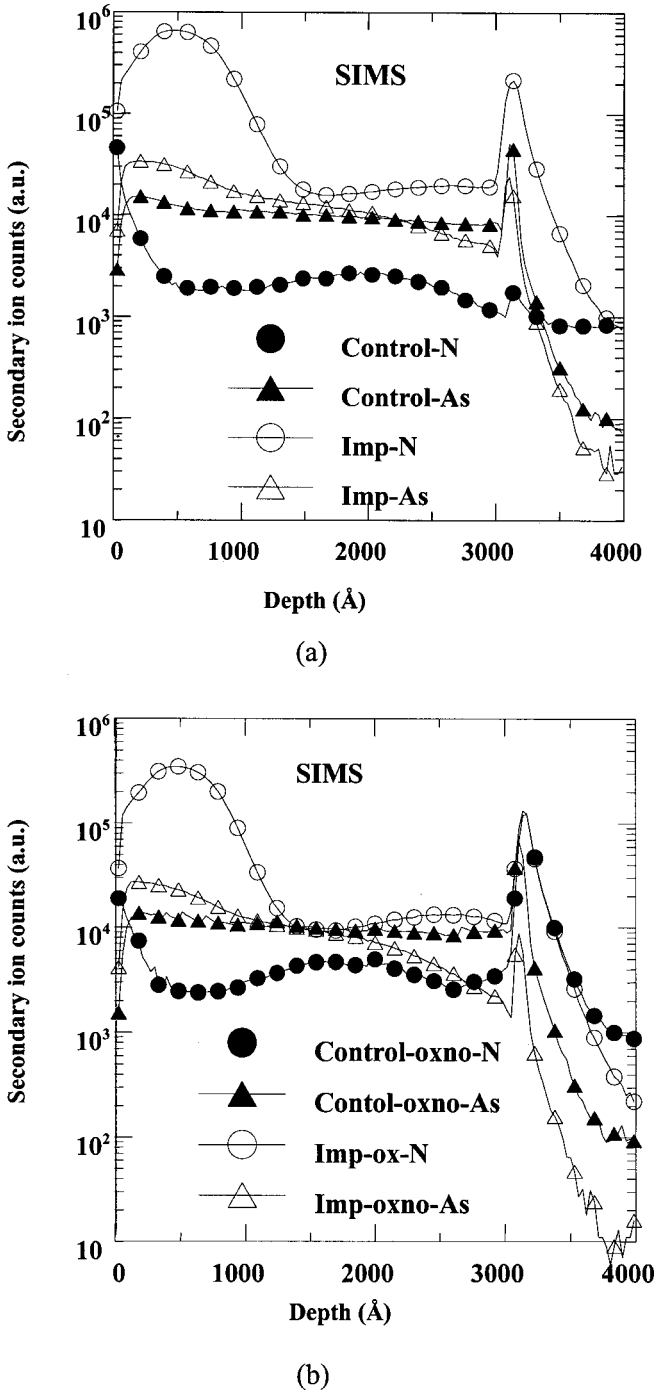

Figure 10. SIMS depth profiles of N and As in control and implanted samples.

Fig. 9 shows, the pumping current is reduced and reaches its minimum after combining nitrogen implantation and HF vapor cleaning.

Dopant (As) penetration from the polysilicon gate to the substrate was also investigated herein. Figure 10a and b shows the SIMS depth profiles of nitrogen and arsenic atoms in the control and implanted samples. The nitrogen atoms were piled up in the polysilicon bulk and at the gate oxide/silicon substrate interface in implanted samples. Meanwhile, nitrogen atoms were reported to be able to suppress dopant (boron) penetration from the polysilicon gate to the silicon substrate by the interface and bulk effect.[8,12] Interface effects include the modification of dopant segregation into the gate oxide, or a pileup of nitrogen atoms at the poly/oxide interface. An example of a bulk effect is a reduction of dopant (boron) diffusivity within the polysilicon bulk.[8] Here, nitrogen was implanted into undoped polysilicon before implantation of the gate electrode dopant (arsenic, 30 keV, 3×10^{15} cm^{-2}). A high temperature furnace annealing (850°C for 30 min) was then done to drive the nitrogen (together with the arsenic) to the gate oxide interface, thus reducing the concentration of nitrogen (and arsenic) in the bulk of polysilicon. Figure 10a and b shows that, in the implanted sample, the arsenic peak nearly coincides with the nitrogen peak in the bulk of polysilicon. Possibly, nitrogen within the polysilicon bulk is primarily responsible for the suppressing dopant (arsenic) penetration, thus reducing levels of arsenic released into the gate oxide. Consequently, device performance is improved, as shown in Fig. 5b.

The use of oxynitrides has been proposed as a diffusion barrier to dopant (boron) penetration into the channel. However, since nitrogen incorporation occurs at the bottom gate of the oxide/substrate interface, dopant (boron) can still enter and degrade the dielectric at the top polysilicon/gate oxide interface.[8] In the case of nitrogen implantation, the nitrogen is introduced into the polysilicon gate and is more effective in suppressing the dopant atom diffusion (herein, arsenic) into the gate oxide. This significantly improves the J-E, I_d, G_m, Q_{bd}, interface state density, and hot carrier reliability for the oxynitride.

Conclusions

This study demonstrates a high performance and reliable deep submicrometer n-MOSFET with ultrathin gate oxide prepared by combining nitrogen gate electrode implant and native-oxide-free *in situ* HF vapor preoxidation cleaning. Additional *in situ* HF vapor cleaning and transferring of wafers in the closed ambient can reduce the regrowth of native oxide and improve the surface roughness. The improved reliability and performance are attributed to the smooth interface and reduced As incorporation in the gate oxide resulting from HF vapor cleaning and nitrogen implantation, respectively. The results presented herein also indicate that the performance and reliability, including the leakage current of ultrathin gate oxide, drain current (I_d), G_m, charge pumping current (I_{cp}), SILC, Q_{bd}, interface state density, and hot carrier reliability of n-MOSFETs are all significantly improved.

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