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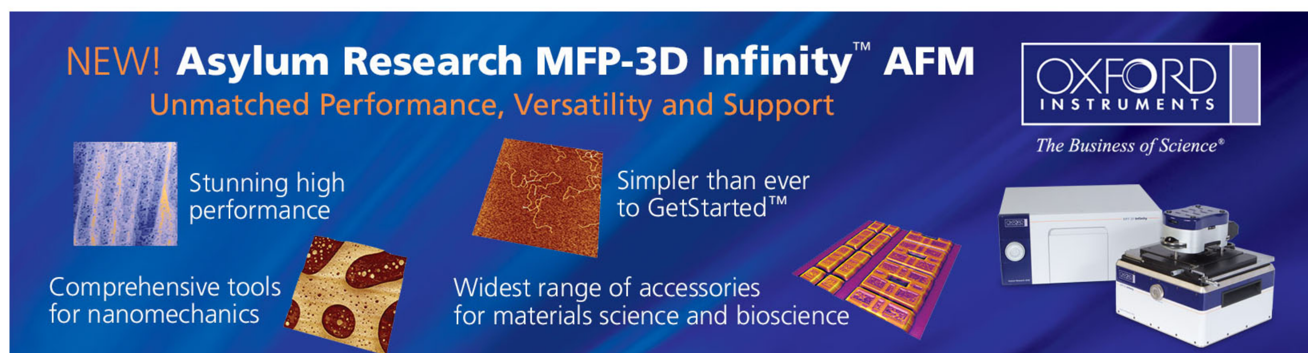


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# Enhanced dopant activation and elimination of end-of-range defects in $BF_2^+$-implanted silicon-on-insulator by high-density current

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Enhanced dopant activation and elimination of end-of-range (EOR) defects in $BF_2^+$-implanted silicon-on-insulator (SOI) have been achieved by high-density current stressing. With the high-density current stressing, the implantation amorphous silicon underwent recrystallization, enhanced dopant activation and elimination of the (EOR) defects. The current stressing method allows the complete removal of EOR defects that has not been possible with conventional thermal annealing in the processing of high-performance SOI devices. © *2001 American Institute of Physics.* [DOI: [10.1063/1.1423773]

Silicon-on-insulator (SOI) has been shown to be an attractive technology for low power, low voltage, and high-speed semiconductor devices.[1,2] The advantages of the devices made on SOI over that on bulk Si are the absence of latchup, reduced parasitic capacitance, process simplification, radiation hardness, and high-temperature operation.[3] Commercial products based on SOI devices have been realized lately by IBM, making SOI a very important technology in semiconductor industry.

Ion implantation in silicon, and specifically in SOI, has been investigated extensively in recent years due to its applications in tailoring material properties and device structures. In particular, ultrashallow $p$-$n$ junctions have been achieved by preamorphization and through oxide implantation processes.[4–6] However, ion implantation leads, after annealing, to the formation of a high density of structural defects beneath the original amorphous/crystalline ($a/c$) interface where the space charge region of the junction extends and causes leakage currents. These defects are called end-of-range (EOR) defects and it is very difficult to prevent them from forming once an amorphous layer is generated during implantation. Furthermore, even after high temperature annealing, it is impossible to annihilate them completely. The defects strongly affect impurity diffusion giving rise to "anomalous" diffusion when they locate within or close to the dopant distribution region.[7]

Conventionally, postimplantation annealing at 900 °C for 30 min or rapid thermal annealing at 1050 °C for 30 s has been employed to activate the dopants. Dopant activation of heavily doped SOI by high-density currents have previously been demonstrated.[8] It remains to be seen that whether the troublesome EOR defects can be removed by high-density currents in heavily doped Si since it is known that conventional thermal processes are incapable of removing all EOR defects. In this letter, electrical current stressing is shown to achieve not only the activation of the electrically inactive dopants but also the removal of all EOR defects. Mechanisms of resistance reduction of Si strips during high-current stressing are discussed.

The wafers used in the present study are 100 mm phosphorus-doped (001) SOI supplied by IBIS Corp. Figures 1(a) and 1(b) show the schematic diagrams of planview and cross-sectional view, respectively, of the test Si strip. The dimensions of the Si strips are 100 $\mu$m long, 200 nm thick, and 10 $\mu$m wide. To fabricate the test structures, a first level mask was used to define the test regions, or the implantation channels. Then the rest of thin film silicon-on-insulator (TFSOI) was etched away by a solution of $HNO_3$ and HF at room temperature. Next a 20-nm-thick screen oxide was grown, followed by 40 keV, $5\times10^{15}\,BF_2^+/cm^2$ implantation into the $n$-type SOI wafers. After implantation, the screen oxide was stripped away by a buffered oxide etchant. Some of the wafers were annealed at 900 °C for 30 min. Low temperature oxide (LTO) was deposited at 450 °C for 2 h. Part of the implantation amorphous Si was regrown into crystalline

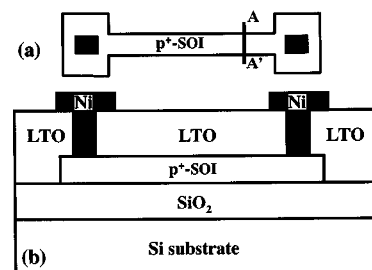


FIG. 1. Schematic diagrams of (a) plan-view and (b) cross-sectional view of the test structure.

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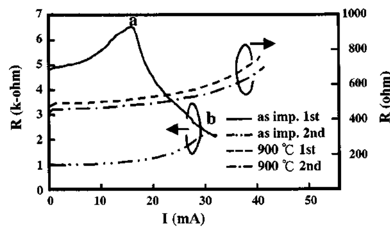


FIG. 2. $I-R$ curves of $BF_2^+$ doped as-implanted and 900 °C annealed SOI channels with two cycles.

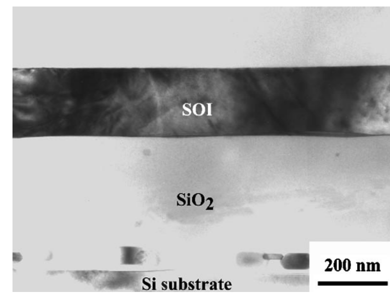


FIG. 4. XTEM image of central region of an as-$BF_2^+$-implanted SOI strip stressed by ramping current to 32 mA.

Si in unannealed sample during the LTO deposition process. On the other hand, for 900 °C annealed samples, all the amorphous layer was converted into crystalline Si. A second mask was then applied to open the contact holes and 150-nm-thick nickel film was deposited by electron-beam evaporation to contact the TFSOI strips. A third mask was used to pattern the Ni contact pads. The advantage of this structure is that the conducting Si strips or channels are isolated by the oxide vertically and horizontally so that the applied current is confined in the channels completely.

Samples were stressed under high-density currents. A Keithley Model 2400 tester was used as the current source and meter. The $I-V$ measurement of the SOI strips was carried out simultaneously. Resistance changes of the SOI strips were measured as a function of applied current, which was ramped from 0 to about 30 or 50 mA at a rate of 0.2 mA/step or 0.2 mA/s. The samples were stressed with two cycles to show the influence of high current on the resistance decrement. The maximum stressing current in the first cycle was limited by the Joule heating or contact failure problems.

The $I-R$ curves of both as-prepared and annealed samples stressed with two cycles are shown in Fig. 2. The resistance change on Si strip was irreversible when applied current was higher than the critical current, defined as the current that the resistance drops suddenly and corresponding to point a in Fig. 2. The total resistance for the as-implanted samples was decreased from 4.8 k to 1 kΩ, about 80% reduction, after the current exceeded 32 mA. The resistance was not reduced further apparently as a result of uneven Joule heating which led to nonuniform structural change in the doped channel as will be described later.

The recrystallization of $a$-Si and release of dopants trapped by defects were found to be the main factors contributing to the resistance reduction of stressed SOI strips. Figure 3 shows cross-sectional transmission electron microscope (XTEM) image of a SOI strip, along $A-A'$ direction in Fig. 1(a), stressed by ramping up the current density to $8\times10^5$ A/cm$^2$ (16 mA) corresponding to the point a in Fig. 2. The growth rate of the $a$-Si was found to increase from the edge to the center of the channel along the $A-A'$ direction. The nonuniform $a$-Si recrystallization indicated the existence of a temperature gradient between the center and edge of the channel. The SOI channel was gradually heated up with the increasing current. Since the SOI strip is buried in the $SiO_2$, the poor heat dissipation led to higher temperature at the center of channel. At higher temperature, regrowth of $a$-Si and activation of dopants would improve the conductivity of the Si channel. Therefore, more dopants were activated and redistributed near the central region of the channel. As a result, the current density in the channel is also expected to be the highest at the center of the channel. Nonuniform heating during current stressing was also inferred from the observation of uneven recrystallization in doped bulk Si channels as described in a previous report. Most of the EOR defects remained due to the inadequate Joule heating since the thermal insulation property of the silicon is relatively poor.[9]

As stressing current was raised beyond $8\times10^5$ A/cm$^2$ (16 mA), the resistance of the channel dropped further. The lower resistance implied that more boron atoms are activated. Figure 4 shows the XTEM image of the central region of the SOI strip with current ramped up to $1.6\times10^6$ A/cm$^2$ (32 mA) corresponding to point b in Fig. 2. EOR defects were no longer evident and were known to be induced from the precipitation of excess Si interstitials atoms and boron atoms which are trapped at the defect periphery.[10] Since the presence of interstitial dopant atoms in the Si lattice will lead to more extensive scattering of electrons during the current stressing, Joule heating will become more severe. The local heating would be high enough to cause the excess interstitial atoms to dissolve and rearrange local atomic positions.[8] As the EOR defects were dissolved, the dopants were increas-

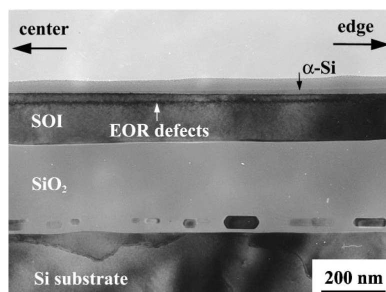


FIG. 3. XTEM image of an as-$BF_2^+$-implanted SOI strip stressed by ramping current to 16 mA.

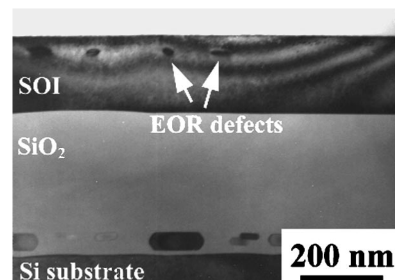


FIG. 5. XTEM image of a $BF_2^+$-implanted SOI strip annealed at 900 °C for 30 min.

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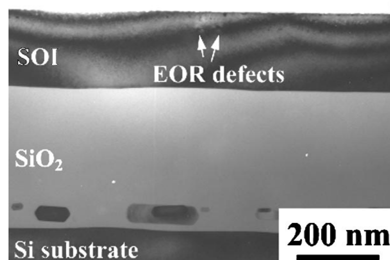


FIG. 6. XTEM image of an annealed at 900 °C for 30 min $BF_2^+$-implanted SOI strip stressed by ramping current to 42 mA.

ingly released and activated. As a result, the elimination of EOR defects led to the further reduction in the resistance of Si strip.

For the samples annealed at 900 °C for 30 min, as shown in Fig. 2, the resistance of the Si strip decreased further from 480 to 450 Ω after stressing with a current of $2 \times 10^6$ A/cm$^2$. Nonuniform heating was also found in this set of samples. Figure 5 shows the XTEM image of a SOI sample annealed at 900 °C for 30 min and without any current stressing. The EOR defects at the center of the doped Si channel were markedly reduced in the stressed samples than those in samples without stressing as shown in Fig. 6. The resistance drop was due to the partial EOR defects elimination and further dopant activation. The local Joule heating may enhance the elimination of EOR defects to release the dopants as well as the dissolution of B/Si-interstitial clusters. A previous study showed that current stressing possesses an additional mechanism, other than the thermal effect, to reduce the resistance. It was speculated that an electrical force as in electromigration might contribute to the dopant activation of the SOI strip.[8]

In summary, recrystallization, enhanced dopant activation and elimination of EOR defects have been achieved by high-density current stressing in $BF_2^+$-implanted silicon in SOI strip. Evidence for the uneven distribution of current flow in the doped SOI strip was obtained from direct observation of more advanced recrystallization and reduction of EOR defects at the central region of the strip by cross-sectional transmission electron microscopy. It was inferred that current flows preferentially at the central region of the doped SOI strip and accentuate the current stressing effects. The current stressing method allows the complete removal of EOR defects that has not been possible with conventional thermal annealing in the processing of high performance SOI devices.

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