Edge Hole Direct Tunneling Leakage in Ultrathin Gate Oxide p-Channel MOSFETs

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***Abstract*—This paper examines the edge direct tunneling (EDT) of holes from p^+ polysilicon to underlying p-type drain extensions in off-state p-channel MOSFETs having ultrathin gate oxides that are 1.2 nm–2.2 nm thick. It is for the first time found that for thinner oxides, hole EDT is more pronounced than both conventional gate-induced drain leakage (GIDL) and gate-to-channel tunneling. As a result, the induced gate and drain leakage is more accurately measured per unit gate width. Terminal currents versus input voltage are measured from a CMOS inverter with gate oxide thickness $T_{\rm OX} = 1.23$ nm, exhibiting the impact of EDT in two standby modes. For the first time, a physical model is derived for the oxide field $E_{\rm OX}$ at the gate edge by accounting for the heavy and light holes' subbands in the quantized accumulation polysilicon surface. This model relates $E_{\rm OX}$ to the gate-to-drain voltage, oxide thickness, and doping concentration of the drain extension. Once $E_{\rm OX}$ is known, an existing direct tunneling (DT) model consistently reproduces EDT current–voltage $(I–V)$, and the tunneling path size extracted falls adequately within the gate-to-drain overlap region. The ultimate oxide thickness limit due to hole EDT is projected.**

***Index Terms*—Direct tunneling (DT), edge direct tunneling (EDT), gate-induced drain leakage (GIDL), MOSFETs, oxide, surface quantization, valence-band electron tunneling (VBET).**

I. INTRODUCTION

THE gate oxide thickness in scaled MOSFETs is now approaching the direct tunneling (DT) regime [1]. The gate leakage due to DT [2] is usually measured per unit oxide area [3], [4], and a certain criterion of 1 A/cm^2 was thought to be the ultimate limit of scalable oxide thickness [3], [4]. For n-channel devices in off-state or in standby mode during the normal circuit operating conditions, the edge direct tunneling (EDT) [5]–[7] of electrons from n^+ polysilicon to the underlying drain extensions not only dominates over the gate leakage, but also can prevail over the conventional gate-induced drain leakage (GIDL) [8], [9]. This paper explores the EDT of holes from p^+ polysilicon to the drain extensions in p-channel devices. The treatment is similar to the one for nMOSFET EDT version [6], [7], which facilitates direct comparisons between the two. Here, we report for the first time that for thinner oxides, hole EDT becomes more significant than the GIDL and gate-to-channel tunneling. This indicates that the induced gate and drain leakage originate from the oxide edge rather than the whole gate oxide, and thus it is best measured or evaluated per unit gate width. To get an understanding of the impact of EDT, we measured current–voltage $(I–V)$ from a CMOS inverter on the same wafer. The ability to model hole EDT $I–V$ is essential. An existing DT $I–V$ model cited in [10], [11] is utilized. Unlike the whole area counterpart where the so-called capacitance–voltage $(C–V)$ integration technique [12] is valid, however, it is very difficult to measure the oxide field at the gate edge—which is the input parameter to the model—since the overlap capacitance is too small to detect using present $C–V$ equipment. To alleviate this problem, we present a physical model for the oxide field $E_{\rm OX}$ at the gate edge by accounting for heavy and light holes' subbands in the quantized accumulation polysilicon surface. This model is quite vital in enabling the consistent reproduction of EDT $I–V$, the extraction of EDT path size and dopant concentration of drain extension, and even the projection of ultimate oxide thickness.

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II. EXPERIMENT AND CHARACTERIZATION

Test patterns including p^+ poly-gate p-channel MOSFETs and CMOS inverters were fabricated in an 0.18-μm process technology [13]. The gate oxides were grown in dilute wet oxygen ambient to three different physical thicknesses: 1.23, 1.85, and 2.16 nm. These oxide thicknesses for p-channel devices were adequately extracted by using an electron DT $I–V$ model [10] and were all confirmed by high-resolution transmission electron microscope (TEM) and a $C–V$ method accounting for polysilicon depletion and quantum mechanical effects, as detailed elsewhere [14]. Other process parameters like poly reoxidation, extension source/drain implant dose, and spacer thermal budget were unchanged.

Fig. 1 illustrates three plausible tunneling leakage paths for off-state p-channel MOSFETs and related band diagrams. With the source open to prevent subthreshold conduction and $V_{\rm D} = -V_{\rm G}$, where $V_{\rm D}$ is drain voltage and $V_{\rm G}$ is gate voltage, the measured drain current $I_{\rm D}$, gate current $I_{\rm G}$, and bulk current $I_{\rm B}$ are plotted in Fig. 2 versus $V_{\rm GD}$ $(= V_{\rm G} - V_{\rm D})$ for three different oxide thicknesses. Fig. 2(a) and (b) reveals that the drain current is primarily due to the GIDL and the gate current, with EDT being the origin of the latter component. It is seen that a certain range of $V_{\rm GD}$ exists where the EDT dominates over the GIDL, and this range is extended for decreased gate oxide

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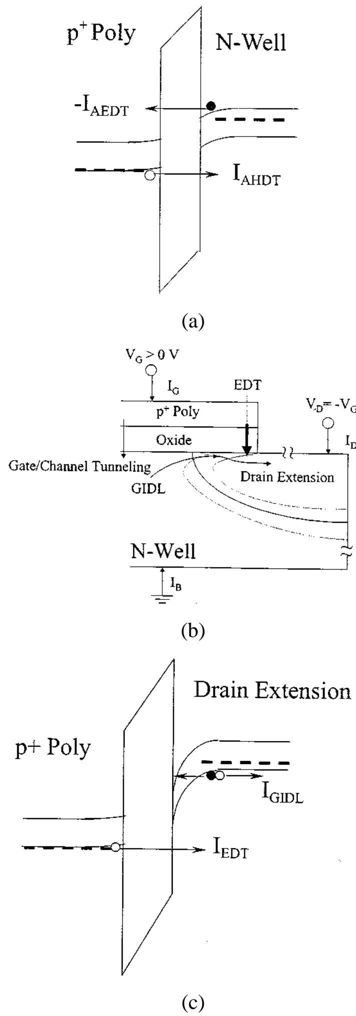


Fig. 1. (a) Band diagram located at channel region far from drain extension region. Accumulation hole DT current (I_{AHDT}) and electron DT (I_{AEDT}) both contribute to gate/channel tunneling. (b) Schematic cross section near gate/drain overlap region under $V_{\mathrm{G}} > 0$ V and $V_{\mathrm{D}} = -V_{\mathrm{G}}$. Three tunneling current paths are shown. (c) Band diagram located at gate/drain overlap region, showing hole EDT and GIDL.

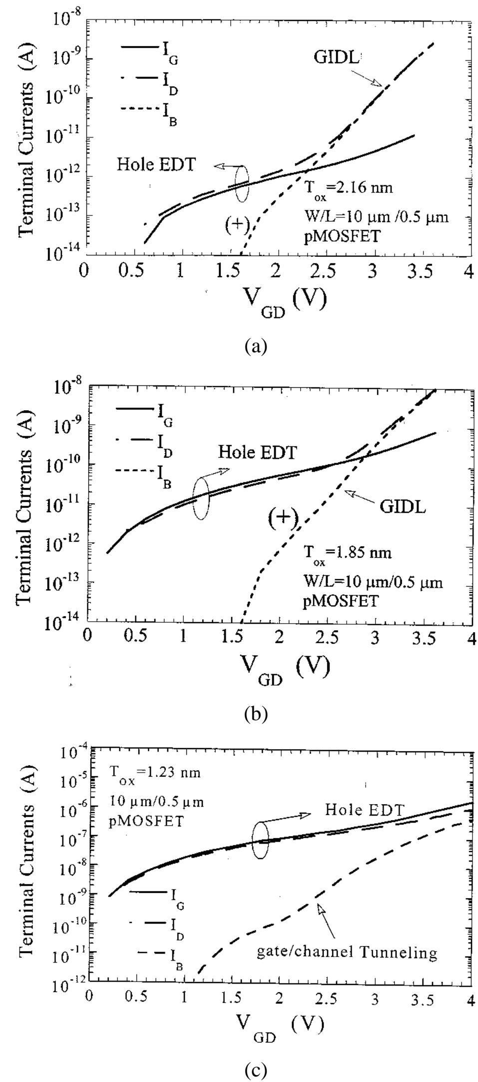


Fig. 2. Measured terminal currents versus V_{GD} for (a) $T_{\mathrm{OX}} = 2.16$ nm; (b) $T_{\mathrm{OX}} = 1.85$ nm; and (c) $T_{\mathrm{OX}} = 1.23$ nm, under $V_{\mathrm{D}} = -V_{\mathrm{G}}$ and source open. The aspect ratio $W/L = 10\ \mu\mathrm{m}/0.5\ \mu\mathrm{m}$. In (a), hole EDT dominates the drain leakage I_{D} in $0\ \mathrm{V} < V_{\mathrm{GD}} < 2.3$ V. In (b), hole EDT dominates I_{D} in $0\ \mathrm{V} < V_{\mathrm{GD}} < 2.6$ V and GIDL constitutes drain leakage for $V_{\mathrm{GD}} > 2.6$ V. In (c), the edge tunneling mechanism dominates the drain leakage current.

thickness. We attribute the EDT herein to hole tunneling rather than valence electron tunneling. This is based on the band diagrams in Fig. 1 which show that for low-voltage V_{GD}, it is extremely improbable that valence electrons will tunnel across the oxide to the forbidden gap in polysilicon side. In Fig. 2(c) for $T_{\mathrm{OX}} = 1.23$ nm, the bulk current is solely due to gate-to-channel tunneling, making GIDL impossible to detect. Note that hole EDT dominates the gate current for all T_{OX}. With the source grounded and $V_{\mathrm{D}} = -1.8$ V, the measured terminal currents versus both polarities of V_{G} are plotted in Fig. 3. Obviously, the GIDL dominates the drain leakage for $T_{\mathrm{OX}} = 2.16$ nm, while for a thinner T_{OX} of 1.85 nm hole EDT dominates from $0\ \mathrm{V} < V_{\mathrm{G}} < 0.9$ V, and eventually the drain leakage is entirely controlled by hole EDT for $T_{\mathrm{OX}} = 1.23$ nm. Fig. 3(c) shows the bulk current reversal phenomenon due to two opposite sources: GIDL and gate-to-channel tunneling. Regarding on-state I–V (negative V_{G}) in Fig. 3, the impact of hole DT from the inverted channel on degrading drive capability is described in our recent work [14]. Particularly for $V_{\mathrm{G}} < -1$ V in Fig. 3(c), the significant I_{B} is attributed to valence-band electron tunneling (VBET) from the p^{+}-polysilicon to the conduction band of the n-well. We also found experimentally that the hole EDT leakage is indeed proportional to the gate width, regardless of the aspect ratio. This again suggests that the induced gate and drain leakage is better measured or evaluated per unit gate width.

Fig. 4 displays the supply current and input current versus input voltage V_{IN} measured for a CMOS inverter with $T_{\mathrm{OX}} = 1.23$ nm and with supply voltage V_{DD} as a parameter. It can be observed in Fig. 4(a) that:

1) at low-level state ($V_{\mathrm{IN}} = 0$ V), the standby current is due to the electron EDT [5]–[7] in the off-state n-channel device and the hole DT from the inverted channel in the on-state p-channel device [14];
2) at high-level state ($V_{\mathrm{IN}} = V_{\mathrm{DD}}$), the standby current comes from the hole EDT in the off-state p-channel device and the electron DT from the inverted channel in the on-state n-channel device.

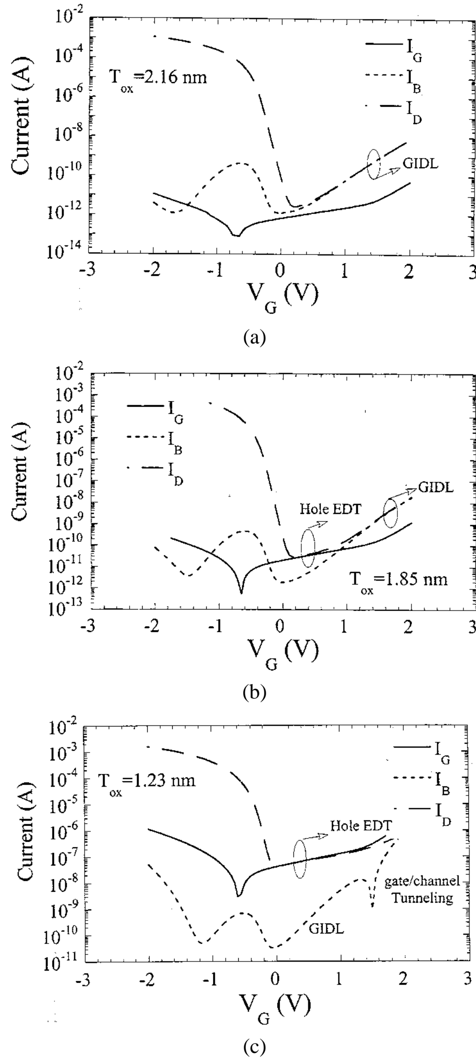


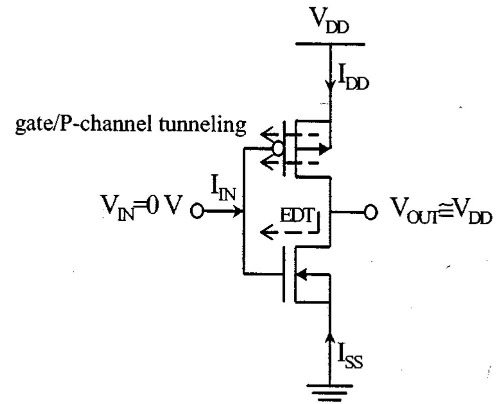
Fig. 3. Measured terminal currents versus gate voltage for both polarities. The aspect ratio is $W/L = 10\ \mu\text{m}/0.5\ \mu\text{m}$. Source grounded and $V_D = -1.8$ V.

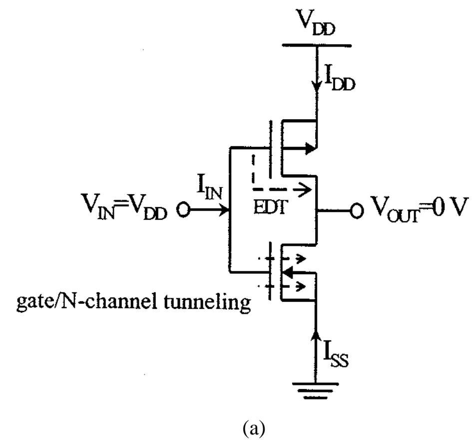
Attached in Fig. 4(b) is the measured ratio of each component. For the inverter in low-level state, $V_{\text{IN}} = 0$ V, the electron EDT resulting from the off-state nMOSFET accounts for 25% of the total input leakage current while the hole DT current originating from on-state pMOSFET accounts for 75%. As for high-level state $V_{\text{IN}} = V_{\text{DD}}$, the hole EDT resulting from off-state pMOSFET is responsible for 36% of the total input leakage current while the electron DT current originating from on-state nMOSFET contributes the rest. Note that the apparent difference of 36% versus 25% in EDT contribution can be attributed to the fact that the p-channel pull-up device has about two times the gate width of the n-channel pull-down device. Obviously, as channel length continues to shrink, the role of EDT substantially increases since diffusion extension does not easily scale [5], [15].

III. Hole EDT Modeling

By following a published analytic electron DT model [11], a hole EDT version was built

$$I_{\text{EDT}} = A_o \sum_{i=\text{H,L}} Q_i f_i T_i = L_{\text{TP}} W \sum_{i=\text{H,L}} Q_i f_i T_i \quad (1)$$





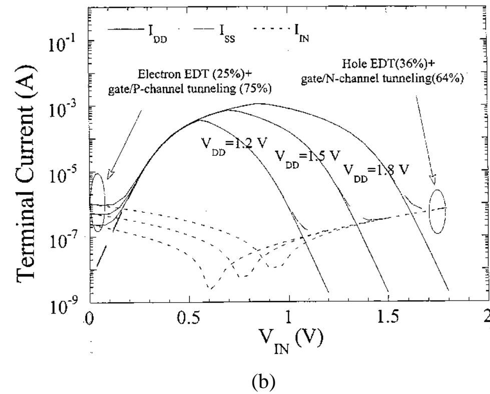


Fig. 4. (a) Gate leakage paths in two standby modes. (b) Measured supply currents I_{DD} and I_{SS}, and input current I_{IN} versus input voltage V_{IN} for an inverter with $T_{\text{OX}} = 1.23$ nm and with supply voltage V_{DD} as a parameter. The gate length is 0.18 μm.

where

H	heavy hole;
L	light hole;
$A_o (= L_{\text{TP}} \times W)$	effective tunneling path area;
L_{TP}	effective tunneling path size;
Q_i	sheet charge of the accumulation layer;
f_i	hole impact frequency on p^+-poly/SiO_2 interface;
T_i	modified Wentzel-Kramer-Brillouin (WKB) transmission probability including the interface reflection correction.

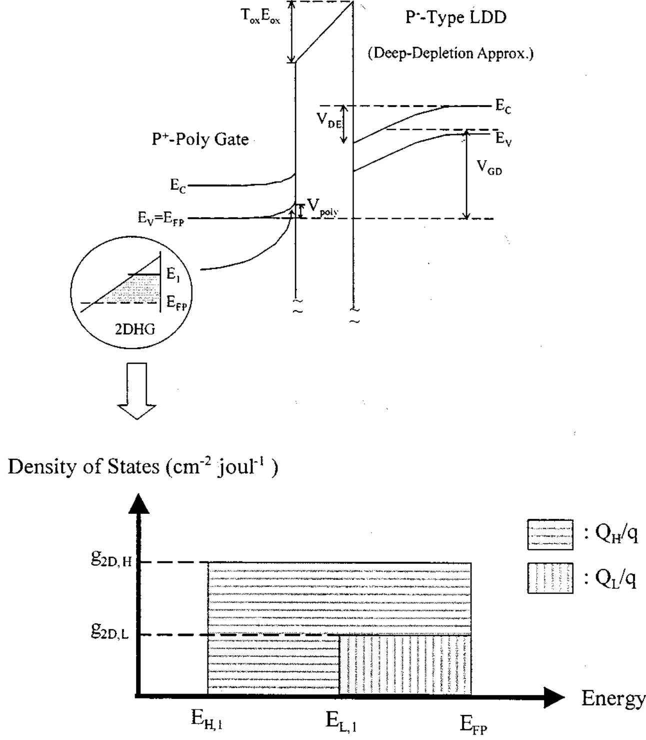


Fig. 5. Band diagram drawn along p$^+$-polysilicon/oxide/drain extension. The accumulation potential bending, $V_{\rm poly}$, with 2-D hole gas (2DHG) concept and the silicon surface potential, $V_{\rm DE}$, with the deep depletion approximation are adopted in the procedure of $E_{\rm OX}$ calculation.

The oxide field $E_{\rm OX}$ at gate edge is a key input parameter to the model. It has to be estimated under each value of $V_{\rm GD}$. In our work, the C–V integration technique failed to extract $E_{\rm OX}$ because hole EDT occurs only within the area of gate/drain overlap region and it is difficult to measure such a small capacitance in the overlap part. $E_{\rm OX}$ at the gate edge can be obtained by solving the following equation:

$$V_{\rm GD} - V_{\rm FB}\,(\simeq 0) = V_{\rm poly} + T_{\rm OX}E_{\rm OX} + V_{\rm DE} \qquad (2)$$

where $V_{\rm poly}$ is the potential drop in the p$^+$ polysilicon and $V_{\rm DE}$ is that in the drain extension region. We apply the first subband approximation to accumulated p$^+$ poly-gate and the deep depletion approximation to the underlying drain extension region, as shown in Fig. 5 The charge Q available for tunneling is modeled as field induced, i.e.,

$$Q = \epsilon_{\rm OX}E_{\rm OX}. \qquad (3)$$

Relating this sheet charge density to the number of occupied subband states leads to the charge conservation relationship $Q = Q_{\rm H} + Q_{\rm L}$. Here, $Q_{\rm H} = q(E_f - E_{\rm H,1})g_{\rm 2D,H}$ and $Q_{\rm L} = (E_f - E_{\rm L,1})g_{\rm 2D,L}$. This leads to

$$q\left[(E_f - E_{\rm H,1})g_{\rm 2D,H} + (E_f - E_{\rm L,1})g_{\rm 2D,L}\right] = \epsilon_{\rm OX}E_{\rm OX}. \qquad (4)$$

Here, $g_{\rm 2D} = m_{\|}/\pi\hbar^2$ represents the two-dimensional (2–D) density of states. The quantized energy of the first subband E_1 can be estimated directly with Sommerfeld-Wilson's quantization rule under triangle-like electrostatic potential approximation to the polysilicon surface

$$E_1 = \left(\frac{\hbar^2}{2m_\perp}\right)^{1/3}\left(\frac{9\pi q\epsilon_{\rm OX}E_{\rm OX}}{8\epsilon_{\rm Si}}\right)^{2/3}.$$

We thus get

$$V_{\rm poly} \simeq \frac{E_f}{q} = \frac{\epsilon_{\rm OX}}{q^2(g_{\rm 2D,H}+g_{\rm 2D,L})}E_{\rm OX} + \frac{g_{\rm 2D,H}E_{\rm H,1}+g_{\rm 2D,L}E_{\rm L,1}}{q(g_{\rm 2D,H}+g_{\rm 2D,L})} \qquad (5)$$

$$V_{\rm DE} = \frac{\epsilon_{\rm OX}^2E_{\rm OX}^2}{2q\epsilon_{\rm Si}N_{\rm DE}} \qquad (6)$$

where $N_{\rm DE}$ is the dopant concentration of the drain extension. As a result, (2) can be further rearranged as

$$V_{\rm GD} = a_1E_{\rm OX} + a_2E_{\rm OX}^2 + a_3E_{\rm OX}^{2/3} \qquad (7)$$

where

$$a_1 = T_{\rm OX} + \frac{\epsilon_{\rm OX}}{q^2(g_{\rm 2D,H}+g_{\rm 2D,L})}$$

$$a_2 = \frac{\epsilon_{\rm OX}^2}{2q\epsilon_{\rm Si}N_{\rm DE}}$$

$$a_3 = \frac{1}{q(g_{\rm 2D,H}+g_{\rm 2D,L})} \times \left[g_{\rm 2D,H}\left(\frac{\hbar^2}{2m_{\rm H,\perp}}\right)^{1/3}\left(\frac{9\pi q\epsilon_{\rm OX}}{8\epsilon_{\rm Si}}\right)^{2/3} + g_{\rm 2D,L}\left(\frac{\hbar^2}{2m_{\rm L,\perp}}\right)^{1/3}\left(\frac{9\pi q\epsilon_{\rm OX}}{8\epsilon_{\rm Si}}\right)^{2/3}\right].$$

For $\langle 100\rangle$ poly-grain orientation, $m_{\rm H,\perp} = 0.29m_o$, $m_{\rm H,\|} = 0.433m_o$; $m_{\rm L,\perp} = 0.20m_o$, $m_{\rm L,\|} = 0.169m_o$ as cited in [16]. Thus, it is easy to extract $E_{\rm OX}$ by solving (7) numerically. Once $E_{\rm OX}$ is quantified, we can compute the hole EDT current in terms of (1). We found from experiments (similar to [6], [7]) that EDT is insensitive to the n-well bias under off-state condition. This suggests that the lateral field component in the gate-to-drain overlap region can reasonably be ignored. In other words, a one-dimensional (1-D) approach is sufficient in our work. In carrying out the above model, it was found that the slope of $I_{\rm G}$ versus $E_{\rm OX}$ depends strongly on $N_{\rm DE}$. An excellent reproduction was achieved with a drain extension doping of $N_{\rm DE} =$

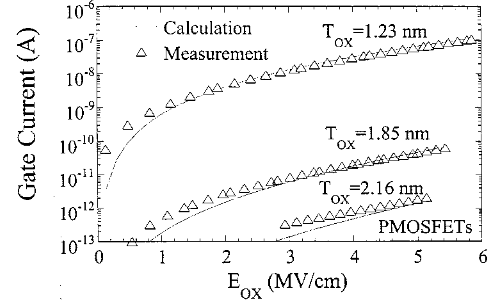


Fig. 6. Comparison of the calculated and experimental hole EDT current versus $E_{\rm OX}$. The extracted effective EDT range is 6 nm wide from the gate edge. $W = 10\ \mu$m.

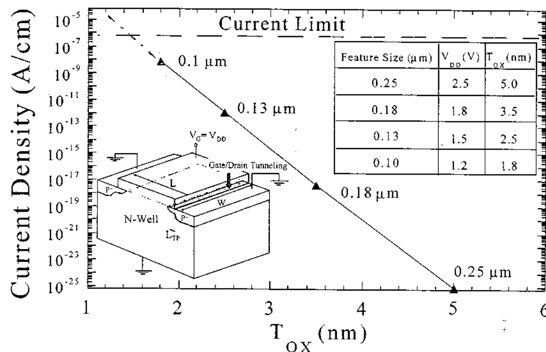


Fig. 7. Calculated hole DT current per gate width versus scaling generation oxide thickness in pMOSFETs. The table shows the scaling parameters from [1]. The inset schematically exhibits the hole EDT path in pMOSFET structure. $L_{\rm TP} = 6$ nm.

8×10^{18} 1/cm^3 and effective mass, $m_{\rm oxh} = 0.38 m_o$ for both heavy and light holes resulting from the parabolic dispersion relation in tunneling oxide, as depicted in Fig. 6. The extracted tunneling path size $L_{\rm TP}$ was 6 nm wide from the gate edge since the extracted $N_{\rm DE}$ quite matches the experimental one in the highly-doped region. This is reasonable since the drain extension beneath the gate is about 8 nm. Therefore, the modeling work validates the hypothesis that hole EDT is the origin of the leakage in pMOSFETs.

It was very recently recognized [5], [15] that the drain extension may be considered a nonscalable factor, implying a constant $L_{\rm TP}$ of 6 nm in the scaling direction. With this in mind, the conventional criterion of 1 A/cm^2 can be effectively transformed to 0.6 μA/cm. Using the roadmap parameters [1], the hole EDT current was calculated versus scaling generation oxide thickness, as shown in Fig. 7. In this figure, the new criterion due to hole EDT sets the ultimate oxide thickness to around 1.42 nm.

IV. Conclusion

The EDT of holes from p$^+$ polysilicon to the underlying p-type drain extension has been shown to have a tremendous impact on the drain leakage and gate leakage. This unwanted effect is more serious for thinner oxide thickness. It is shown that the gate leakage in practical standby mode should be measured or evaluated per unit gate width rather than by the whole gate area. We have shown experimentally that EDT contributes a significant amount of leakage current in a CMOS inverter and is the dominant source of leakage for $T_{\rm OX} = 1.23$ nm. A physical model has been developed that consistently reproduces experimental EDT I–V characteristics. The extracted tunneling area has been found to fall within the gate-to-drain overlap region and the ultimate oxide thickness limit due to hole EDT has been projected.

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Simon S. M. Jang received the B.S. and M.S. degrees from the National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1985 and 1987, and the Ph.D. degree from the Massachusetts Institute of Technology (MIT), Cambridge, in 1993, all in materials science and engineering. His dissertation work included Si/ge CVD technology, kinetics, and thermal stability for HBT application. Sponsored by IBMand SRC, his reseach was conducted in the Microsystems Technology Laboratories, MIT, under the guidance of Prof. R. Reif in electrical engineering.

He joined Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, in 1993. He has successfully developed ozone-TEOS, spin-on coating, HDPCVD dielectrics, PECVD SiON anti-reflection layer, and CMP processes for 0.5-0.18 μm CMOS technologies. He is now the Manager of Dielectric/CMP Projects in the Advanced Module Technology Division, R&D, responsible for the modules of shallow trench isolation, gate stack, ultrashallow junction, interpoly-metal dielectric, low-K intermetal dielectric, and oxide, tungsten and copper CMP for 0.13 μm generation and beyond. He has authored or co-authored more than 40 technical papersand received 48 U.S. patents and 50 Taiwanese patents.

Dr. Jang is a member of Phi Tau Phi.

Douglas C. H. Yu received the Ph.D. degree from the Material Engineering Department of the Georgia Institute of Technology, Atlanta.

He joined AT&T Bell Laboratories, Allentown, PA, where he was involved in work on PECVD thin-film processing, 256 K/l Mb SRAM process integration and yield improvement, 0.35-/0.25-μm ultrahigh performance logic device development, modularBiCMOS, and MiM process integration. He later joined the R&D Department of the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C., where he led a module team to successfully develop TSMC's 0.5-μm, 0.35-μm, 0.25-μm, and 0.18-μm core logic technologies. He performed yield improvement and transferred the process to manufacturing. He also managed an advanced technology team to develop and qualify TSMC's first Cu technology for 0.18-μm technology. Recently, he developed TSMC's 0.13-μm Cu/low-K technology and transfers to manufacturing. Currently, he manages a module team to develop TSMC Cu/low-K interconnect, gate stack, silicide, shallow-trench-isolation, etc. He has been been awarded 138 U.S. patents. He also has numerous publications in technical journals and conferences, all in the area of VLSI processing, device, and integration.

Mong-Song Liang received the B.S. and M. S. degrees from the National Cheng-Kung University, Taiwan, R.O.C., in 1975 and 1977, respectively, and the Ph.D. degree in 1983 from the University of California (UC), Berkeley, all in electrical engineering and computer sciences. At UC Berkeley, his research was on the scaling of ultrathin gate dielectrics and device reliability physics.

In 1983, he joined Advanced Micro Devices (AMD), Sunnyvale, CA, where he worked on nonvolatile memory technologies (EEPROM and EPROM). From 1988 to 1992, he was with Mosel Electronics Corporation, Sunnyvale, where he worked on SRAM and embedded memory technology (emb-DRAM, emb-SRAM, and emb-Flash) development. He was the Director of Memory Division of the R&D Organization until 1998. His current assignment is Senior Director of Advanced Module Technology Division of the R&D Organization. He is responsible for all advanced modules development, including etch, thin film, diffusion, CMP, and Cu/low-K interconnect.