Tunnel Oxide Prepared by Thermal Oxidation of Thin Polysilicon Film on Silicon (TOPS)

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Abstract—**This letter presents a textured tunnel oxide, TOPS, prepared by thermally oxidizing a thin polysilicon film on a Si substrate. Due to the rapid diffusion of oxygen through the grain boundaries of the thin polysilicon into Si substrate and the enhanced oxidation rate at the grain boundaries, a textured Si/SiO_2 interface is obtained. The textured interface results in the localized high fields and enhances electron injection into TOPS. The TOPS exhibits a higher electron injection efficiency, a better immunity to the electron trapping and the interface state generation under the high-field operation, and a higher asymmetric injection polarity as compared to the normal oxide.**

I. Introduction

THIN tunnel oxides (≤ 100 Å) or thick polyoxides (oxides grown on polysilicon, ≈ 600 Å) are used as the tunneling gate dielectrics of electrically erasable programmable read-only-memories (EPROM's) [1]. It had been reported that thermal oxides grown on an n^+ heavily-doped silicon substrate exhibited a higher electron conduction efficiency due to the reduction of the effective barrier height at the Si/SiO_2 interface [2]. Recently, Fong *et al.* [3] and Hao *et al.* [4] have also reported that tunnel oxide grown on a pretexturized silicon substrate can achieve the enhanced electron conduction efficiency due to the surface field enhancement.

In this letter, we propose a novel simple method to fabricate a thin textured tunnel oxide with a higher electron conduction efficiency, a lower electron trapping rate, and a highly asymmetric injection polarity.

II. Experimental Procedures

The thin textured tunnel oxide capacitors were fabricated on n-type 0.55–1.1 $\Omega \cdot$cm (100) Si wafers. Some wafers were heavily doped by using an arsenic ion implantation of a dose of 5×10^{15} cm^{-2} at 100 keV through a 500-Å pad oxide followed by annealing at 900°C in an N_2 ambient for 40 min. After removing the pad oxide, a very thin amorphous silicon (α-Si) film (≤ 100 Å) was deposited on Si wafers at 550°C by using an LPCVD system. In this study, the deposition rate and deposition pressure of a α-Si were controlled at about 20 Å/min and 150 mtorr, respectively. The thickness of α-Si film was estimated by the deposition rate and deposition time. The wafers were carefully loaded into furnace at 600°C to reduce the thermal stress and to minimize the native oxide growth. The temperature was gradually raised to 900°C in an N_2 ambient. During the temperature ramping-up step, the α-Si films were crystallized into polysilicon [5]. Then, thin tunnel oxides were grown by completely oxidizing the thin polysilicon films at 900°C in a dry O_2 ambient. Due to the rapid diffusion of oxygen through the grain boundaries of thin polysilicon into Si substrate and the enhanced oxidation rate at the grain boundaries, a textured Si/SiO_2 interface is obtained. As a result, after the polysilicon was completely converted into the oxide, an irregular and textured interface with the Si substrate was formed. This textured tunnel oxide is referred to as TOPS. To characterize the textured tunnel oxide, a 4000-Å $POCl_3$-doped polysilicon layer was then deposited on TOPS to form MOS capacitors. For comparison, MOS capacitors with the normal oxide were also made at 900°C with a similar thickness as that of TOPS. The effective oxide thickness of TOPS was determined by the high-frequency *CV* measurement. The transmission electron microscopy (TEM) was used to examine the morphology of the Si/SiO_2 interface.

III. Results and Discussion

Fig. 1 shows the TEM micrograph of the cross section of TOPS, where a textured Si/SiO_2 interface is clearly observed. The textured interface results in the localized high fields and enhances electron injection into TOPS.

Fig. 2 shows the accumulation-mode and inversion-mode J_g–V_g characteristics of TOPS and normal oxide with a thickness of about 100 Å. The thickness of the stacked α-Si is about 50 Å and the area of the samples is 2.8×10^{-4} cm^2. It is seen that the TOPS exhibits a much higher electron conduction efficiency than the normal oxide in both injection polarities. For example, for a constant injection current density of 10 mA/cm^2, which is the typical rapid charging of the floating gate [3], the TOPS with the textured interface reduces the gate voltage from

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Fig. 1. TEM micrograph of the cross section of TOPS.

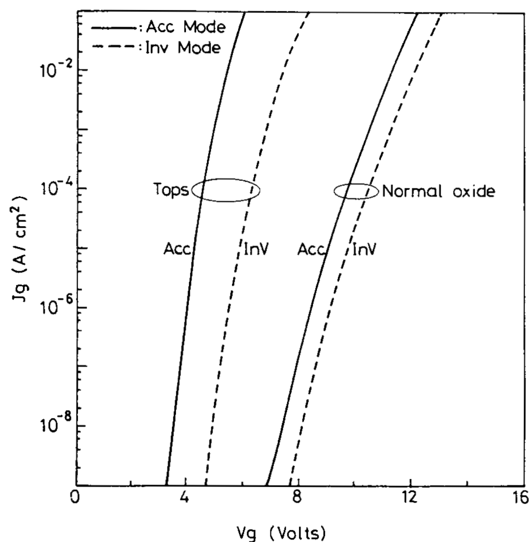

Fig. 2. The accumulation-mode and inversion-mode J_g–V_g characteristics of TOPS and normal oxide of 110 Å thickness grown on the lightly doped substrate.

about 11.2 V of the normal oxide to about 5.5 V for the accumulation-mode J_g–V_g characteristics.

It is interesting that, as shown in Fig. 1, the degree of the texturization of the Si/SiO_2 (bottom) interface is much larger than that of the poly-Si/SiO_2 (top) interface. Hence, the electron injection from the bottom interface into TOPS is much more efficient than from the top interface. For example, the current density at $V_g = 5$ V of electron injection from the bottom interface is about five orders in magnitude larger than that of electron injection from the top interface. The asymmetrical characteristics have special advantages for the EEPROM device application.

Fig. 3 shows the J_g–E_{ox} characteristics of TOPs (160 Å) and normal oxide (180 Å) grown on the heavily doped substrate. The thickness of the stacked α-Si is about 75 Å. It is seen that the enhanced electron injection efficiency becomes more significant. This is due to the textured Si/SiO_2 interface of TOPS, in conjunction with the substrate heavy doping effect [2].

Fig. 4 shows the curves of the gate voltage shift (ΔV_g) versus the stressing time of TOPS and normal oxide under

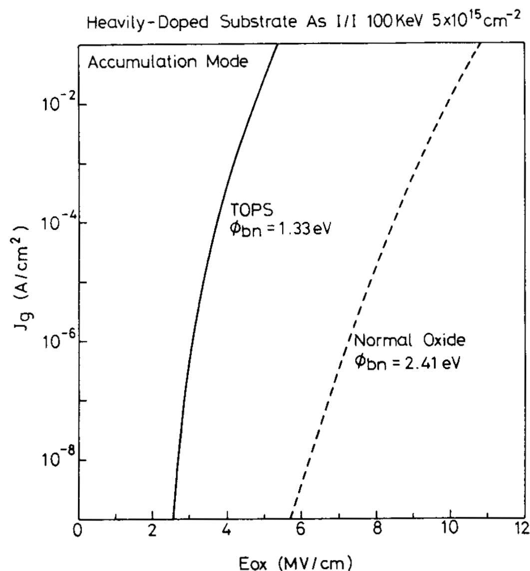

Fig. 3. The J_g–D_{ox} characteristics of TOPS (160 Å) and normal oxide (180 Å) grown on the heavily doped substrate. The measurement polarity is in accumulation mode.

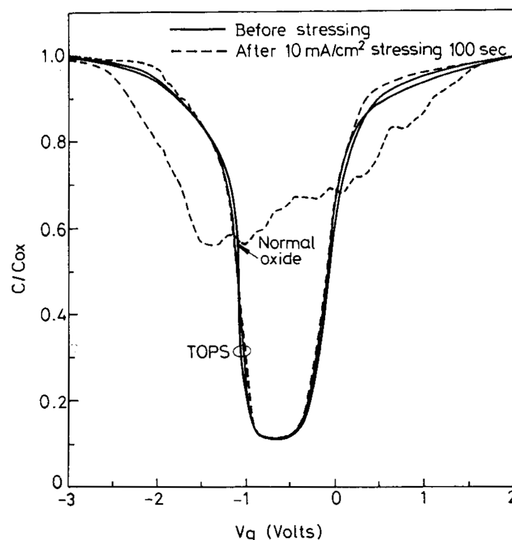

Fig. 4. The curves of the gate voltage shift (ΔV_g) versus the stressing time for TOPS and normal oxide under a constant current stressing of 1 mA/cm² for 5000 s.

a constant current stressing of 1 mA/cm² up to 5000 s (in accumulation mode). It is seen that both oxides exhibit an electron trapping behavior, however, the TOPS exhibits a ΔV_g of 4 times lower than that of the normal oxide. This implies that TOPS has a better immunity to the electron trapping under a high-field operation. This may be because for the TOPS, a lower bulk electric field existed which consequently generated less electron–hole pairs as compared to the normal oxide [3]. This lower bulk electric

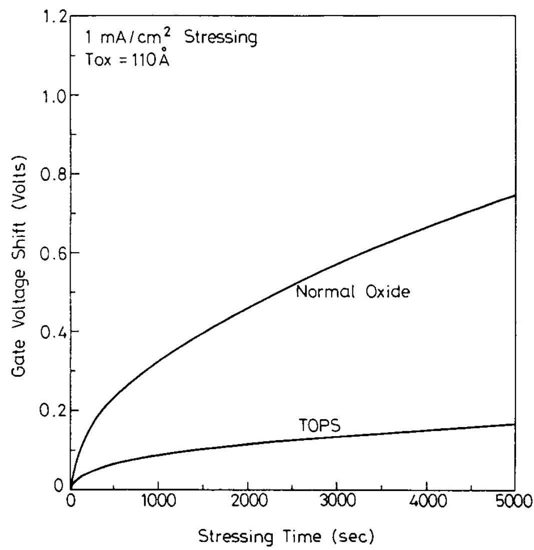

Fig. 5. The quasi-static *CV* characteristics of TOPS and normal oxide before and after 10-mA/cm^2 stressing for 100 s.

field further increases the stressing endurance of TOPS. Fig. 5 shows the quasi-static *CV* (QSCV) characteristics of TOPS and normal oxide before and after a constant current of 10-mA/cm^2 stressing for 100 s. For the TOPS, there is no significant degradation in the QSCV curve after stressing.

IV. Conclusion

The TOPS tunnel oxide presented in this letter is very simple to fabricate and offers a much higher electron conduction efficiency, smaller electron trapping rate, and less associated interface state generation.

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