New CMOS 2 V low-power IF fully differential Rm-C bandpass amplifier for RF wireless receivers

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Abstract: A new CMOS fully differential bandpass amplifier (BPA) based on the structure of a transresistance (Rm) amplifier and capacitor is proposed and analysed. In this design, the Rm amplifier is realised by a simple inverter with tunable shunt–shunt feedback MOS resistor and tunable negative resistance realised by crosscoupled MOS transistors in parallel with a current source. The capacitor is in series with the input of the Rm amplifier, which realises the filter function and blocks the DC voltage. Under a 2 V supply voltage, the post-tuning capability of the gain can be as high as 55 dB whereas the tunable frequency range is 41–178 MHz. The power consumption is 14 mW and the dynamic range (DR) is 50 dB. The differential-mode gain is 20 dB and the common-mode gain is −25 dB so that the CMRR is 45 dB. Simple structure, good frequency response and low power dissipation make the proposed bandpass amplifier quite feasible for application in the IF stage of RF receivers.

1 Introduction

A typical block diagram of the RF front-end circuit in wireless receivers is shown in Fig. 1. The circuit consists of a duplexer, a low noise amplifier (LNA), an intermediate frequency bandpass filter (IF BPF), a series of cascaded IF amplifiers and two downconversion mixers with associated local oscillators (LO). In CMOS design, both IF BPF and IF amplifiers can be combined together to form the IF bandpass amplifier (BPA) so that the function of the filter, amplifier and AGC can be realised efficiently with low power and small chip areas.

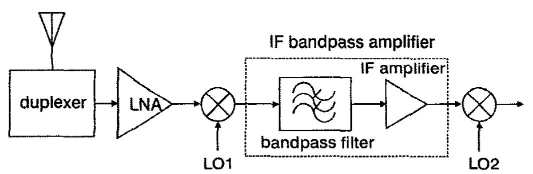

Fig. 1 *Typical block diagram of RF front-end circuit in wireless receivers*

In conventional mobile communication systems, the surface acoustic wave (SAW) bandpass filters play a key role because of their flat passband, sharp stopband rejection and high reliability features in the predominant applications of cellular telephones and radio paging. Generally, at very high frequencies (VHF), these SAW devices can be used as the IF filters for cellular telephones, whose frequencies vary from 45 MHz to more than 200 MHz. For pager applications, the SAW bandpass filters with narrow flat bandwidths are operated at frequencies 138–174 MHz. However, one major problem with these passive SAW devices is that they generally have high insertion loss. Therefore, new design techniques for SAW filters have been proposed to reduce the insertion loss drastically and to meet the specifications of mobile communication systems [1].

As well as the SAW filters, several single-chip pager receivers [2, 3] and a monolithic filter [4, 5] for applications in mobile communication systems have been implemented using the bipolar, silicon bipolar, GaAs and BiCMOS RFIC process technologies which are well suited to this market. In CMOS technology, there have been few impressive monolithic filters proposed so far, although much effort has been devoted to the research of RF components in CMOS technology.

In recent years, most IF BPFs have been designed with transconductance-C (Gm-C) filters in CMOS technology [6–10]. The basic element in Gm-C filters is the integrator formed by an open-loop transconductance element with a capacitive load. So, the main difficulty in designing Gm-C filters for 60–200 MHz IF applications is the high sensitivity to output parasitic capacitance and significant power dissipation. Moreover, many cascaded filter stages are required to achieve the specified sideband rejection in RF receivers. Thus Gm-C filters are not suitable for the design of IF BPAs for CMOS low-power RF receivers.

In this paper, a new circuit structure of a 2 V CMOS IF BPA based on the Rm-C differentiator [11] is proposed and analysed. In this structure, a simple CMOS inverter-based Rm amplifier is connected with a capacitor to form an Rm-C biquad filter and a simple Q-enhancement circuit is incorporated to adjust the filter operating frequency and gain. Thus filtering, amplifier and AGC functions can be realised in compact circuits. The proposed IF BPA has advantageous features of high sideband rejection, high gain and high linearity with the centre frequency around 100 MHz.

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2 Circuit structure

The basic element of the proposed Rm-C BPA is illustrated in Fig. 2 where the capacitor C_d is connected in series with the input of the Rm amplifier. It is called the Rm-C differentiator because the low-frequency transfer function V_O/V_I is equal to SC_dR_m. To realise the Rm amplifier for high-frequency applications, a simple NMOS inverter with shunt–shunt feedback resistance and current–source load is proposed [11] as shown in Fig. 3. In Fig. 3, the PMOS transistor M_{q1} biased by the gate voltage V_Q is the current source as the inverter load. The feedback resistance is implemented by the NMOS transistor M_{NF} biased by the gate voltage V_{CN} in parallel with the PMOS transistor M_{PF} biased by the gate voltage V_{CP}. The crosscoupled PMOS transistors M_{P1} and M_{P2} are used to provide a negative resistance to the output node V_O. Thus the filter Q value can be increased. Since M_{P1} is connected in parallel with M_{q1}, the negative resistance can be adjusted by the gate voltage V_Q of M_{q1}. Generally, the smaller the V_Q value, the larger the current of the inverter, and then the larger the magnitude of the gain.

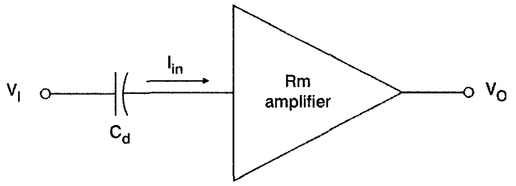

Fig. 2 *Basic element of proposed Rm-C filter*

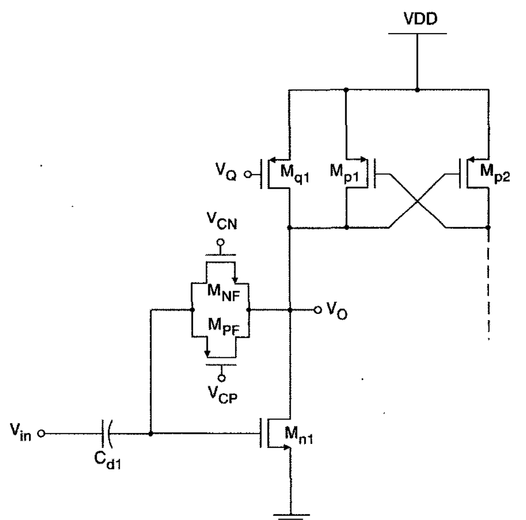

Fig. 3 *Inverter-based Rm-C bandpass amplifier*

By using small-signal analysis, the midband transresistance of the inverter-based R_m amplifier can be expressed as

$$R_m \cong \left(1 - \frac{g_{mi}}{g_f}\right) \frac{1}{g_{mi}(g_d - g_n)} \tag{1}$$

where $g_{mi} = g_{mn1}$ is the transconductance of M_{n1}, g_f is the feedback conductance, g_n is the magnitude of the negative resistance, and $g_d = g_{dn1} + g_{dq1}$ is the total output conductance which is the sum of output conductances g_{dn1} and g_{dq1} of M_{n1} and M_{q1}, respectively.

In the shunt–shunt feedback resistance r_f realised by M_{NF} and M_{PF}, the source–drain voltage is zero and both MOS devices are operated in the triode region. By using the equation of drain current, the resistance r_f can be derived as

$$r_f^{-1} = \left(r_n \| r_p\right)^{-1} = \beta\left(V_{CN} - V_{CP} - V_{tn} - |V_{tp}|\right) \tag{2}$$

where

$$\beta = \mu_n C_{ox}\left(\frac{W_n}{L_n}\right) = \mu_p C_{ox}\left(\frac{W_p}{L_p}\right)$$

is satisfied by designing a suitable dimension ratio $(W_n/L_n)/(W_p/L_p)$. V_{tn} (V_{tp}) is the threshold voltage of the NMOS (PMOS) device, μ_n (μ_p) is the electron (hole) mobility, C_{ox} is the oxide capacitance per unit area and W_n (W_p) and L_n (L_p) are the channel width and channel length of the NMOS (PMOS) device. As seen from eqn. 2, r_f is a voltage-controlled resistor with a resistance value dependent on the control voltages V_{CN} and V_{CP}. Since the dependence of V_{CN} and V_{CP} on r_f is linear in eqn. 2, the resistance tuning through V_{CN} and V_{CP} can be performed easily.

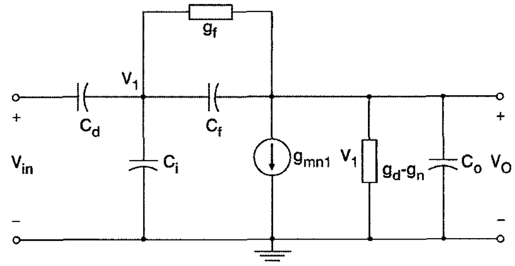

Fig. 4 *Simplified small-signal equivalent circuit of Rm-C bandpass amplifier in Fig. 3*

Considering the intrinsic capacitance of the MOS transistors as filter elements, the basic Rm-C differentiator in Fig. 3 can be regarded as a biquadratic BPF. The small-signal equivalent circuit of Fig. 3 is depicted in Fig. 4, where C_o is the total output capacitance including the capacitance of the MOS transistors and the external capacitance loading C_L, C_i is the input capacitance at the gate of M_{n1}, and C_f is the capacitance between the output node and the input node of M_{n1}. The transfer function can be expressed as

$$H(s) = \frac{V_o}{V_{in}} \cong \frac{sC_dD}{(As^2 + Bs + C)} \tag{3}$$

where

$$A \equiv (C_d + C_i)(C_f + C_o) + C_fC_o \tag{4}$$

$$B \equiv g_{mn1}C_f + (g_d - g_n)(C_d + C_i + C_f) + g_f(C_d + C_i + C_o) \tag{5}$$

$$C \equiv (g_{mn1} + g_d - g_n)g_f \tag{6}$$

$$D \equiv -(g_{mn1} - g_f) + sC_f \tag{7}$$

$$C_i \equiv C_{gsn1} + C_{gbn1} + C_{gdnf} + C_{dbnf} + C_{gspf} + C_{sbpf} \tag{8}$$

$$C_o \equiv C_{dbn1} + C_{dbp1} + C_{gsnf} + C_{gdpf} + C_{sbnf} + C_{dbpf} + C_L \tag{9}$$

$$C_f \equiv C_{gdn1} \tag{10}$$

$$g_d \equiv g_{dn1} + g_{dp1} \tag{11}$$

From eqns. 7 and 10, it can be seen that C_f is very small so that SC_f is much smaller than $g_{mn1} - g_f$. Thus SC_f in D can be neglected. This means that D is a constant and $H(S)$ in eqn. 3 can be approximated as the transfer function of a biquadratic bandpass filter.

According to eqn. 3 with constant D, the centre frequency w_O and the quality factor Q of the VHF biquad can be expressed as

$$w_o = \sqrt{\frac{C}{A}} = \sqrt{\frac{(g_{mn1} + g_d - g_n)g_f}{(C_d + C_i)(C_f + C_o) + C_f C_o}} \quad (12)$$

$$Q = \frac{\sqrt{AC}}{B} = \frac{\sqrt{[(C_d+C_i)(C_f+C_o)+C_f C_o](g_{mn1} + g_d - g_n)g_f}}{g_{mn1}C_f + (C_d+C_i+C_f)(g_d-g_n) + (C_d+C_i+C_o)g_f} \quad (13)$$

As mentioned before, g_f is tunable by the voltages V_{CN} and V_{CP}, whereas g_n is tunable by V_Q. It can be seen from eqns. 12 and 13 that the changes of g_f and g_n lead to the change of w_o and Q. Although g_n or V_Q has a stronger effect on Q and g_f or V_{CN} (V_{CP}) on w_o, both Q and w_O are changed with g_n and g_f. Thus iterative tuning is required to obtain the desired Q and w_o. If process variations are small from run to run, V_{CN} (V_{CP}) and V_Q may be on-chip generated and the resultant errors on Q and w_o are still tolerable.

With the basic circuit of Fig. 3, the fully differential IF Rm-C biquadratic bandpass amplifier (BPA) can be designed as shown in Fig. 5. It has a simple structure to retain high-frequency response. Moreover, the crosscoupled PMOS transistors can be compactly merged. They can provide the required negative resistance to both output nodes. Besides, they can also suppress the common-mode gain of the differential BPA to raise its common-mode rejection ratio (CMRR).

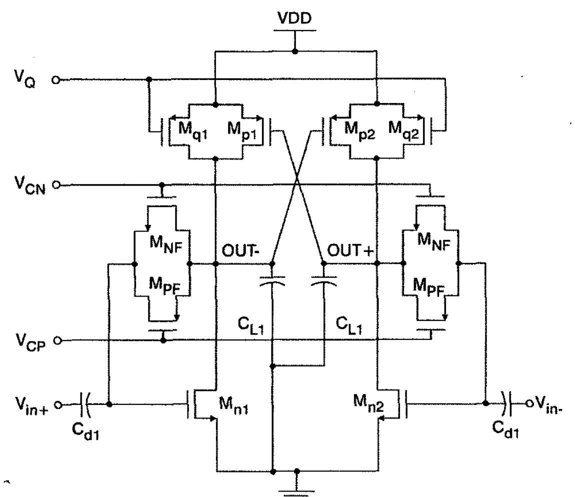

Fig. 5 *Circuit diagram of fully differential Rm-C IF biquadratic BPA*

The required BPA for RF receiver applications is of about six orders. This can be realised by directly cascading three stages of the biquadratic BPAs in Fig. 5 with V_Q in the three stages connected together and similarly V_{CN} and V_{CP}. Owing to the input capacitance C_d, the DC voltage in one stage is blocked to the next stage. Thus, the problem of the DC voltage among stages can be avoided without adding any extra element.

3 Stable conditions

Fig. 3 shows the implementation of negative resistance directly using a positive feedback circuit which is composed of two identical PMOS transistors crosscoupled to each other. The purpose of these extra positive feedback circuits is to generate a higher gain value. The positive feedback circuit will create a negative conductance

$$g_n = -r_n^{-1} = \frac{g_{mp}^2}{g_{dp}}$$

where g_{mp} is the transconductance of M_p and g_{dp} is the load conductance seen from the load terminal. The total output conductance g_t is now the parallel combination of g_o and g_n, i.e. $g_t = g_o - g_n$. By designing the relative sizes such that the negative conductance will cancel most of the positive conductance at the output stage, a higher impedance and consequently high Q can be achieved.

If g_t is negative, the Q-factor and the gain of the BPF increase. However, the g_t value cannot be too negative. The potential problem associated with the use of positive feedback is the tendency for oscillation to occur in the circuit. It is obvious that the fully differential biquadratic Rm-C BPF has two poles and they are negative real numbers or conjugate complex numbers in the left-half plane if the circuit system is stable. Thus, the coefficients $B > 0$ and $C > 0$ in eqns. 5 and 6. That is

$$\begin{cases} |g_t| < \frac{g_m C_f + g_f (C_i + C_o)}{C_i + C_f} \\ |g_t| < g_m \end{cases} \quad (14)$$

Although the g_t value cannot be precisely quantified, eqn. 14 gives the range that has stable operation for the Rm-C BPF circuit.

4 Measured results

The proposed Rm-C IF BPA has been designed and simulated with 0.5μm double-poly–double-metal CMOS technology. After the design optimisation, component values and device dimensions of the 100MHz CMOS bandpass amplifier are listed in Table 1. All MOS devices have the minimum gate length of 0.5μm to reduce the device capacitance. The active chip area is about 635 × 960μm².

Table 1: Component values and device dimensions of IF filter

Device	1st stage			2nd stage			3rd stage		
	W, μm	L, μm	M	W, μm	L, μm	M	W, μm	L, μm	M
PMOS (mp1, mp2)	5	0.5	30	5	0.5	30	5	0.5	20
PMOS (mq1, mq2)	5	0.5	40	5	0.5	20	5	0.5	30
NMOS (mn1, mn2)	20	0.5	50	20	0.5	50	20	0.5	40
PMOS (msp1)	5	0.5	40	5	1	40	5	1	50
NMOS (msn1)	2	0.5	40	2	0.5	40	2	0.5	50
C_{d1}, C_{d2}	2pF			2pF			1pF		
C_{L1}, C_{L2}	5pF			5pF			5pF		

Fig. 6 shows the measured frequency response of the three-cascaded-stage high-gain Rm-C IF bandpass amplifier with V_{CP} = 0.1V, V_{CN} = 1.68V and V_Q = 0.57V and the supply voltage V_{DD} = 2V. The differential-mode gain is 20dB whereas the common-mode gain is –25dB so that the CMRR is 45dB. Normally the IF BPA has to be large in order to be able to perform the high-frequency mirror signal suppression with a bandpass filter with limited Q. It has out-of-band signal suppression comparable to the ideal sixth-order BPF. If the frequency of the desired signal is

80 MHz and the frequency of the mirror signal is 120 MHz, an equivalent mirror signal suppression of 20 dB can be obtained by the proposed IF BPA.

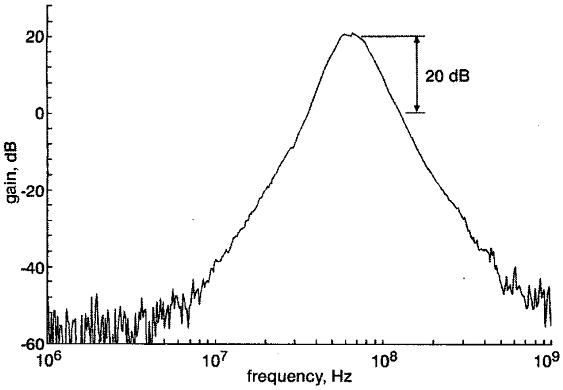

Fig. 6 *Measured frequency response of fully differential 6th-order Rm-C IF BPA*
V_{DD} = 2V, V_{CN} = 1.68 V, V_{CP} = 0.1 V, V_Q = 0.57 V

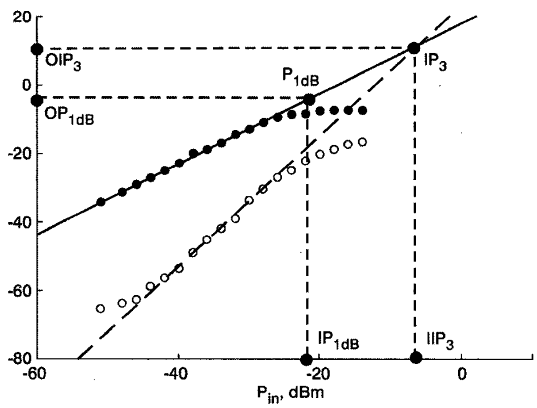

Fig. 7 *Measured I_{1dB}, OP_{1dB}, IIP_3, and OIP_3 of fully differential 6th-order Rm-C IF BPA*
● P_{o1}
○ P_{o2}
——— line 1
— — — line 2

The measured input and output 1 dB compression points IP_{1dB} and OP_{1dB} and input third-order intercept point IIP_3 are –21 dBm, –6 dBm, and –5 dBm, respectively, as shown in Fig. 7. The dynamic range DR = (IP_{1dB} – MDS) = 50 dB, since the minimum discernible signal (MDS) is –65 dBm. The bandwidth of the IF BPA is about 40 MHz. The chip power consumption is 14 mW under a 2 V power supply.

Fig. 8 shows the measured tunability of the fully differential sixth-order IF BPA with fixed V_{CP} = 0.1 V and V_{CN} = 1.75 V, and variable V_Q from 0.26 to 0.94 V. As can be seen from Fig. 8, the adjustable gain of the IF BPA is in the region of 55 dB with only a small change of centre frequency. Thus, the control voltage V_Q may be used to perform the automatic gain control (AGC). In the tuning of the IF BPA, the initial values of the controlled voltages are V_{CP} = 0.1 V, V_{CN} = 1.75 V, and V_Q = 0.57 V. After finding the optimal values, one of the controlled voltages can be kept constant while the other is adjusted to perform the fine tune. As shown in Fig. 9, the measured centre frequency of the BPA varies from 41 to 178 MHz whereas there is no gain variation in the passband. Under the condition of V_{CP} = 0.1 V, V_{CN} = 1.61 ~ 1.95 V and V_Q = 0.26 ~ 0.94 V, the tunability of the centre frequency is 137 MHz. The measured results of the fully differential sixth-order Rm-C BPA are summarised in Table 2. The layout of the IF BPA is shown in Fig. 10.

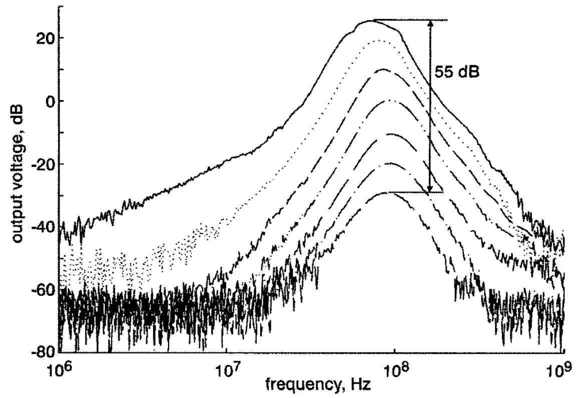

Fig. 8 *Measured frequency responses of fully differential 6th-order Rm-C BPA*
V_{CP} = 1 V, V_{CN} = 1.75 V, V_Q = 0.26~0.94 V
V_Q values:

———	0.26 V	— — —	0.74 V
··········	0.40 V	— · — ·	0.83 V
- - - -	0.52 V	— — — -	0.94 V
– · – · –	0.63 V		

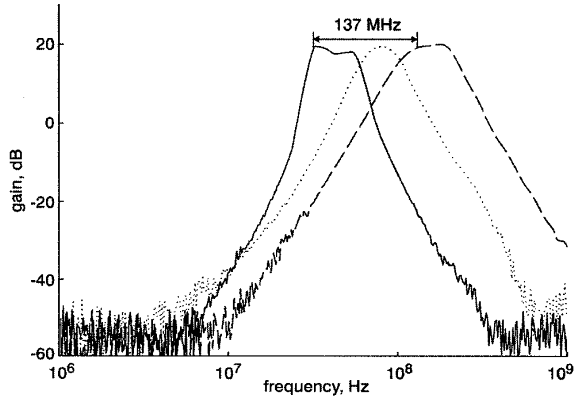

Fig. 9 *Measured frequency responses of fully differential 6th-order Rm-C BPA*
V_{DD} = 2.0 V, V_P = 1.5 V, V_{CP} = 0.1 V
——— V_{CN} = 1.61 V, V_Q = 0.87 V
·········· V_{CN} = 1.74 V, V_Q = 0.4 V
— — — V_{CN} = 1.95 V, V_Q = 0.0 V

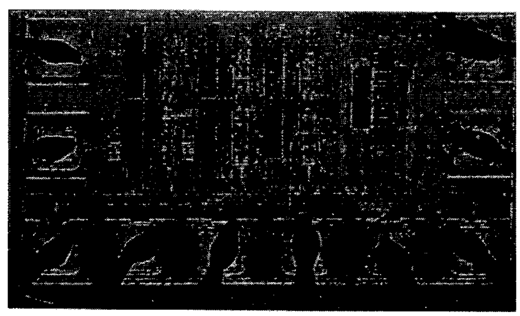

Fig. 10 *Photograph of IF BPA chip*

5 Conclusions

A new CMOS 2 V low-power fully differential Rm-C bandpass amplifier (BPA) with low power dissipation suitable for application in the IF stage of RF receivers has been successfully designed, analysed and fabricated by using

Table 2: Measured results of IF BPA

	Value	Unit
Supply voltage	2	V
Power gain S_{21}	20	dB
Centre frequency f_c	80	MHz
Noise figure	15	dB
IIP_3	−5	dBm
IP_{1dB}	−21	dBm
DR	50	dB
IR	20	dB
DC power	14	mW
Gain variation (ΔG)	55 (−25~30)	dB
f_c variation (Δf_c)	170 (30~200)	MHz

0.5 μm double-poly–double-metal CMOS technology. In this design, the voltage mode bandpass biquads are implemented by the transresistance amplifier–capacitor (Rm-C) structure. The tunable shunt–shunt feedback MOS resistor and a crosscoupled PMOS load are applied to the biquadratic filter. Thus, both centre frequency and gain of the IF BPA are fully adjustable to account for processing tolerances and drifts caused by temperature variation or changing operating conditions. The performance of the proposed Rm-C BPA has been verified through measured results on a sixth-order BPA design. Besides the above, the proposed biquad is suitable for low-power and low-voltage applications. Suitable central frequency, amplifier gain and low-power dissipation make the proposed bandpass amplifier quite feasible in the IF stage for wireless communication applications.

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