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Design on the Low-Capacitance Bond Pad for High-Frequency I/O Circuits in CMOS Technology

Ming-Dou Ker, Hsin-Chin Jiang, and Chyh-Yih Chang

***Abstract*—A new structure design of bond pad is proposed to reduce its parasitic capacitance in general CMOS processes without extra process modification. The proposed bond pad is constructed by connecting multilayer metals and inserting additional diffusion layers into the substrate below the metal layers. The metal layers except top metal layer are designed with special patterns, which have smaller area than that in the traditional bond pad. Both the additional diffusion layers and patterned metal layers are used to reduce the parasitic capacitance of bond pad. An experimental test chip has been designed and fabricated to investigate the reduction of parasitic capacitance of the bond pad. The bonding reliability tests on the fabricated bond pad, including the ball-shear and wire-pull tests, are also used to verify the bonding adhesion. The experimental results show that the proposed low-capacitance bond pad has a capacitance less than 50% of that in the traditional bond pad. The new proposed bond pads can also keep the same good bonding reliability as that of a traditional bond pad.**

***Index Terms*—Bond pad, high-speed I/O, low capacitance pad, parasitic capacitance.**

I. INTRODUCTION

The large input capacitance generated from the bond pad and input electrostatic discharge (ESD) protection devices often limit the frequency performance of high-speed integrated circuits such as the GHz RF IC [1]–[4]. The parasitic input capacitance of an I/O pad with ESD protection devices, M_{p1} and M_{n1}, is illustrated in Fig. 1(a). The traditional bond pad structure with four metal layers is shown in Fig. 1(b). The total input capacitance $(C_{\rm in})$ looking into the bond pad can be expressed as

$$C_{\rm in} = C_{\rm pad} + C_{p1} + C_{n1}, \tag{1}$$

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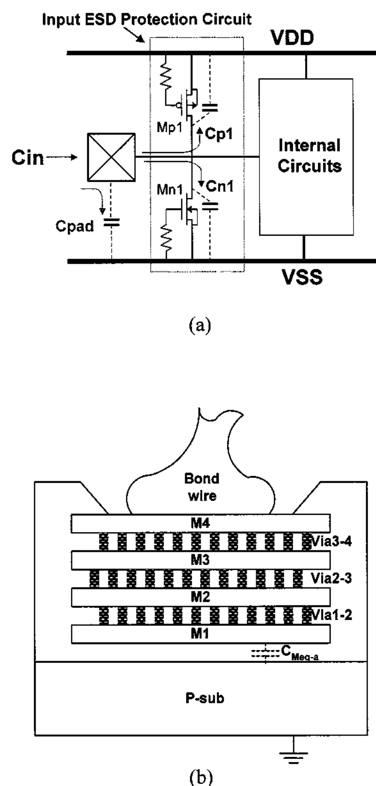

Fig. 1. Parasitic capacitance in (a) an I/O pad with ESD protection devices and (b) a traditional bond pad.

where $C_{\rm pad}$ is the parasitic capacitance of bond pad, and C_{p1} and C_{n1} are the parasitic capacitance of ESD protection devices M_{p1} and M_{n1}, respectively. Although the progress of deep-submicron CMOS technology enables the dimension of devices dramatically shrunk, the dimension of bond pad is not reduced due to the limitation of bonding machines. The area of bond pad metal overlapped with the substrate is sizable, which results in a large parasitic capacitance. Moreover, the input pad must be drawn with the on-chip ESD protection devices to protect the internal circuits against ESD damages. To sustain a desired high ESD robustness, the ESD protection devices often have larger device dimensions, which also contribute large parasitic junction capacitance (2–8 pF) to the input pad [3]. The large input capacitance limits the operating frequency of the I/O signals.

Recently, a new on-chip ESD protection circuit with a very low input capacitance for analog or RF applications had been reported [5], [6], where the ESD protection devices connected to the bond pad have a device dimension (W/L) of only 50 μm/0.5 μm but it can sustain the human-body-model (HBM) ESD level of 6 kV in a 0.35-μm CMOS process. With such small ESD protection devices, the total input junction capacitance generated from the ESD protection devices is only 0.37 pF. The layout size of the metal bond pad for wire bonding in this 0.35-μm CMOS process is specified as $96 \times 96\ \mu\text{m}^2$ for reliable bonding consideration, which contributes a parasitic capacitance of 0.67 pF. So, the total input capacitance of the analog ESD protection circuit including the bond pad is only 1.04 pF, but the bond pad contributes 64% of the total input capacitance [6]. If the bond pad capacitance can be further reduced, the total input capacitance of this analog ESD protection circuit can be significantly reduced for more high-frequency or high-speed circuit applications.

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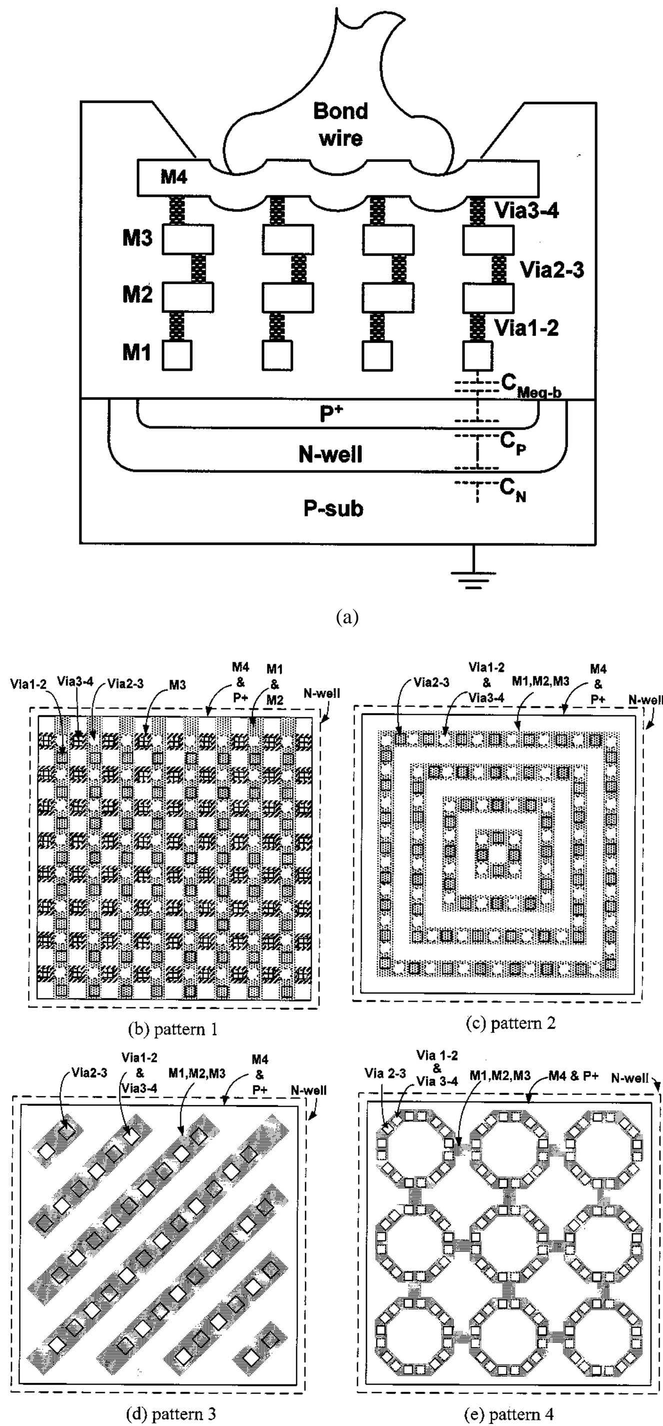

Fig. 2. (a) Cross-sectional view of the proposed bond pad. Schematic layout top views of the new proposed low-capacitance bond pads in (b) cross-bar style, (c) square-ring style, (d) slash style, and (e) octagon-ring style.

In this brief, a new bond pad structure is proposed to reduce its parasitic capacitance in general CMOS processes without extra process modification [7]. The test chips with the designed bond pad have been fabricated and measured to demonstrate the reduction of parasitic capacitance. The proposed new bond pad structure has a parasitic capacitance less than 50% of that in the traditional bond pad structure. In addition to reducing the parasitic capacitance, this new bond pad structure also provides better bonding adhesion of 10% improvement than the traditional bond pad.

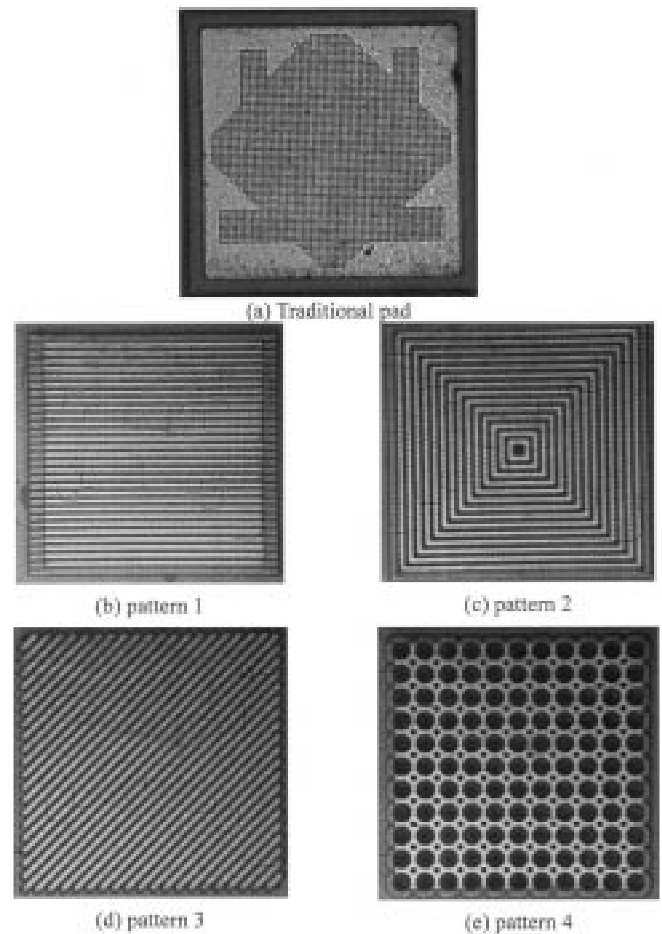

Fig. 3. Photographs of the fabricated bond pads, which are photographed without the top-layer-metal cover to show the different bond pad patterns.

II. Low-Capacitance Bond Pad

The cross sectional view of a traditional bond pad structure realized in a 0.35-μm CMOS process with four metal layers has been shown in Fig. 1(b). All metal layers (M1, M2, M3, and M4) are constructed in the same square shape. These metal layers are connected by the via plugs which are indicated as Via1-2, Via2-3, and Via3-4 in Fig. 1(b). Via1-2 is the via plug which connects the metal layers M1 and M2. Similarly, Via2-3 and Via3-4 connect the corresponding metal layers. The bond pad parasitic capacitance, $C_{\mathrm{Meq\text{-}a}}$, is contributed by the metal layer nearest to the grounded substrate. In theory, increasing the distance between the nearest parallel plate of the capacitor can reduce the bond pad parasitic capacitance. For this reason, using only top metal layer, M4, to construct the bond pad can lower the capacitance without any process modification. But, the method of using only top metal layer to construct the bond pad structure for getting lower parasitic capacitance results in the worse bonding adhesion and the peel-off phenomena [8]. The top metal layer has no connection to deeper material and only adhered to the top dielectric layer. When a bonding machine is performing the wire bond on such a bond pad, the bond pad suffers a pressing force and then a pulling force. If the bond pad does not adhere reliably to semiconductor die, the peel-off phenomena often occur [8]. To avoid the peel-off problem, several forms and materials of via plugs which connect the multimetal layers had been reported to increase the adhesion of the metal layers on the dielectric layers during wire bonding [8]–[10].

Both to reduce the parasitic capacitance and to overcome the peel-off issue, the new proposed bond pad structure is consisted

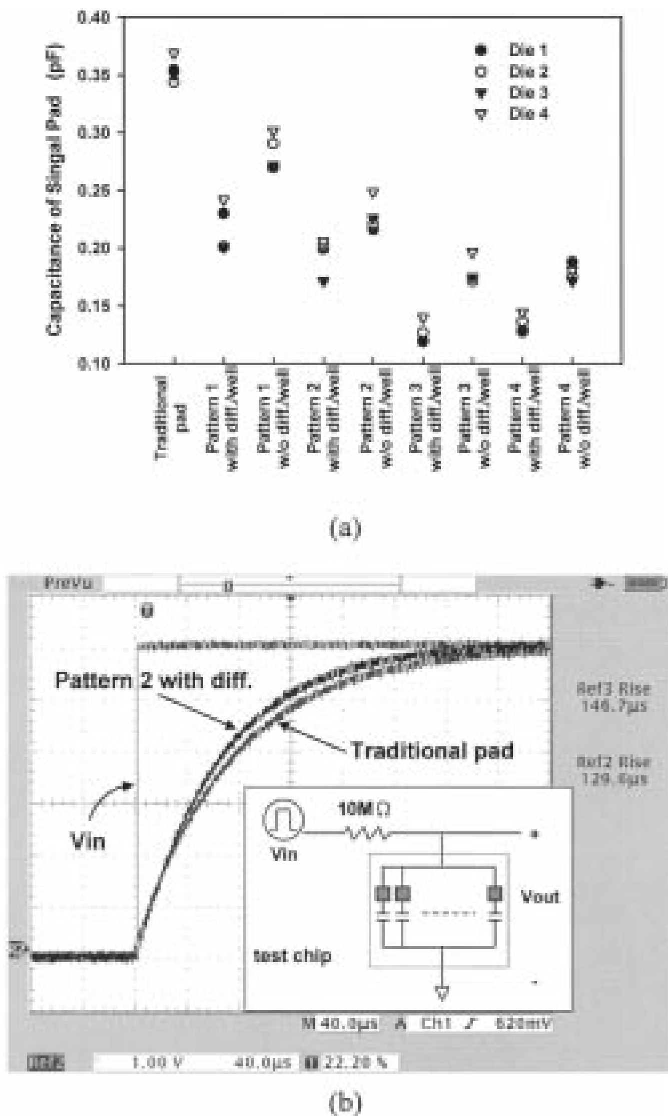

Fig. 4. Measured results on the fabricated bond pads. (a) Comparison among the capacitance of each bond pad. (b) Comparison on the step transient response between pattern 2 and the traditional bond pad.

of the connected multi-metal layers. Besides, the shape of the top metal layer is still designed with a whole plate for wire bonding, but the underlying metal layers close to the substrate are designed in broken shapes with smaller areas to reduce the overlapped area to the substrate. Fig. 2(a) shows the cross sectional view of the proposed low-capacitance bond pad in a CMOS process with four metal layers. The top metal layer, M4, is a plate to carry the bond wire. The three underlying metal layers (M3, M2, and M1) are designed in broken shapes to reduce the metal-induced parasitic capacitance, $C_{\rm Meq\text{-}b}$. Thus, this $C_{\rm Meq\text{-}b}$ is much smaller than $C_{\rm Meq\text{-}a}$ shown in Fig. 1(b). Moreover, the additional diffusion layers P+ and N-well are inserted below the multi-metal layers to form the serial junction capacitance $C_{\rm P}$ and $C_{\rm N}$ under the pad, respectively. Therefore, the total parasitic capacitance of the proposed bond pad can be expressed as

$$C_{\rm total} = \frac{1}{\frac{1}{C_{\rm Meq\text{-}b}} + \frac{1}{C_{\rm P}} + \frac{1}{C_{\rm N}}}. \tag{2}$$

Because the area of capacitor constructed by the metal layer overlapping on the substrate is reduced and the junction capacitors are inserted in serial, the proposed bond pad has a much lower parasitic capacitance than the traditional bond pad. Besides, the broken shapes of the underlying metal layers can make the surface of the top metal layer irregular to provide a better adhesion between the bond wire and the top metal layer.

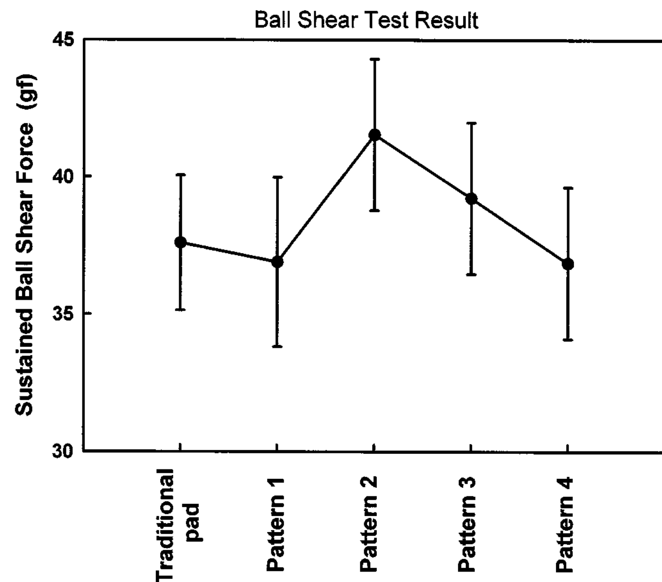

Fig. 5. Measured results of ball shear test on the fabricated bond pads.

TABLE I
WIRE PULL TEST RESULTS ON THE EXPERIMENTAL BOND PADS

	Traditional pad	pattern 1	pattern 2	pattern 3	pattern 4
Wire pull force (gf)	8.4 ± 0.8	8.4 ± 0.6	8.8 ± 0.9	9.4 ± 0.9	8.3 ± 0.4

To verify the performance of the new bond pad structure, several kinds of bond pads are designed and fabricated in a 0.35-μm 1P4M standard CMOS process. There are four different layout patterns designed for reducing the area of underlying metal layers. Fig. 2(b) shows the schematic layout view of the first designed pattern called as pattern 1. The metal layers M1 and M2 are designed as bars, which are paralleled in the column direction, when the metal layer M3 is designed as bars aligned in the row direction. Top metal layer M4, P+ and N-well diffusions are designed as whole plates without broken shapes. The via plugs are placed in the proper location where the corresponding metal layers have overlapping and different kinds of via plugs are not stacked. Fig. 2(c) shows the schematic layout view of the second designed pattern called as pattern 2. All the metal layers except top metal layer M4 were designed with the same pattern style that is a square ring. To further reduce the area of underlying metal layers, the third design pattern called as pattern 3, is designed and shown in Fig. 2(d). All the metal layers except M4 are patterned as parallel bars and arranged in slash style. The smallest area of underlying metal layers is designed in the pattern 4 and illustrated in Fig. 2(e). In the pattern 4, the metal layers except M4 are designed as connected octangle-ring style and the stacked via plugs Via1-2 and Via3-4 are alternated with Via2-3 like the pattern 2 and the pattern 3. In all patterns, the layout area of the top metal layer for wire bonding is fixed as 96 × 96 μm^2 in this study. The relation among the areas of the underlying metal layers overlapping with the substrate is traditional pad > pattern 1 > pattern 2 > pattern 3 > pattern 4. The designed bond pad having smaller areas of the underlying metal layers overlapping with the substrate should have smaller bond pad parasitic capacitance.

III. Experimental Results

To verify the performance of the designed bond pad structure, the test chip had been fabricated in a 0.35-μm 1P4M standard CMOS process. Fig. 3 shows the photographs of the fabricated bond pads in the experimental test chip, including the traditional pad shown in Fig. 3(a). In particular, to clearly see the designed patterns of pattern 1 to pattern 4, the fabricated bond pads in a test chip were striped the top metal layer off to be photographed. The photographs of the pattern 1 to pattern 4 are shown in Fig. 3(b)–(e), respectively, which are corresponding to the layout in Fig. 2(b)–(e). For each type of the bond pads, ten pads are connected together in parallel in the test chip to measure the capacitance per pad for more accuracy consideration. Fig. 4(a) compares the measured capacitance of the experimental bond pads. The capacitance of the traditional bond pad is about 0.35 pF per pad and that of the proposed bond pad is from 0.24 to 0.12 pF per pad. It can be seen that the smaller areas of the underlying metal layers give the smaller parasitic capacitance indeed, and the inserted serial junction capacitors can provide with smaller parasitic capacitance further. Comparing with the traditional pad, the parasitic capacitance of the new proposed bond pad can be reduced to only about 50% from that of the traditional bond pad. For the pattern 4 with the P+ and N-well diffusions, the parasitic capacitance per pad can be reduced to only 0.12–0.15 pF, which is only $\sim 35\%$ of that in the traditional pad.

Moreover, to verify the effect of the bond-pad parasitic capacitance on the I/O signal of integrated circuits, a step transient response measurement was performed. The circuit for step response measurement is shown in the inset figure in Fig. 4(b), where a simple RC network is used. The transient voltage waveforms are detected by a Tektronix P6139A voltage probe, which has a parasitic input capacitance of 8 pF and an input resistance of 10 MΩ. The test pads have ten same bond pads connected in parallel in the test chip to increase the measurement accuracy. Because the parasitic capacitance of each bond pad is reduced to very small, a large resistor of 10 MΩ is therefore used to distinguish the step transient response on different bond pads. The measured transient voltage waveforms between the pattern 2 and the traditional pad are compared in Fig. 4(b). With a same step input signal, the waveform of the pattern-2 bond pad with additional P+ and N-well diffusion layers has a shorter rise time of about 11.6% reduction from that of the traditional bond pad. This value includes the parasitic capacitance effect of the voltage probe, but it still has successfully verified that the new bond pad provides quicker step transient response than the traditional pad.

A practical bond pad design must be reliable enough to be used. Therefore, the reliability test was also performed to investigate bonding reliability on the fabricated bond pads. In MIL-STD-883E bondability test standard [11], ball shear test and wire pull test had been standardized. For both, ball shear test and wire pull test, there are five samples of each fabricated bond pad for testing to investigate its bonding reliability. The measurement result of the ball shear test on the fabricated bond pads is shown in Fig. 5. All the testing bond pads can sustain ball shear force greater than 30 g-force, which is the minimum industrial specification suggested by the MIL-STD-883E standard. As shown in Fig. 5, the pattern 2 and pattern 3 provide better bonding reliability than that of the traditional bond pad structure. The improvement is about 10%. In MIL-STD-883E bondability test standard, the minimum sustained wire pull force is specified as 5 gram-force. The test results of wire pull test on the fabricated bond pads are listed in Table I. All the test results are greater than the standard specification of 5 gf. Pattern 2 and pattern 3 also provide better bonding reliability than the traditional bond pad structure in the wire pull test. The failure location for all experimental pads under the wire-pull test is all of bond ball neck broken which results in the maximum adhesion between the pad and wire ball not able to obtain. But, at least, it has proven that no peel-off problem occurs on the proposed bond pads in the test chip under such wire pull test.

IV. Conclusion

By using broken shape metal layer and additional diffusion layers, a low-capacitance bond pad structure has been designed and experimentally verified. The broken shape metal layer reduces the overlapped area to the substrate, therefore to reduce the parasitic capacitance. The additional diffusion layers inserted under the pad generate the capacitor connected in serial to further reduce the total parasitic capacitance of the bond pad. From the measurement results, it has confirmed that the proposed design on the bond pads provides a low cost solution for reducing parasitic capacitance on the I/O pads of chips, whereas the bonding reliability can be still maintained good enough. The proposed bond pad design is achieved by only layout pattern modifications on the metal layers of the bond pad, therefore this design is fully process-compatible to general CMOS processes. With a significantly reduced parasitic capacitance, the proposed bond pads can be widely used in high-frequency or GHz integrated circuits to improve frequency response.

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