Novel Technique for SiO_2 Formed by Liquid-Phase Deposition for Low-Temperature Processed Polysilicon TFT

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***Abstract*—A novel technique for SiO_2 formation by liquid-phase deposition (LPD) at nearly room temperature for low-temperature processed (LTP) polysilicon thin-film transistor (poly-Si TFT) was developed. LPD-SiO_2 film with a lower P-etch rate shows its dense structure. LPD-SiO_2 also exhibits good electrical characteristics. LTP poly-Si TFT's with LPD-SiO_2 as gate insulator have been fabricated and investigated. Their characteristics exhibit sufficient performance for pixel transistor in liquid crystal display (LCD).**

I. Introduction

Low-temperature deposited silicon dioxide (SiO_2) film as gate insulator is a key issue in polysilicon thin-film transistor (poly-Si TFT) for liquid crystal display (LCD) [1]. Traditionally, chemical vapor deposition (CVD) methods were used to fabricate such a film [2], [3]. But all of these methods need expensive equipment and the processes are complex. Considering that the future large-area LCD will be expected to be realized on low melting-point glass substrate [4], an economical and low-temperature SiO_2 formation technology is required. Recently, a new SiO_2 formation technology using liquid phase deposition (LPD) method was developed [5]. The technology is easy to operate at low temperature, and the apparatus required is inexpensive and simple. In this paper, the properties of LPD SiO_2 film are discussed. And the characteristics of low-temperature processed (LTP) poly-Si TFT with LPD SiO_2 gate insulator are also presented.

II. Experimental

As an immersing solution, H_2SiF_6 solution (2 M) saturated with silica was used. To make a supersaturated state with SiO_2 in the immersing solution, boric acid solution (0.5 M) was continuously added. The basic reaction kinetics of deposition were represented by two equilibrium processes as shown in the inset of Fig. 1. In equilibrium (1), addition of silica leads to a shift of reaction from right to left. Therefore, the solution saturated with silica may include minimum hydrofluoric acid. However, this equilibrium may be changed by adding boric acid to the solution. Normally boric acid easily reacts with hydrofluoric acid as shown in equilibrium (2) and leads to a consumption of hydrofluoric acid, and accordingly brings about a transient state supersaturated with SiO_2 in equilibrium (1). Such supersaturation of SiO_2 enhances equilibrium (1) from left to right followed by silica deposition on the substrate.

The n-type (100) silicon substrates with 4–7-$\Omega \cdot$cm resistivity were used in our experiment. The various SiO_2 films deposited at different temperature were prepared to compare the deposition rate. The deposition time of all the samples is one hour. For characterizing the SiO_2 films, the thickness and the refractive index were measured by ellipsometer. The chemical composition was analyzed by FTIR. Etching rate was examined with P-etch solution (48% HF:70% HNO_3:H_2O = 3:2:60) at room temperature. The investigation of electrical properties was made on MOS capacitor with aluminum gate contact of 0.12 mm^2 in area. The density of interface trap states is determined by high-frequency (1 MHz) capacitance–voltage measurements. The cross-sectional view of fabricated LTP ($\leq$ 620°C) poly-Si TFT with LPD SiO_2 as gate insulator is shown in the inset of Fig. 3.

III. Results and Discussions

Fig. 1 shows the FTIR spectra of deposited LPD SiO_2 film. It indicates that the intensive peaks at around 1090 and 930 cm^{-1} are due to the stretching vibrations of the Si–O–Si bond and Si–F bond, respectively. From the richness of the Si–O–Si bond, we can see that the film has a more orderly silica network and consequently more chemical stability. At the same time, the FTIR spectra shows that there is no IR absorption peak at 3600 cm^{-1}, which is the OH bond stretching mode. That is, there is no water absorption in the LPD SiO_2 film even in the as-deposited film. Because this aspect is very important for the electrical and structural stability of the film, we conclude that the quality of LPD SiO_2 film is good.

In Fig. 2, we found that the film thickness and the P-etch rate became larger as the deposition temperature

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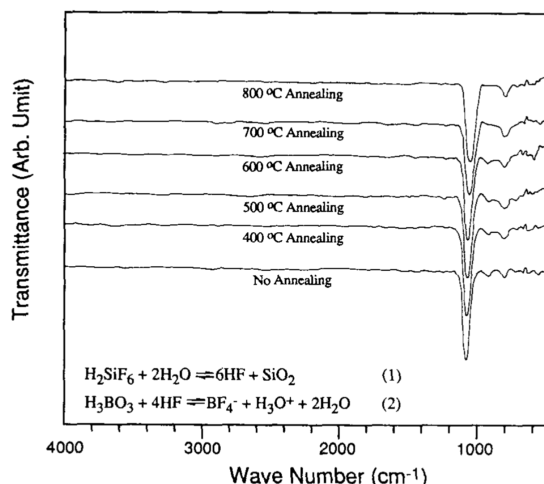

Fig. 1. FTIR spectra of 0.1-μm-thick LPD SiO_2 film with various annealing temperature for 1 h. The insert shows the reaction equations of LPD SiO_2 formation.

TABLE I
THE PROPERTIES AND TFT CHARACTERISTICS OF LPD-SiO_2 AND CVD-SiO_2

	LPD-SiO_2	CVD-SiO_2
FTIR Si-O-Si Peak	1092.5 cm^{-1}	1070 cm^{-1}
Refractive Index	1.43	1.45
P-etch Rate	24 A/sec	25A/sec
Leakage Current Density (at 5V)	2.2×10^{-12} A/cm^2	9.0×10^{-12} A/cm^2
Dielectric Breakdown Field	7 MV/cm	5.8 MV/cm
Dielectric Constant (1MHz)	3.5	4.3
Field Effect Mobility	15	35
Threshold Voltage	5.6	8.3
ON-OFF Current Ratio (Log)	6 (V_D = 5V)	5.6 (V_D = 40V)

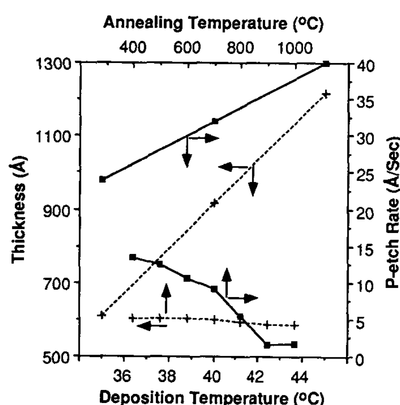

Fig. 2. The thickness and P-etch rate of LPD-SiO_2 for different deposition temperature and annealing temperature, respectively.

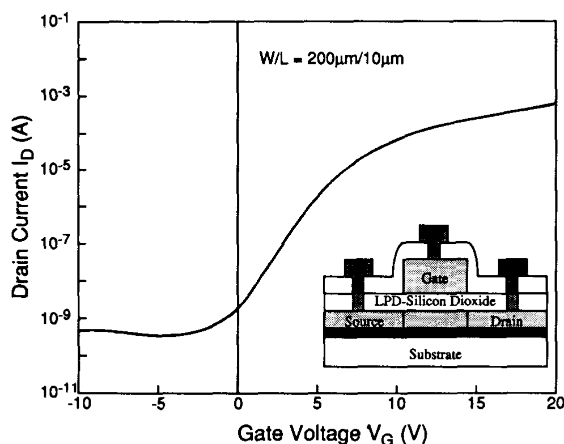

Fig. 3. I_D–V_G characteristics of LTP poly-TFT with LPD SiO_2 as gate insulator. The insert shows the cross-sectional view of fabricated device. (The thicknesses of poly-Si active layer and gate insulator are both 0.1 μm. Phosphorus ion concentration of source and drain is 1×10^{15} cm^{-2}. Hydrogenation was performed at plasma reactor in 300°C for 60 min.)

increased. It reveals that the film grown at higher temperature seems less dense. But after annealing, the LPD SiO_2 film became denser. This phenomenon as shown in Fig. 1 is attributed to the reduction in Si–F bonds. The Si–F bonds may be altered to Si–O–Si ones, because the Si–O stretching mode near 1090 cm^{-1} is shifted to a lower wave number and the half-width of the peak is increased. The decrease of P-etch rate and film thickness also reveals that the film indeed becomes more dense through annealing.

The experimental results of electrical characteristics of I–V and CV are summarized in Table I. It also shows the comparison between LPD SiO_2 and CVD SiO_2 [2]. From this table, we can conclude that the LPD SiO_2 film exhibits satisfactory electrical integrity.

The I–V characteristic of poly-TFT with LPD SiO_2 as gate insulator is shown in Fig. 3. The on–off current ratio is 10^6 at $V_D = 5$ V, the field-effect mobility is 15 $cm^2/V \cdot s$ at $V_D = 0.1$ V, the threshold voltage is 5.6 V, and the subthreshold swing is 1.6 V/decade. Comparing with the electrical behavior of another LTP device [3], also as shown in Table I, we found that the device with LPD SiO_2 exhibited better performance except that the mobility of LPD SiO_2 poly-TFT is lower than the similar values reported in [3]. The reason is, according to the discussions of [3], that the device structure with two-layer gate oxide (APCVD SiO_2 + photo-CVD SiO_2) can keep the interface cleaner and make hydrogenation more effective. The cleanness of interface decreases the surface charge density, and then increases the mobility of the device. The surface charge density of LPD SiO_2 is 1.5×10^{11} cm^{-2},

but that of photo-CVD SiO_2 is 9×10^{10} cm^{-2}. The higher surface charge density of LPD SiO_2 may be the reason why the mobility of LPD SiO_2 poly-TFT is lower than the similar values reported in [3].

IV. Summary

The physical, chemical, and electrical properties have shown that LPD-SiO_2 is similar to that grown by CVD methods. The performances of LTP poly-Si TFT's with LPD-SiO_2 applied to the gate insulator reveal that the technology of LPD-SiO_2 is feasible to economically supply excellent dielectric layer, and will be a promising candidate to replace the traditional CVD methods.

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