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Characterization and reliability of low dielectric constant fluorosilicate glass and silicon rich oxide process for deep sub-micron device application

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Abstract

Fluorosilicate Glass (FSG) with low dielectric constant currently has been replaced as an alternative to SiO_2 for device speed improvement. However, several integration aspects, such as Fluorine (F) distribution, F thermal stability, gap fill capability, capacitance reduction and via resistance of FSG prepared by the high density plasma (HDP) chemical vapor deposition (CVD) method are of concern for sub-0.18-μm devices. In this study, HDP–FSG films show different F concentrations at different locations on an 8-inch wafer. In addition, the FSG film shows poor thermal stability and F diffuses out of the film after high temperature annealing and the pressure cook test (PCT). However, the thermal stability of FSG film can be improved by capping with an oxide layer. The results indicate that silicon rich oxide (SRO) has a better effect at blocking the F diffusion out of FSG films at high temperature than plasma enhanced oxide (PE-OX). For the gap fill capability, HDP-FSG can fill all 0.23-μm gaps and some of the 0.21-μm gaps with an aspect ratio <3.8 but not the 0.19-μm gaps. A 8000 Å HDP–FSG film with 600 Å USG liner and 2000 Å cap layer shows approximately 7.5 to 7.7% capacitance reduction on 0.23/0.23-μm gaps when compared with USG (undoped silicate glass). In addition, FSG has a larger capacitance reduction on the wider metal lines than the thinner metal lines at the same gap size due to a capacitance fringe effect. The via resistance for 0.26 μm unlanded via (which allow minor photo mis-alignment) of HDP-FSG film is also similar to that of USG. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: High density plasma (HDP); Fluorosilicate glass (FSG); Reliability; Gap fill; Capacitance; Via resistance

1. Introduction

When the minimum geometry in the integrated circuits (ICs) continues to shrink, the most challenging tasks in the interconnects are using new materials such as low *K* and low *R* materials to reduce the RC delay [1]. With the reduction in capacitance, the signal propagation speed in the devices will be increased and the device will achieve a better performance. To adapt to these changes, Cu has been well accepted as the new low *R* material to replace Al/Cu alloy for metal interconnects in the semiconductor industry. Regarding the low *K* materials, there are various candidates such as FSG, hydrogen silsesquioxane (HSQ), flare, poly(arylene ether) (PAE) and benzocyclobutene (BCB) [2]. However, it is very hard for a low *K* material to fulfill all the requirements [2]. Since high density plasma undoped silicate glass (HDP-USG) or sub-atmosphere-chemical vapor deposition (SACVD) have been used for the dielectric layers for 0.25-μm devices, it would be easier to implement low-dielectric-constant (low-*K*) CVD dielectric, such as FSG with dielectric constant lower than SiO_2, for sub-0.18-μm devices. Because of these reasons, many research and development groups

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have investigated the feasibility of using fluorosilicate glass (FSG) in the sub-0.18-μm processes. However, there are several integration issues related to the device reliability that need to be considered before implementing FSG in sub-0.18-μm processes. Therefore, the uniformity of F distribution, F stability under high temperature and humid environment, gap fill capability, line-to-line capacitance reduction and via resistance were investigated.

2. Experimental

FSG films were prepared using a HDP-CVD system with gas sources of SiF_4, SiH_4, O_2 and Ar. The pressure of the system is 5 mtorr. The flowrates of the gases are Ar 50, O_2 150, SiH_4 38, SiF_4 57 sccm, respectively. The USG film was also deposited in the same system with the gas source of SiH_4 and O_2. The substrate temperature was set at 420°C. The film thickness and refractive index of FSG films were measured using an ellipsometer. The Si–F peak and F percentage were monitored by Fourier infrared spectroscopy (FTIR) and secondary ion mass spectroscopy (SIMS), respectively. The F% distribution was measured from the center of an 8-inch Si wafer and at 8 mm away from the edge of the wafer. The dielectric constant was measured using a Mercury Probe at 1 MHz. However, FSG films were deposited on 2000 Å USG/7000 Å Al stack structure for thermal stability study. In addition, there were two kinds of cap layers for FSG used in this study: SRO and plasma-enhanced oxide (PE-OX). The SRO and PE-OX cap layer were deposited by a plasma enhanced CVD (PECVD) system. These films were annealed at 400°C for 3 h and then tested under the pressure cook test at 100% RH, 120°C, 2 atmosphere for 2 h. 7000 Å thick Al patterns with metal width/gap of 0.23/0.23 μm, 0.21/0.21 μm, 0.19/0.19 μm was used for the gap fill study. The gap fill capability of FSG films with 4% F was verified by the cross-section scanning electron microscope (SEM). The capacitance reduction and via resistance at different metal widths and gaps were measured by using a two-layered Al metal structure deposited with 600 Å of USG liner, 8000 Å of FSG inter-layer-dielectric (ILD) layer and 2000 Å of SRO cap layer.

3. Results and discussions

3.1. F uniformity

The uniformity of F distribution in FSG films is the first integration issue we investigated. The concern for the non-uniform distribution of F is that the capacitance reduction and the device performance vary with the location of the devices on the wafer. This will lead to a wide distribution of device performance for devices processed on the same wafer, which is not practical for manufacturing.

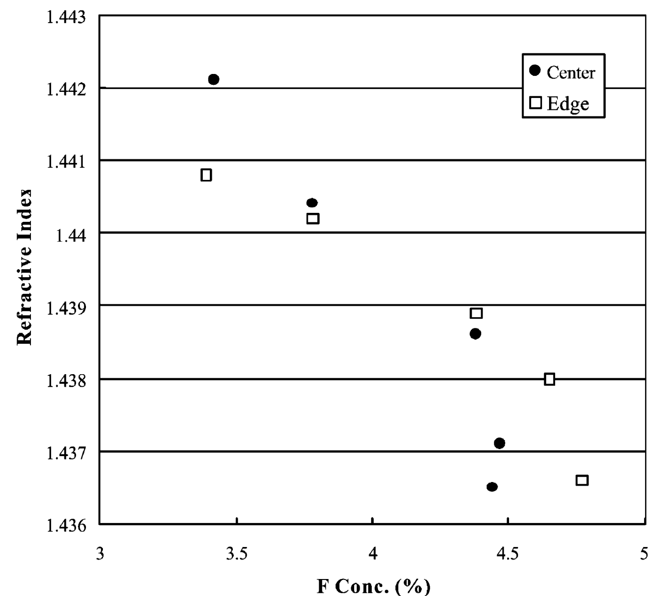

Fig. 1. The R.I. of FSG films with different F concentrations at the center and the edge of wafers.

It has been known that the introduction of F can reduce the dielectric constant of SiO_2 films [3–6]. It is because F can reduce the ionic and electronic polarizability in the oxide films by replacing the Si–O bond with Si–F or Si–O–F bonds [7]. Generally, the dielectric constant of FSG decreases by increasing the F content until it reaches the minimum and then increases by increasing the F content [6]. It has been reported that the stable FSG film can be deposited at 3–5% of F percentage with SiF_4 as the gas source [6]. At F percentage larger than approximately 4.5%, the dielectric constant of FSG film increases due to the presence of highly polar Si-O–H bonds formed when the films pick up moisture. However, the F percentage to achieve minimum dielectric constant depends on the reagents and the process conditions [3,8].

Since SiF_4, SiH_4 and O_2 were used as the reagent sources for film deposition, FSG films with 3.3–4.9% of F were deposited on Si wafers for this study. The refractive index (R.I.) and dielectric constant of FSG films with different F concentrations are shown in Figs. 1 and 2. It shows that the R.I. decreases from 1.444 to 1.436 as the F% increases from 3.3 to 4.9%. The dielectric constant also varies from 3.35 to 3.63 depending on the F% in the FSG films. All FSG films show non-uniform F% at the center and the edge locations of 8-inch Si wafers. It is found that the F% in FSG films is higher at the edge of the wafer than at the center (non-uniform F% from center to edge locations). The difference is approximately 0.2 at.% of F which represents 0.2 in dielectric constant. The higher dielectric

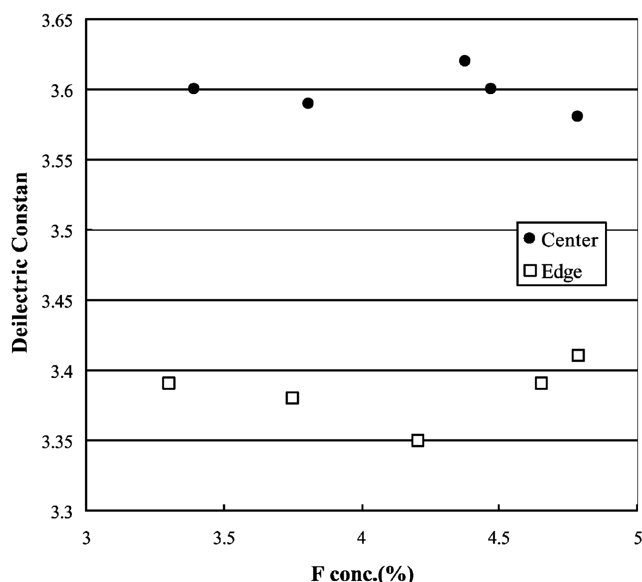

Fig. 2. The dielectric constant of FSG films with different F concentrations at the center and the edge of wafers.

constant of 3.6 at the center compares to dielectric constant of 3.4 at the edge. It may be caused by the plasma density non-uniformity across the wafer and the different distance from the SiF_4 gas inlet location. This non-uniformity in F% and dielectric constant will cause the large variations in device performance depending on its location on the wafers.

3.2. F stability

The second concern for the integration reliability of FSG film is the film stability. It has been known that FSG films are not stable if the F% is too high and as it reduces its resistance to moisture [3]. The absorbed moisture in FSG films will react with the Si–F bonds and become Si–O–H and HF. The increasing concentration of highly polarized O–H bonds will increase the dielectric constant. In addition, the HF and F diffused out of the films at high temperature will react with Al lines resulting in Al corrosion [9].

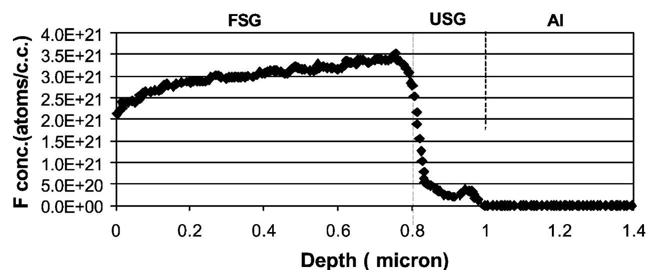

Fig. 3. The F concentration of FSG film without cap layer after PCT for 2 h and annealing at 400°C for 3 h.

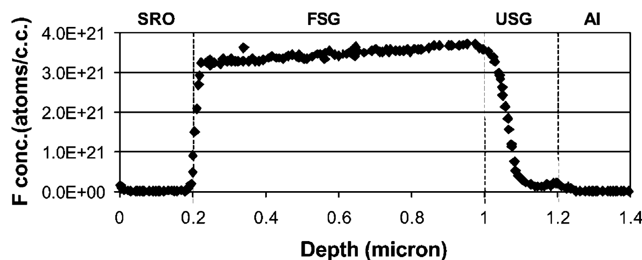

Fig. 4. The F concentration of FSG film with SRO cap layer as deposited.

The F stability in FSG film without any cap layer under PCT for 2 h and 400°C annealing for 3 h is shown in Fig. 3. The data show that the F in FSG decreases from 3×10^{21} atoms/cm^3 at the FSG/USG interface to 2×10^{21} atoms/cm^3 at FSG/air interface. It indicates that F is not stable in FSG films and diffuses out of the films after the PCT and 400°C annealing.

It has been suggested that FSG films can be capped with 200–500 Å oxide film to prevent F diffusion out of the FSG film and enhance the stability of FSG film.[10]. In addition, exposing FSG to the CMP slurry will form HF due to the F dissolving in water. This cap layer can prevent FSG from direct contact with CMP slurry. Therefore, two different cap oxide layers, SRO and PE-Oxide, were studied as the diffusion barriers for HDP–FSG.

The F concentration profiles for FSG films capped with SRO before and after PCT and 400°C annealing are shown in Figs. 4 and 5, respectively. The FSG film capped with SRO shows that the F concentration is slightly lower than that before tests in the film. It indicates that there are some F atoms depleted in FSG films. However, the F concentration is still very low before and after PCT and 400°C annealing at SRO/air interface. Instead, F concentration is slightly higher at the SRO/FSG interface after tests. This indicates that SRO layer can be a good barrier layer for F diffusion. As shown in Fig. 6, FSG film with SRO cap layer still remained stable after 48 h in ambient, PCT and annealing test. The depleted F in FSG film was accumulated at the SRO/FSG interface. For FSG films capped with

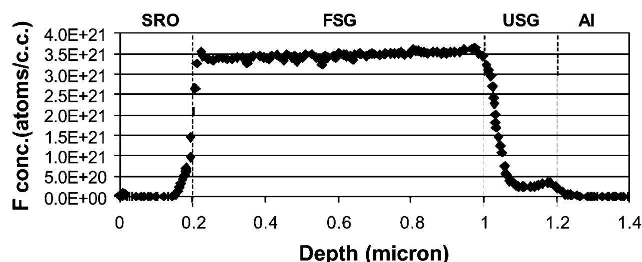

Fig. 5. The F concentration of FSG film with SRO cap layer after annealing at 400°C for 3 h.

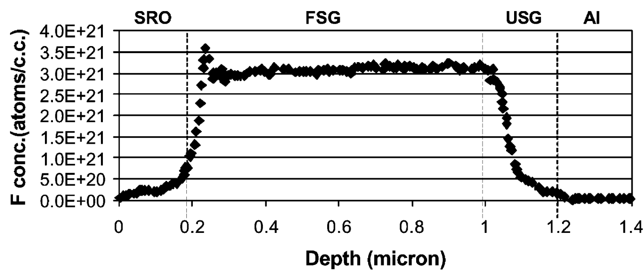

Fig. 6. The F concentration of FSG film with SRO cap layer after PCT for 2 h and annealing at 400°C for 3 h.

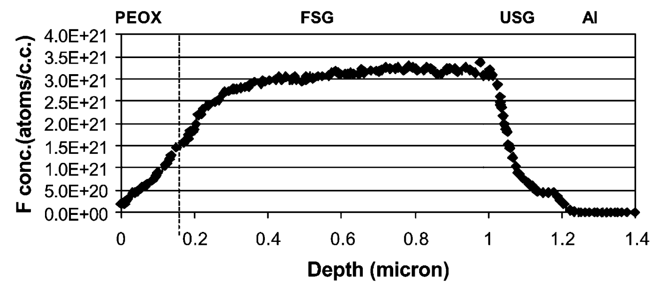

Fig. 7. The F concentration of FSG film with PEOX cap layer after PCT for 2 h and annealing at 400°C for 3 h.

PEOX, the F diffused into PEOX cap layer and generated an F concentration gradient in PEOX layer and FSG layer close the PEOX/FSG interface as shown in Fig. 7. This indicates that using PEOX as the FSG cap layer cannot block the F diffusion.

3.3. Gap fill capability

The third concern for the integration reliability of FSG is the gap fill capability. As the minimum geometry of IC devices becomes smaller and smaller, the gaps between metal lines become smaller as well. Since the film deposition rate is lower at the side wall of metal gaps than at the bottom of the gap, there is a limitation for the smallest gap that dielectric film can fill by the CVD method. If the deposition rate is too fast, it will generate voids in the gap. It has been reported that HDP–CVD can enhance the gap fill capability of USG for 0.25 μm processes due to the slower deposition rate of HDP [3]. In addition, F in SiO_2 may facilitate the deposition to fill a smaller gap. In the 0.18-μm design rule, the minimum metal gap should be close to 0.23 μm. Therefore, HDP–FSG film needs be able to fill metal gap smaller than 0.23 μm before it can be used for 0.18-μm processes.

The gap fill capability was investigated by depositing FSG films on patterned wafers with different metal width/gap: 0.23/0.23 μm, 0.21/0.21 μm and 0.19/0.19 μm. The results show that FSG films can fill all 0.23/0.23 μm patterns at the center and the edge pattern in the wafers as shown in Figs. 8 and 9. However, FSG films can fill the 0.21/0.21 μm patterns at the center but not the 0.21/0.21 μm at the edge of wafer. Especially, the gap fill is the worst for gaps in the wafer at notch area (Fig. 10). For 0.19/0.19 μm patterns, large holes were observed both in the center and the edge of wafer. It is found that the aspect ratio is approximately 3.4 at the center of wafer, approximately 3.8 at the edge of wafer and is approximately 4 for wafer notch region. Apparently, the FSG can only fill the 0.21/0.21-μm gas with aspect ratio up to approximately 3.6 and there is void generated when the aspect ratio increases to 3.8. Therefore, with the capability of filling 0.23/0.23 μm gaps, FSG can still be used for 0.18-μm processes.

3.4. The capacitance reduction and via resistance

The last concern for the reliability is the capacitance reduction and via resistance of FSG film. Since the purpose of using low K materials is to reduce the capacitance for smaller geometry, the capacitance reduction will directly effect the device performance. In addition, the via resistance for FSG film needs to be investigated to ensure that FSG can be processed without affecting the via yield. Since SRO is good diffusion barrier for F, devices with 600 Å USG/8000 Å FSG/

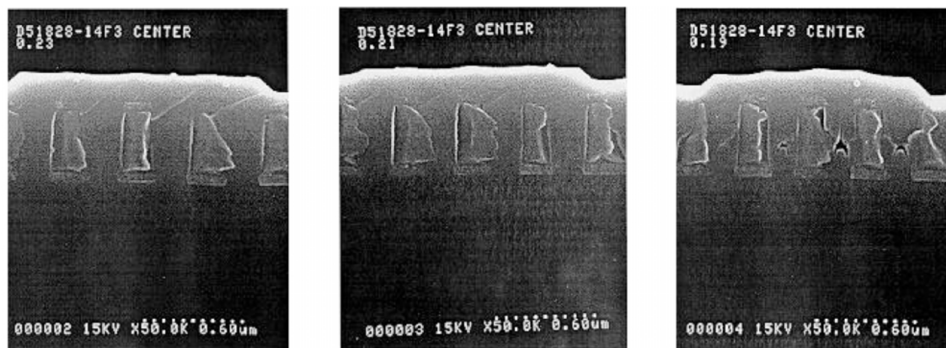

Fig. 8. Different patterns at center of the wafer.

Fig. 9. Different patterns at edge of the wafer.

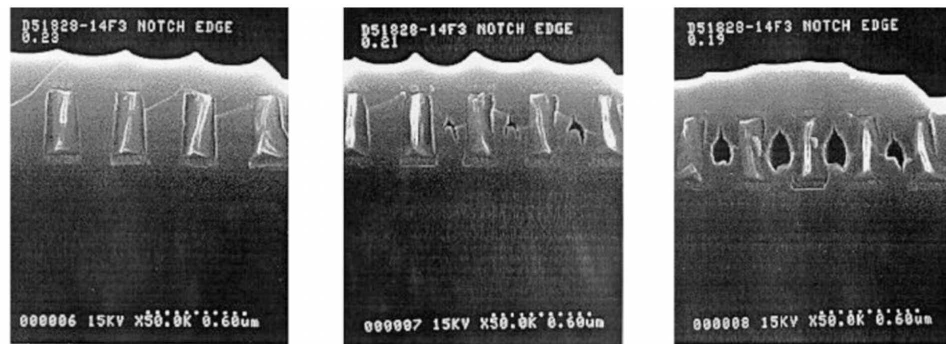

Fig. 10. Different patterns at notch of the wafer.

2000 Å SRO sandwich structures were processed for capacitance and via resistance measurement.

The line-to-line capacitance of patterns with FSG as the dielectric layer was measured at different metal widths and gaps. For the metal line-to-line capacitance, it was found that the there was approximately 7.45–7.7% reduction in capacitance for 0.23/0.23-μm patterns and approximately 6.75–7% reduction in capacitance for 0.23/0.46 μm pattern as shown in Figs. 11 and 12. In addition, the capacitance reduction also varies with the metal width as shown in Fig. 13. It shows that FSG with wider metal line has a larger impact than the thinner metal line on the line-to-line capacitance. It is believed that the larger capacitance observed at wider metal lines is due to a larger fringe capacitance between wider metal lines. The via resistance of FSG at different unlanded via mis-alignment is

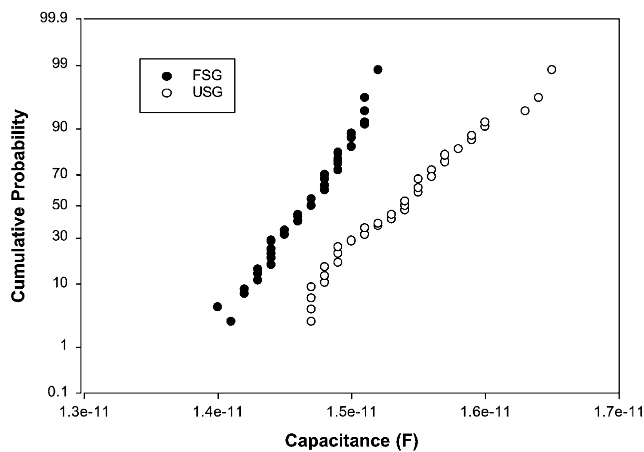

Fig. 11. Line-to-line capacitance of FSG and USG for a 0.23/0.23-μm metal structure.

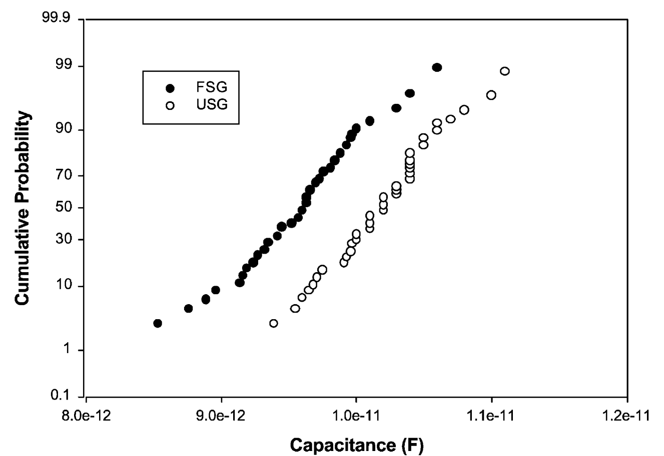

Fig. 12. Line-to-line capacitance of FSG and USG for 0.23/0.46-μm metal structure.

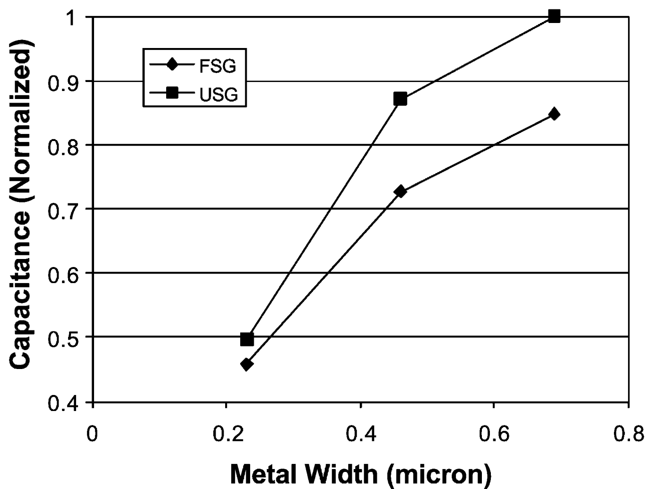

Fig. 13. Normalized line-to-line capacitance of FSG and USG for different metal structure with 0.23-μm gap.

shown in Fig. 14. It shows that the FSG has similar unlanded via resistance (which is caused by photo mis-alignment) to USG. It is consistent with the results that FSG can have similar via yield as USG.

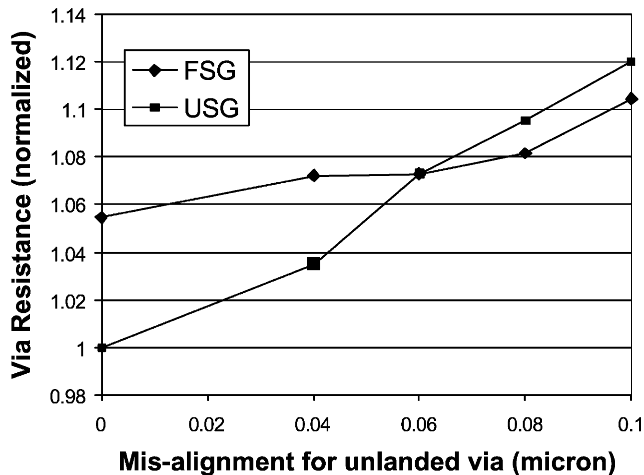

Fig. 14. Normalized via resistance of FSG and USG for different mis-alignment of 0.26 μm via.

4. Conclusions

In our study, it was found that there is approximately 0.2% F variation between the center and the edge of wafers. This non-uniform F distribution leads to the variation in dielectric constant of approximately 0.2 at the center and the edge of wafers. Because of that, the device performance will vary for devices processed on the same wafer and it will be a concern to put FSG into production. The SIMS data show that the thermal stability of FSG can be enhanced by using a cap layer and SRO is superior than PE-OX in blocking the F diffusion at high temperature and moisture environment. HDP-FSG can fill gaps as small as 0.23-μm, which indicates that FSG can be used for the 0.18-μm processes. However, it will be more difficult to use FSG in process <0.18 μm. In 600 Å USG/8000 Å FSG/2000 Å SRO cap layered structure, HDP–FSG shows 7.45 to 7.7% line-to-line capacitance reduction and has similar via resistance to that of USG film. Therefore, HDP-FSG with SRO cap layer can be used for 0.18-μm processes if the issue of the F% variation in the FSG film can be improved.

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