Characteristics of polycrystalline silicon thin-film transistors with thin oxide/nitride gate structures

Huang-Chung Cheng
Ya-Hsiang Tai
National Chiao Tung University
Department of Electronics Engineering
and
National Nano Device Laboratory
Hsinchu, Taiwan 30050

Ming-Shiann Feng
National Chiao Tung University
Institute of Materials Science and
Engineering
Hsinchu, Taiwan 30050

Jau-Jey Wang
TSMC Corporation
Hsinchu, Taiwan 30050

Abstract. Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with thin oxide/nitride (O/N) structures as gate dielectrics are fabricated. Various gate dielectrics, i.e., high-temperature thermal oxides with different thicknesses, low-pressure chemical-vapor-deposited silicon nitrides, and different combinations of O/N structures with various thicknesses, are performed to study their effects on poly-Si TFTs. The effective carrier mobility of devices with thin gate oxides is several times larger than of those with thick gate oxides. However, the breakdown voltages of thin gate oxides are too low to satisfy the requirements of TFT applications. Silicon nitrides can be substituted because of the high breakdown voltage and the smooth dielectric/poly-Si interfaces. A problem in adopting silicon nitride is the large interface stress between the silicon nitride and the poly-Si. A thin thermal pad oxide beneath the silicon nitride is therefore grown to reduce the high interface stress. Finally, the equivalent oxide thickness effect of the O/N gate structures on the electrical characteristics of TFTs is systematically investigated.

Subject terms: display technologies; polycrystalline silicon thin-film transistors.

Optical Engineering 32(8), 1798–1802 (August 1993).

1 Introduction

In recent years, thin-film transistors (TFTs) fabricated on insulating substrates have been of great interest. TFTs are used not only in 3-D integrated circuits but also in various large-area electronic systems such as switching elements and driving circuits for liquid crystal displays (LCDs). For the application of an active matrix flat-panel display, some addressing types must be chosen.[1] However, for the consideration of resolution, contrast and angle of view, color and gray-scale capabilities, and the possibility of deposition on inexpensive substrates, an LCD matrix addressed by TFTs is the best method.[1]

TFTs of polycrystalline silicon (poly-Si) and hydrogenated amorphous silicon are used in most LCD applications because their fabrication processes are compatible to very large scale integration (VLSI) technologies. A further advantage is their fabrication cost, since hard glass substrates are used. Moreover, polysilicon TFTs have a practical higher field-effect mobility[2] as compared with amorphous silicon TFTs. This renders them capable of peripheral drive circuit integration.[3]

Most studies of polysilicon TFTs are concentrated in reduction of the defects in polysilicon films to realize higher performance TFTs. Various approaches in the fabrication processes have been proposed[4–11] that are aimed in two directions: enlargement of the grain size of the polysilicon film and removal of defects in the poly-Si layer by hydrogen passivation. Recently, the effects of gate dielectrics on the characteristics of TFTs are receiving more and more attention. In this paper, the thickness effects of gate thermal oxides are investigated. Oxide/nitride dielectric structures as gate insulators are proposed. Their relationship to device performance, including threshold voltage, field-effect mobility, and ON/OFF state currents, is discussed.

2 Device Fabrication

We used 6- to 20-Ω-cm, 3-in.-diam, (100) oriented p-type silicon wafers to fabricate the investigated TFTs. Figure 1 shows a cross-sectional view of the polysilicon TFTs used in this experiment. A layer of silicon dioxide 600 nm in thickness was grown on the silicon substrate to simulate the glass substrate. Small-grained poly-Si film 300 nm thick was deposited on the substrate using low-pressure chemical vapor deposition (LPCVD) at 625°C and was defined as the active region. After a cleaning process, thermal oxides with different thicknesses and oxide/nitride dielectric structures with different thickness combinations of thermal oxides and LPCVD nitrides were formed. Then, a second layer of poly-Si was patterned to obtain the gate electrode. Ion implantation of arsenic at 180 keV to a dose of 4×10^{15} cm^{-2} or $POCl_3$ diffusion was implemented to form the source, drain, and gate. A layer of sputtering oxide was deposited and thermal annealing in a conventional furnace was conducted to activate the dopants and anneal out the damages induced by the im-

Invited paper DPT-07 received Jan. 22, 1993; revised manuscript received Mar. 28, 1993; accepted for publication Mar. 31, 1993. This paper is a revision of a paper presented at the SPIE conference on Display Technologies, Dec. 1992, Taiwan. The paper presented there appears (unrefereed) in SPIE Proceedings Vol. 1815.

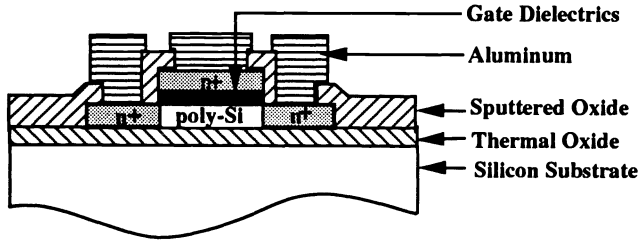


Fig. 1 Cross-sectional view of a polysilicon TFT.

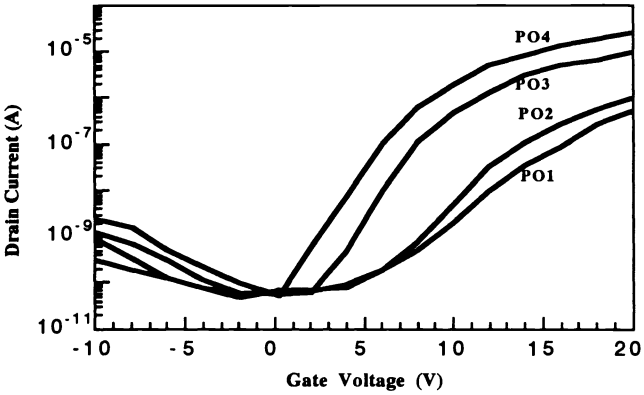


Fig. 2 The transfer curves of I_D versus V_G at $V_D = 1$ V for the pure-oxide samples with different gate-oxide thicknesses measured at $V_D = 1$ V.

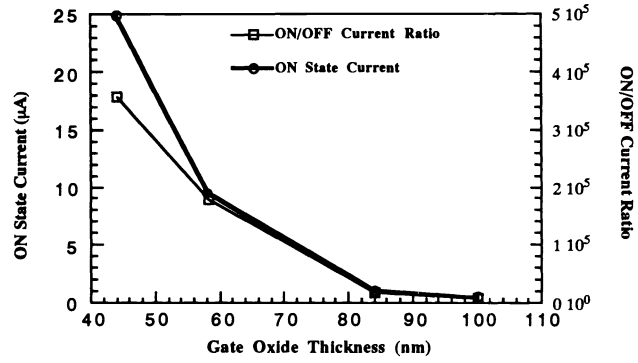


Fig. 3 The curves of ON-state current and ON/OFF current ratio versus gate-oxide thickness for the pure-oxide specimens.

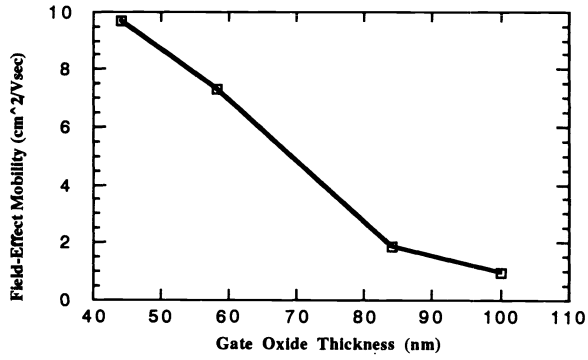


Fig. 4 Field-effect mobility dependence on the gate-oxide thickness for the pure-oxide samples.

plantation. Finally, contact holes were opened and Al evaporation was used to form the contact pads at the source, drain, and gate.

The thicknesses of gate oxides and silicon nitrides were measured by a Dektak IIA surface profile measurement tool and a Rudolph AutoEL III ellipsometer. The current-voltage measurements were tested using an HP 4145B semiconductor parameter analyzer.

3 Results and Discussion

3.1 *Thermal Oxides as Gate Dielectrics*

Polysilicon TFTs with gate oxides of 100, 84, 58, and 44 nm in thickness are labeled as PO1, PO2, PO3, and PO4, respectively. These samples were fabricated and measured to investigate the effect of gate-oxide thickness. The oxides of these samples were thermally grown at 1050°C and the source/drain regions were formed by $POCl_3$ diffusion at 950°C for 10 min and drive-in at 900°C for 20 min. Figure 2 shows the transfer curves of the samples PO1, PO2, PO3, and PO4, with channel length and channel width of 10 and 40 μm, respectively, measured with gate voltage (V_G) from -10 to 20 V and 0.3 V/step, and drain voltage (V_D) of 1 V. The OFF-state currents (I_{OFF}) are tested at $V_G = 0.2$ V, $V_D = 1$ V and the ON-state currents (I_{ON}) are extracted at $V_G = 20$ V, $V_D = 1$ V. The ON-state current increases with decreasing gate-oxide thickness (t_{OX}), while I_{OFF} is almost independent of t_{OX}, thus resulting in the increase of ON/OFF current ratio with decreasing oxide thickness, as shown in Fig. 3. In other words, TFTs with thinner gate oxides have better performance. The thinner gate oxide has the larger gate capacitance, so more carriers are induced by the preset gate voltage. This means that the thinner gate-oxide thickness improves the ability to induce the channel carriers. In contrast, I_{OFF} is defined at low V_G, where little channel induction occurs and it is not affected by the gate-oxide thickness.

The dependence of field-effect mobility and threshold voltage on the gate-oxide thickness is shown in Figs. 4 and 5, respectively. Threshold voltage V_T is defined at $V_D = 1$ V, $I_D = 1$ nA, and the field-effect mobility μ_{fe} of charge carriers is calculated at $V_D = 1$ V and $V_G = 20$ V. For TFTs with thinner gate oxides, the carrier mobilities become larger and the threshold voltages become smaller. A previous report also indicated that high-performance poly-Si TFTs could be obtained by reducing the gate-oxide thickness.[12]

We now discuss the results mentioned above more carefully. The potential barrier height in the channel of poly-Si can be described as

$$\phi_B = \frac{q^2 N_t^2 d_{ch}}{8\varepsilon_{Si} C_{OX}(V_G - V_T)} , \quad (1)$$

where q is the elementary charge, N_t is the trap-state density, d_{ch} is the induced channel thickness, ε_{Si} is the dielectric constant of silicon, and C_{OX} is the gate-insulator capacitance.[13] The effective carrier mobility of poly-Si is written as

$$\mu_{fe} = \mu_0 \exp(-\phi_B) , \quad (2)$$

where μ_0 is the preexponential term.[4,13] By shrinking the

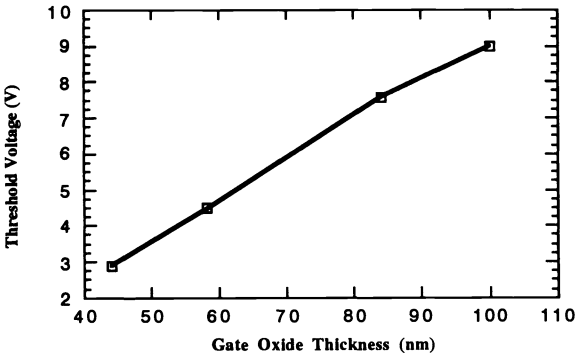


Fig. 5 Threshold voltage of TFTs with pure-oxide gates as a function of gate-oxide thickness.

thickness of the gate oxide, the gate capacitance is increased. Thus, the potential barrier is reduced. This results in the increase of carrier mobility. In addition, the threshold voltage is smaller for TFTs with thinner gate oxides, which leads to the increase of μ_{fe} and I_{ON} at a constant gate voltage. Moreover, TFTs with thin gate oxides have more electrons to be induced than those with thick gate oxides for the same gate bias, due to the higher capacitance. Thus, the PO4 samples have the highest ON-state currents because they have the strongest inversion at $V_G = 20$ V and $V_D = 1$ V. Furthermore, the better characteristics of TFTs with thin gate oxides may be also ascribed to the interface smoothness. The growth rate of oxide at poly-Si grain boundaries is faster than that in poly-Si grains because of the higher diffusivities of oxygen atoms in grain boundaries than those in grains. Thus, the interface morphology of poly-Si and silicon dioxide is rough. Hence, transporting electrons in the channels of poly-Si TFTs are scattered by the grooving polyoxides. As electrons drift from source to drain for TFTs with thicker gate oxides, they collide more easily with the rougher gate oxides. This phenomenon degrades the carrier mobility and the ON-state currents of TFT devices with thick gate oxides. This scattering effect of electrons is similar to that in single crystalling metal-oxide semiconductor field-effect transistors (MOSFETs) biased at very high fields.[12] Consequently, thinner oxides facilitate the mobility of poly-Si TFTs due to less electron scattering. Both the gate-oxide thickness and the interface morphology between the gate oxide and the poly-Si influence the carrier mobility of the poly-Si TFTs.

Since TFTs with thinner gate oxides have better performance and are interesting, samples with further thinning gate oxides of 18 nm in thickness were then fabricated. They also have better performance at low V_G, but the breakdown voltage at the gate is only 6.2 V. Hence, it is necessary to find a method to grow the thin gate dielectrics that possess high breakdown voltages. O/N gate structures are therefore chosen.

3.2 *O/N Dielectric Structures as Gate Insulators*

O/N dielectric structures to replace thermal oxides as the gate insulators of TFTs are proposed in accordance with the following reasons: (1) silicon nitride has twice the breakdown voltage of pure oxide with the same equivalent thickness, since the silicon nitride has almost the same breakdown field as the silicon dioxide,[14] which means silicon nitride is very promising for the device scaling down of TFTs; (2) silicon nitride is able to achieve smoother interface morphology than thermally grown polyoxide because the silicon nitride is deposited by the LPCVD method; and (3) silicon nitride has low fabrication temperatures when it is deposited by the LPCVD method. Hence, silicon nitride seems to be an extremely good material for gate insulators of TFTs. However, a problem in adopting silicon nitride is the large interface stress between silicon nitride and poly-Si. This is also the reason why silicon nitride is rarely used as a gate insulator of single crystalline MOSFETs. Thus, a thin thermal pad polyoxide is grown beneath the silicon nitride to reduce the high stress at the interface between the silicon nitride and poly-Si substrate.

Table 1 Summary of TFT parameters of O/N specimens with nearly the same equivalent oxide thickness.

TFT Parameters \ Sample	ON1	ON2	ON3	ON4
Thickness of Pad Oxide (Å)	0	125	180	225
Thickness of Nitride (Å)	970	830	680	490
Equivalent Oxide Thickness (Å)	485	540	520	470
ON State Current (μA)	1.471	1.681	0.853	0.410
ON/OFF Current Ratio	$7.4\ 10^3$	$9.0\ 10^3$	$6.0\ 10^3$	$1.9\ 10^3$
Field-Effect Mobility (cm^2/Vsec)	1.52	1.92	1.13	0.40
Threshold Voltage (V)	7.65	7.55	7.75	8.2

Table 2 Gate dielectrics of O/N samples with different equivalent dielectric thickness.

Dielectric Thickness \ Sample	ON5	ON6	ON7	ON8	ON9
Thickness of Pad Oxide (Å)	200	125	100	125	100
Thickness of Nitride (Å)	680	380	380	185	200
Equivalent OxideThickness (Å)	540	315	290	218	200

First, TFTs with O/N gate insulators of nearly the same equivalent oxide thickness labeled as ON1, ON2, ON3, and ON4 were fabricated to understand the effect of pad oxides. Table 1 shows a summary of the TFT parameters of these samples. The pad oxides of these TFTs were all thermally grown at 850°C and the nitride were all deposited at 750°C by LPCVD. The source/drain regions were formed by arsenic ion implantation and post-implantation annealing at 850°C. As can be seen from Table 1, TFTs with thinner pad oxides have better performance, which is attributed to the smoother gate insulator/poly-Si interface. However, TFTs without pad oxides, i.e., the ON1 samples, have worse characteristics than those with a pad oxide of 125 Å in thickness because of the interface stress. In other words, utilization of the O/N structure with a polyoxide 125 Å thick can improve the electrical properties of TFTs.

Secondly, the effect of O/N-structure gate dielectrics with various equivalent oxide thicknesses was also studied. Table 2 shows the gate insulator combinations of different equivalent oxide thicknesses specified as ON5, ON6, ON7, ON8, and ON9. These samples have almost the same thickness of pad oxides. The carrier mobility and ON-state current for these TFTs are defined at $V_G = 20$ V, except those of the

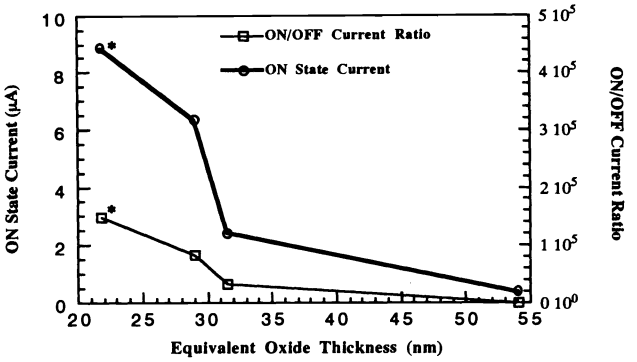


Fig. 6 Dependence of ON-state current and ON/OFF current ratio on the equivalent gate dielectric thickness.

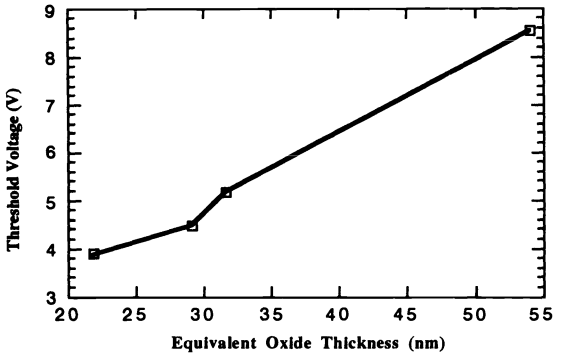


Fig. 8 Dependence of the threshold voltage on the equivalent oxide thickness for the O/N specimens.

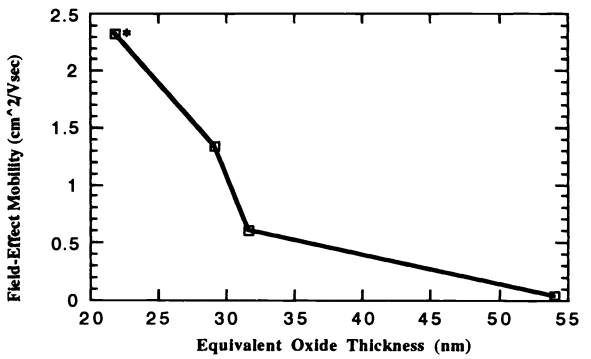


Fig. 7 Field-effect mobility as a function of equivalent oxide thickness for the O/N samples(*measured at $V_G = 15$ V; others at $V_G = 20$ V).

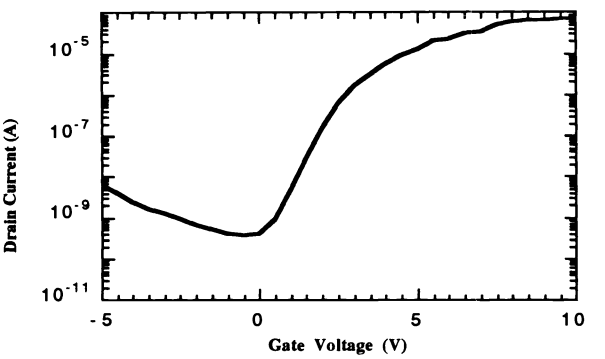


Fig. 9 Characteristics of I_D versus V_G at $V_D = 1$ V for the samples ON10 fabricated at temperatures below 750°C.

ON9 samples defined at $V_G = 15$ V. The ON-state current and ON/OFF current ratio of TFTs with O/N gate structure as a function of the equivalent oxide thickness of the gate insulator are shown in Fig. 6. The dependencies of the field-effect carrier mobility and the threshold voltage on the equivalent oxide thickness are shown in Figs. 7 and 8, respectively. The carrier mobility of these specimens with O/N gate structures is smaller than those with pure oxides because the fabrication temperature is lowered from 1050 to 850°C. These parameters for the O/N gate structures show the same dependence on the equivalent oxide thickness as those for the thermal oxide gate. Namely, TFTs with O/N gates of thinner equivalent oxide thicknesses have better electrical properties than those with thicker O/N dielectrics. The better performance of TFTs with thinner O/N gates is also partly attributed to the higher capacitance and smoother interface morphology.

3.3 *Electrical Properties of TFTs with Optimum O/N Gate Structures*

In this experiment, the ON9 samples have the thinnest gate insulator. Hence, they possess the best electrical characteristics among all of the testing samples. With the shrinking down of the gate dielectric thickness, the gate cannot endure the high voltage necessary to satisfy the requirements of applications. To further improve the electrical properties of TFTs with O/N structures, the ON10 samples were fabricated. The ON10 specimens have the active poly-Si layer LPCVD at 675°C. After the definition of the poly-Si island, a thin pad oxide 100 Å thick is thermally grown at 750°C and subsequently deposited with 200-Å-thick silicon nitride at 750°C in a LPCVD system. A second layer of poly-Si for the gate region is then deposited and patterned. Ion implantation by arsenic and a following annealing at 750°C are carried out to form the source, drain, and gate. The fabrication processes of samples ON10 are the same as those of ON9, except the deposition temperature of the poly-Si active layer is raised from 625 to 675°C. The transfer curve of I_D versus V_G at $V_D = 1$ V for the specimens ON10 is shown in Fig. 9. The field-effect mobility, ON-state current, and ON/OFF state current ratio are improved to 17.4 cm^2/V s, 77.9 μA, and 2.2×10^5, respectively, at $V_G = 10$ V and $V_D = 1$ V. For the conventional process, grain-growth schemes, such as Si^+ self-amorphization and recrystallization, and long-time grain growth are very complex or inconvenient. By using O/N gate structures, better performance TFTs with as-deposited poly-Si for the active layer can be achieved.

4 Summary and Conclusions

The thickness of gate oxides plays a very important role in the influences of the characteristics of TFTs. The effective carrier mobilities of the devices with the thin gate oxides are several times as large as those of TFTs with thick gate oxides. Thin gate oxides suffer from low breakdown voltages, so silicon nitrides are proposed instead. Silicon nitride has the advantages of high breakdown voltage, smooth gate

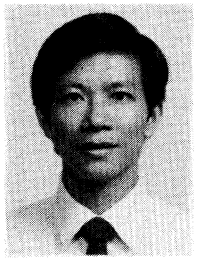
dielectric/poly-Si interface, and lower fabrication temperatures as compared to thermal oxides, but the disadvantage of large interface stress. Hence, O/N dielectric structures as gate insulators have been utilized to improve the electrical properties of TFTs. In contrast to conventional TFTs with pure thermal oxides as gates, TFTs with O/N gate structures can attain a higher ON/OFF current ratio and carrier mobility by reducing the equivalent oxide thickness. Consequently, the performance of TFTs can be easily improved by thin O/N gate structures.

Acknowledgments

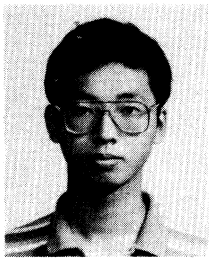
This research was supported in part by the National Science Council under contract no. NSC-82-0404-E009-235. Support from the National Nano Device Laboratory is also acknowledged.

References

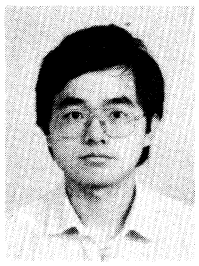
1. J. Magarino, "Amorphous silicon diodes and TFTs for active matrix flat panel display applications," *Appl. Phys. A* **41,** 297–303 (1986).
2. S. Morozumi, R. Araki, H. Ohshima, M. Matsuto, T. Nakazawa, and A. Sato, "Low temperature processed poly-Si TFT and its application to large area LCD," in *Proc. Japan Dispay '86,* pp. 196–199 (1986).
3. J. Ohwada, M. Takabatake, Y. A. Ono, A. Mimura, K. Ono, and N. Konishi, "Peripheral circuit integrated poly-Si TFT LCD with gray scale representation," *IEEE Trans. Electron Devices* **ED-36,** 1923–1928 (1989).
4. G. Harbeke, L. Krausbauer, E. F. Steigmeter, and A. E. Widmer, "Growth and physical properties of LPCVD polycrystalline silicon films," *J. Electrochem. Soc.* **131,** 675–682 (1984).
5. T. Aoyama, G. Kawachi, N. Konishi, T. Suzuki, Y. Okajima, and K.Miyata, "Crystallization of LPCVD silicon films by low temperature annealing," *J. Electrochem. Soc.* **136,** 1169–1173 (1989).
6. H. Hayashi, T. Noguchi, T. Ohshima, M. Negishi, and Y. Hayashi, "Advanced high mobility polysilicon super thin-film transistor (STFT) using solid phase growth" in *Extended Abstracts 18th Conf. Solid State Devices and Materials,* pp. 549–552 (1986).
7. P. Migliorato and D. B. Meakin, "Material properties and characteristics of polysilicon transistors for large area electronics," *Appl. Surface Sci.* **30,** 353–371 (1987).
8. A. Ishizu, Z. Suzuki, T. Matsumoto, J. Miki, and Y. Ohnishi, "An active-matrix LC display addressed by re-crystallized poly-Si TFTs," in *SID 85 Dig.,* pp. 282–285 (1984).
9. A. Mimura, K. Miyata, T. Suzuki, Y. Hosokawa, H. Kawakami, N. Konishi, Y. A. Ono, K. Ono, and J. Ohwada, "High performance low-temperature poly-Si n-channel TFTs for LCD," *IEEE Trans. Electron Devices* **ED-36,** 351—359 (1989).
10. D. L. Chen, A. M. Guzman, and D. W. Greve, "Effect of hydrogen implantation on polysilicon p-n junctions," *IEEE Trans. Electron Devices* **ED-33,** 270–274 (1986).
11. H. Shichijo, S. D. S. Malhi, W. F. Richardson, G. P. Pollack, A. H. Shah, L. R. Hite, S. K. Benerjee, M. Elahy, R. Sundaresan, R. H. Womack, H. W. Lam, and P. K. Chatterjee, "Polysilicon transistors in VLSI MOS memories," in *IEDM Tech. Dig.,* pp. 228–231 (1984).
12. F. Qian, D. M. Kim, H. K. Park, and J. L. Sachitano, "Inversion-mode MOSFETs in polycrystalline silicon thin films: characterization and modeling," *IEEE Trans. Electron Devices* **ED-35,** 2439–2449 (1987).
13. H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide(insulator)-semiconductor transistors (MOST)," *IEEE Trans. Electron Devices* **ED-12,** 139 (1965).
14. S. M. Sze, "MOSFET," Chapter 8 in *Physics of Semiconductor Devices,* 2nd ed., pp. 431–510, Wiley, New York (1981).



Huang-Chung Cheng received the BS degree from National Taiwan University in 1977 and the MS and PhD degrees in materials science and engineering from National Tsing Hua University of Taiwan in 1979 and 1985, respectively. From 1981 to 1982, he served as a research assistant at the Materials Research Institute in Taiwan. From 1982 to 1984, he was a lecturer at the Chiao Tung University in Taiwan. In 1985, he joined National Chiao Tung University of Taiwan as an associate professor in the Department of Electronics Engineering and Institute of Electronics. Since 1986, he has served as a consultant in the microelectronics industry. He has conducted research on semiconductor materials and devices, electro-optics, liquid crystal display, and material analysis and characterization. His present research areas include ultra large scale integration technologies such as reliability of thin gate dielectrics and contact properties of metals on semiconductors; thin-film transistors of amorphous, polycrystalline, and laser-recrystallized silicon; vacuum microelectronics; and GaAs devices. Dr. Cheng is a member of Phi Tau Phi, IEEE, and the Material Research Society.



Ya-Hsiang Tai received the BS degree from the Department of Electronics Engineering, National Chiao Tung University, Taiwan, in 1990. Currently, he is a PhD candidate at the Institute of Electronics, National Chiao Tung University. He is engaged in the development of thin-film transistors and their applications in liquid crystal displays. Mr. Tai is a member of Phi Tau Phi, Taiwan.



Ming-Shiann Feng received his BS degree in material science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1982 and the MS and PhD degrees in materials science and engineering from the University of Illinois at Urbana-Champaign in 1986 and 1989, respectively. In 1989, he joined the Institute of Materials Science and Engineering, National Chiao Tung University, as a faculty member. He has worked on III-V microwave and optoelectronic materials and devices (metal-semiconductor field effect transistors, heterojunction bipolar transistors, light emitting diodes, and laser diodes) by metal-organic chemical vapor deposition, as well as display materials and devices (thin-film transistor liquid crystal displays and field-effect diodes). Dr. Feng is a member of the Material Research Society and the Society for Information Display.

Jau-Jey Wang received the BA degree in electrical engineering from National Sun-Yet-San University, Taiwan, in 1986 and the MS degree in electronics engineering in 1988 from National Chiao Tung University, Taiwan. He joined the Technology Development Division of the Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan, in 1990. He has been involved in various aspects of very large scale integration technology development and process transfer. He is currently in charge of salicide technology development for submicron processes.