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Cu Contamination Effect in Oxynitride Gate Dielectrics

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We have studied the effect of Cu contamination in oxynitride gate dielectrics. Compared to thermal SiO_2 with a physical thickness of 3-5 nm, the oxynitride shows a much improved Cu contamination resistance. Furthermore, the Cu contamination resistance increases with increasing nitrogen content. The mechanism of improved gate dielectric resistance to Cu is due to the strong diffusion barrier properties of oxynitride as observed by secondary ion mass spectroscopy.
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Copper interconnect technology has been widely implemented in very-large-scale-integration (VLSI) processes because it can reduce the back-end resistance-capacitance delay as required for advanced high speed complementary-metal-oxide-semiconductor (CMOS) circuits. However, Cu contamination is an important concern because Cu related front-end gate dielectric degradation has been reported[1-7] and an appropriate Cu barrier metal must be applied to reduce the Cu out-diffusion. Previously, almost all the Cu contamination studies were focused on its effect on SiO_2 gate dielectrics. Presently, however, high-k gate dielectrics are necessary for further scaling down the VLSI technology.[8-13] Therefore, the study of Cu contamination in high-k dielectric is important for future process integration considerations.

In this paper, we present our studies of the Cu contamination effect in oxynitride gate dielectrics with different N contents. An oxynitride gate dielectric is known to be one of the best candidates used for sub-0.1 μm technology because of its superior boron penetration resistance[14] in combination with its high-k properties. In contrast to the increased trap-assisted leakage current[6] or reduced effective barrier[7] in thermal SiO_2 after Cu contamination, we have found negligible electric characteristic degradation in oxynitride gate dielectrics. According to secondary ion mass spectroscopy (SIMS) measurements, the much-improved Cu contamination resistance is due to the largely reduced Cu diffusion through oxynitride. The much better Cu contamination resistance may be an additional merit for high-k oxynitride gate dielectrics.

Experimental

4 in. p-type Si(100) wafers with 1-10 Ω cm resistivity were used in this study. The oxynitride prepared by oxidizing silicon nitride is similar to the process published in the literature.[10] After the standard RCA clean and 300 nm field oxide patterning, the oxynitride was formed by depositing a 3 nm chemical vapor deposition (CVD) SiN from dichlorosilane and ammonia at 750°C, and subsequently, oxidizing at 900°C for 30-70 min. To avoid a reduction of the effective k, a native oxide was eliminated by HF vapor passivation[12-13] and *in situ* desorption inside the low-pressure CVD (LPCVD) system.[15] The additional oxidation after SiN deposition is to reduce the dielectric and interface traps within the SiN, although the effective k value is also reduced. Different oxidation times are used to form oxynitride film of different N contents. The thickness and refractive index of the oxynitrides were measured by ellipsometry, and the dielectric constant k was measured by the voltage-capacitance (C-V) method. Then a 300 nm poly-Si layer was deposited on the oxynitride and n^+ doped by $POCl_3$. Finally, MOS capacitors of 100×100 μm were fabricated after Al metallization and sintering. The Cu contamination was performed by immersing the Si wafers into a diluted $Cu(NO_3)_2$ solution of 10 ppb and 10 ppm. The contaminated MOS capacitor was further annealed at 400°C for 1 h in a nitrogen gas ambient. More details on the Cu contamination process can be found in our previous publications.[6,7] Standard current-voltage (I-V) and C-V measurements were used to investigate the electrical property changes caused by the Cu contamination. The oxygen and nitrogen content in the oxynitride gate dielectric was measured by X-ray photoelectron spectroscopy (XPS).

Results and Discussion

Table I summarizes the dielectric properties of the studied oxynitride dielectrics. The oxynitride thickness after oxidizing for 30, 50, and 70 min are 3.6, 4.4, and 4.7 nm, and the nitrogen content in the oxynitrides are 23, 16, and 14%, respectively. The k values of 4.7, 4.5, and 4.4 are obtained for the 3.6, 4.4, and 4.7 nm oxynitride capacitors, respectively, which give respective an equivalent oxide thickness (EOT) of 3.0, 3.8, and 4.2 nm for the three oxynitride dielectrics. The typical interface trap density from C-V measurement increases from 3×10^{10} to 1×10^{11} eV^{-1}/cm^2 for an increasing N content from 14 to 23%, indicating a reasonable interface quality for the oxynitride gate dielectrics.

Based on the good dielectric properties of high-k oxynitrides, we have further studied the Cu contamination effect. Figure 1a shows current density-voltage characteristics of different EOT oxynitrides before and after the contamination. For comparison purpose, we also show in Fig. 1b the Cu contamination effect on a 3 nm SiO_2 gate dielectric.[7] As shown in Fig. 1a, a Fowler-Nordheim tunneling current is observed for all three oxynitrides demonstrating good dielectric properties due to a reduced trap density after oxidation. The Cu-contaminated 4.7 nm oxynitride shows a slightly higher pretunneling current, which is due to trap-assisted tunneling as reported previously.[6] In contrast, negligible changes in the pretunneling current[6] and the Fowler-Nordheim tunneling current[7] are observed for the thinnest 3.6 nm oxynitrides. The much-improved Cu contamination resistance as compared with thermal SiO_2 with a physical thickness of 3.0 nm shown in Fig. 1b is believed to be due to the high nitrogen content in the oxynitrides.

Table I. Important dielectric properties of oxynitrides formed by oxidizing a CVD deposited SiN.

Oxidation time	30 min	50 min	70 min
Refractive index	1.65	1.6	1.58
Physical thickness (nm)	3.6	4.4	4.7
EOT (nm)	3.0	3.8	4.2
k from C-V	4.72	4.46	4.41
N% from XPS	23%	16%	14%

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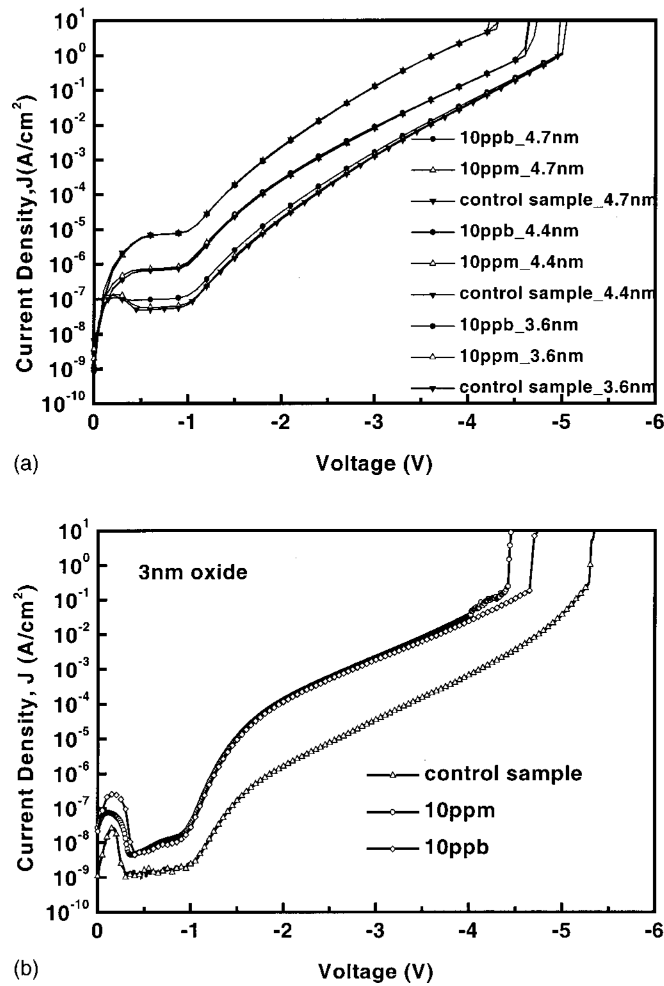

Figure 1. J-V characteristics of gate capacitors with (a) 3.6, 4.4, and 4.7 nm oxynitrides and (b) 3.0 nm SiO_2. The devices are contaminated by 10 ppb or 10 ppm Cu.

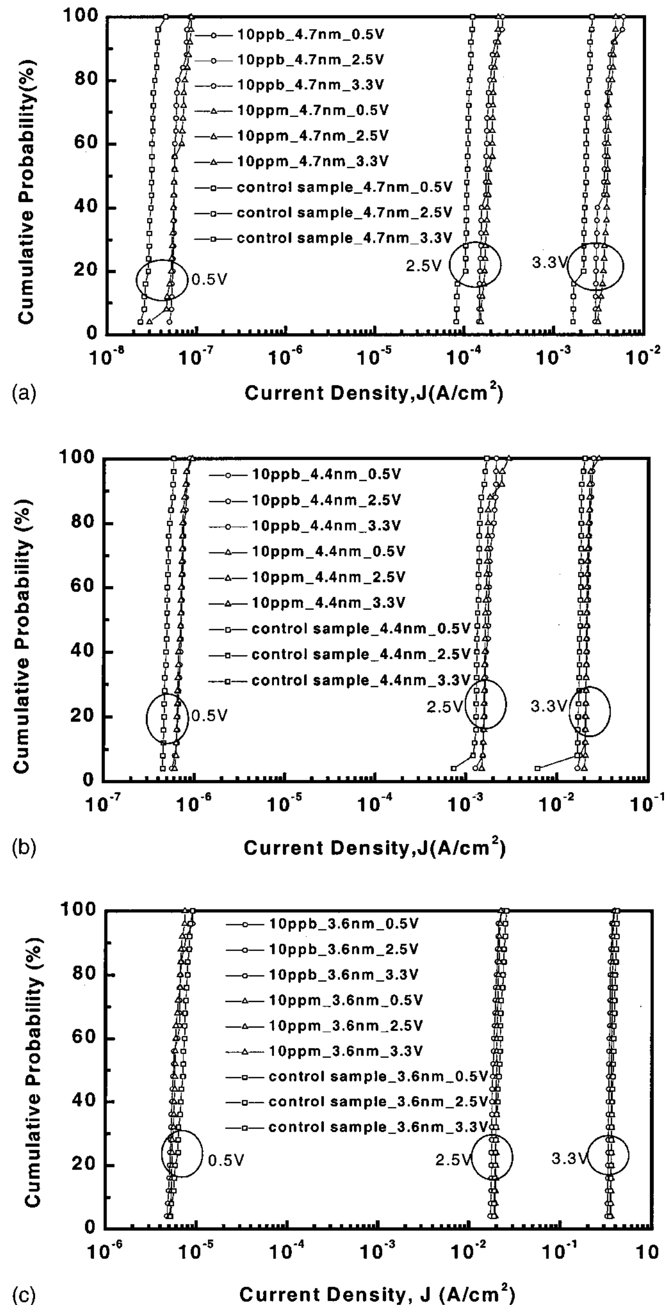

Figure 2. The cumulative current distribution of (a) 4.7 nm, (b) 4.4 nm, and (c) 3.6 nm oxynitrides contaminated by 10 ppb and 10 ppm Cu.

The cumulative leakage current distributions of the respective 3.6, 4.4, and 4.7 nm oxynitrides are shown in Fig. 2a, b, and c. For the thickest 4.7 nm oxynitride with the lowest nitrogen content, the Cu contamination increases the leakage current and the contamination effect saturates for a Cu concentration above 10 ppb. This saturation effect is believed to be due to the limited Cu solubility in the dielectric during the annealing at 400°C for 1 h.[6] Although a similar Cu saturation contamination effect is also observed in the thinner 4.4 nm oxynitride, the leakage current increase is reduced. However, the current increase is negligible for the thinnest 3.6 nm oxynitride with the highest nitrogen content of 23%, which is in sharp contrast to the much larger leakage current for the 3.0 nm thermal SiO_2 shown in Fig. 1b. The reduced Cu contamination effect with increasing nitrogen content suggests that nitrogen strengthens the resistance against Cu contamination coming from the wafer front side.

One advantage of incorporating nitrogen into the oxide is the improved reliability. We have also studied the stress-induced leakage current (SILC) effect in these oxynitrides. Figures 3a and b show the stress effect on [J(t)-J(0)]/J(0) for 14 and 23% nitrogen content, respectively. The stress for both samples is performed at a constant electric field of ~6.3 kV/cm for 200 s, which gives a total charge injection of 7 and 70 C/cm^2 for the oxynitrides with 14 and 23% nitrogen content, respectively.

Under the same stress condition, the control oxynitrides in both cases show the smallest current increase and the Cu contamination increases the SILC effect. The saturated [J(t)-J(0)]/J(0) for increasing Cu concentration is consistent with the saturated current increase in the J-V characteristics shown in the right axis, and attributed to the saturated Cu solubility at 400°C. However, a much-reduced SILC effect is observed for the oxynitrides with 23% nitrogen as compared with our previous work in SiO_2.[7] Because the increased SILC effect in the Cu contaminated oxynitride is due to the increased bulk and interface traps, the small SILC effect in the oxynitrides with 23% nitrogen demonstrates both the excellent Cu diffusion barrier property and the strong Si-N bonding in this sample. The improved SILC effect is important for the reliability of oxynitride gate dielectrics used for sub-0.1 μm technologies.

To study the much-improved Cu contamination resistance, we have used SIMS to measure the Cu concentration within the oxynitride. Figure 4 shows the SIMS profile of the 4.7 nm oxynitride after Cu contamination. In contrast to the Cu penetration through SiO_2

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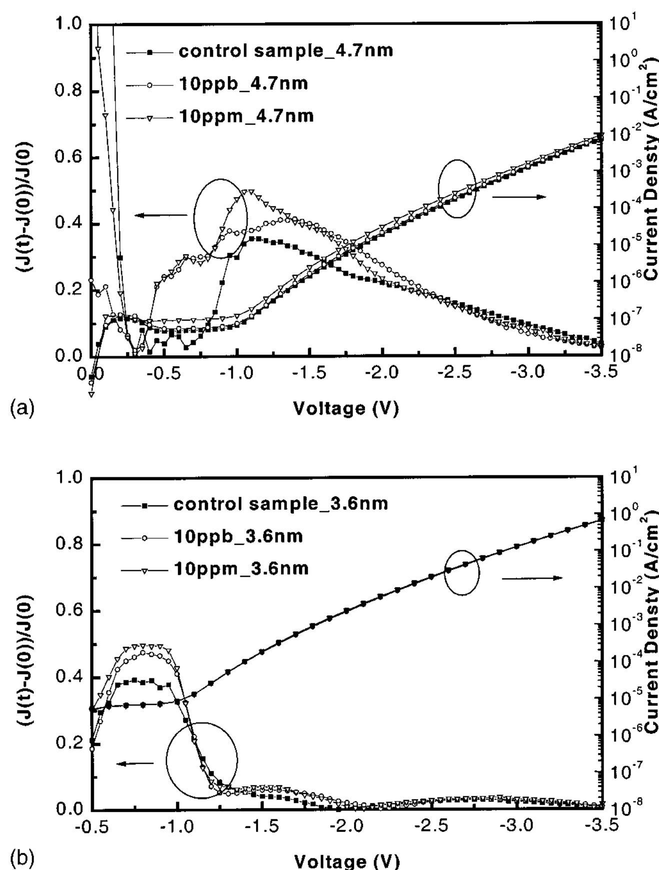

Figure 3. SILC effect of (a) 4.7 nm and (b) 3.6 nm oxynitrides contaminated by 10 ppb and 10 ppm Cu.

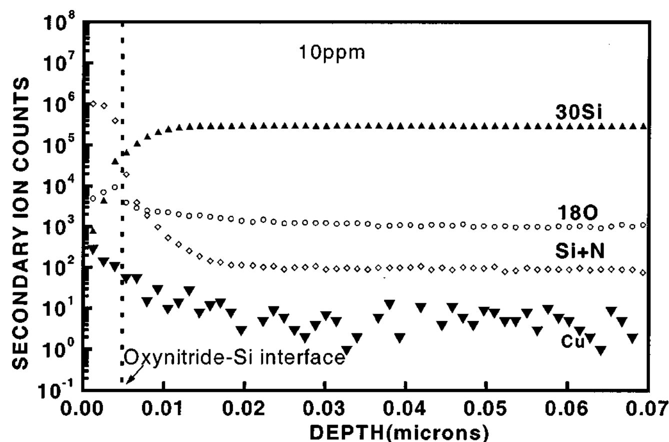

Figure 4. SIMS profile for the 4.7 nm oxynitride contaminated by 10 ppm Cu from the front side of the wafer.

reported previously,[7] the Cu concentration is very small within the oxynitride and decreases rapidly inside the Si substrate. Therefore, the presence of nitrogen inside the Si oxide layer behaves as a diffusion barrier for Cu. This is also confirmed by the increased Cu contamination resistance for increasing nitrogen content. A similar strong resistance to boron penetration is also observed for oxynitrides used for sub-micrometer p-type MOS field effect transistors.[14]

Conclusions

Gate dielectric degradation by Cu contamination is greatly reduced in oxynitrides as compared with thermal SiO_2, and the Cu contamination resistance increases with increasing nitrogen content. Improved gate dielectric resistance to adverse Cu contamination is attributed to the strong diffusion barrier property of the oxynitride as observed by SIMS.

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