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Impact of interface nature on deep sub-micron Al-plug resistance

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Abstract

Sputter clean had been accepted as an effective surface clean process prior to metal deposition. In this work, the impact of interface nature on via resistance of Al-interconnect as via size is scaled down to 0.16 μm was studied. Al–F compound was identified as the main interfacial contaminants after standard post-etch clean process if the TiN layer of the underlying metal line were etched through during via etch. For via size larger than 0.25 μm (aspect ratio lower than 3.2), Al–F compound can be removed by sputter clean effectively. However, below 0.25 μm, sputter clean efficiency decreases such that via resistance is degraded by the existence of Al–F interfacial layer. On the other hand, sputter clean results in oxide re-deposition, which in turn degrades via resistance. It is suggested that to obtain low resistance sub-0.2 μm via, via etch must stop on TiN layer such that no Al–F layer can be formed. Otherwise, new interfacial layer clean technology with high efficiency and without side effect has to be developed. © 2001 Elsevier Science Ltd. All rights reserved.

1. Introduction

As ULSI back-end-of-line wiring is continuously scaled to narrower than sub-quarter micron, conventional W-plug and Al-wire process suffers severe drawbacks like high cost, high via resistance (R_v), and poor electromigration resistance. Cu-wire is expected to be required in the sub-0.13 μm technology node [1]. However, Cu process manufactory is still not mature and has highly contamination issues. On the other hand, advanced pure Al metallization (using simultaneously planarized Al-plug instead of W-plug) has attracted much attention due to its high performance, low cost and superior compatibility with previously technologies [2–7]. It is also expected that Al-interconnect will be used in memory circuits at least down to 0.13 μm technology node [1]. Recently, several Al filling technologies had been proposed to overcome the Al filling difficulties [5–7]. An Al-interconnect process with sub-0.2 μm via based on long throw sputtering (LTS) technology had been reported [7]. All of the above works revealed the extendibility of Al-interconnect into 0.13 μm technology node.

Besides the plug filling technology, the interface nature is another pre-dominant factor to achieve high quality via. Several literatures focused on the interface clean process had been published [8–11]. A three-steps clean process was proposed based on these studies: (i) an oxygen or ozone ashing process to remove the pure fluorocarbon (CF_x) film generated during main etch; (ii) an additional wet clean to remove the CF_x film containing non-volatile metal contamination generated during over etch; and (iii) an in situ sputter clean prior to metal deposition to remove any remaining contaminants as well as metal oxide layers formed during air exposure. However, the via sizes used in most of the previous works are larger than 0.5 μm. Gambino reported a dual damascene structure with 0.22 μm via, but the aspect

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ratio (AR) of via hole itself (excluding trench height) is less than 3.0 [11].

In this work, the impact of interface nature on via resistance as via size is scaled down to 0.16 μm was studied. It is reported for the first time that the efficiency of sputter clean degrades as via size is scaled to be less that 0.25 μm ($AR > 3.2$). If tough compound was formed during via etch process, it is hard to be removed by ion sputtering. In the next section, the sample preparation procedure to from Al-plug of various via size is described. The electrical results are presented in Section 3. Structural and material analyses were performed and a model is proposed in Section 4. This is followed by the conclusions in Section 5.

2. Sample preparation

Double metal interconnect test structure was fabricated to investigate the effect of sputter clean on via resistance. The first layer metal (M1) was deposited at room temperature with stacked structure of TiN(30 nm)/Ti(10 nm)/AlCu(480 nm)/TiN(30 nm). The intermetal dielectric (IMD) was deposited in a high density plasma chemical vapor deposition system and was planarized and polished back by chemical mechanical polishing. The final thickness of IMD above M1 was 800 nm.

A high density plasma etcher with a gas mixture of Ar, C_2F_6, C_4F_8, CO, and/or CH_2F_2 was used to etch via hole. The C_2F_6 gas is the main etch gas while the CH_2F_2 and C_4F_8 are attributed to polymer gas generally. Two recipes, E1 and E2, with different gas ratio were used. The main etch step of E1 and E2 recipes are identical. Both recipes switch to over etch step before the TiN layer of M1 is exposed. Table 1 lists the detailed conditions of the over etch step of these two recipes. Vias with various bottom diameters of 0.38, 0.34, 0.25, 0.23, 0.21, 0.16 μm were patterned simultaneously. The corresponded AR is 2.1, 2.3, 3.2, 3.5, 3.8, and 5.0. Because the E1 recipe has more etch gas (C_2F_6), less polymer gases (CH_2F_2 and C_4F_8), and longer over etch time than the E2 recipe has, the microloading effect performance

Table 1
The over etch recipe used for via etch

Recipe	Top power (W)	Bottom power (W)	Pressure (mTorr)	Ar (sccm)	C_2F_6 (sccm)	C_4F_8 (sccm)	CH_2F_2 (sccm)	CO (sccm)	Time (s)
E1	800	800	10	100	24	8	0	35	70
E2	900	1250	15	125	15	10	12	35	50

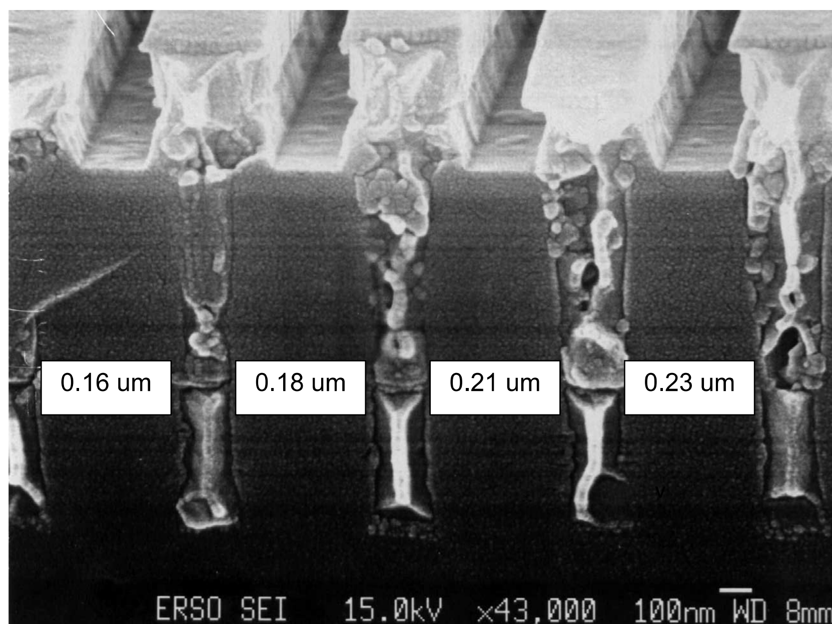

Fig. 1. The cross-sectional SEM micrograph of Al-plug with various via size. The via was etched by E1 recipe. Good profile and perfect Al filling were achieved.

of E1 recipe is less pronounced than that of E2 recipe and the etch rate selectivity of SiO_2 to TiN of E1 recipe is lower than that of E2 recipe. Both recipes produced good via profile. But, E1 recipe etches through the TiN layer of M1 effectively at all via sizes while E2 recipe leaves some TiN as via size is smaller than 0.25 μm. Oxygen plasma ashing and organic solvent rinse were employed as post-etch clean process.

Prior to metal deposition, argon plasma generated by an inductively coupled plasma source at 100 W was used to clean the exposed metal surface at via bottom for 0, 15, and 30 s. A two-steps cold/hot Al-interconnect technology was used to form Al-plug and the second layer metal. Sputter clean and metal deposition were performed sequentially in various chamber of the same LTS system without breaking vacuum. The metal deposition condition had been reported [7]. Fig. 1 shows the cross-sectional scanning electron microscopic (SEM) micrograph of vias with various size of 0.16, 0.18, 0.21, and 0.23 μm. Good profile and perfect metal filling were achieved. All of the sample ID and the corresponded process conditions are listed in Table 2.

Via chains of various via size were used to evaluate the interface effect. Each via chain consists of 10,240 vias. The averaged via resistance (R_v) is calculated from the total resistance of via chain divided by the via number. Forty-eight via chains were measured on each wafer.

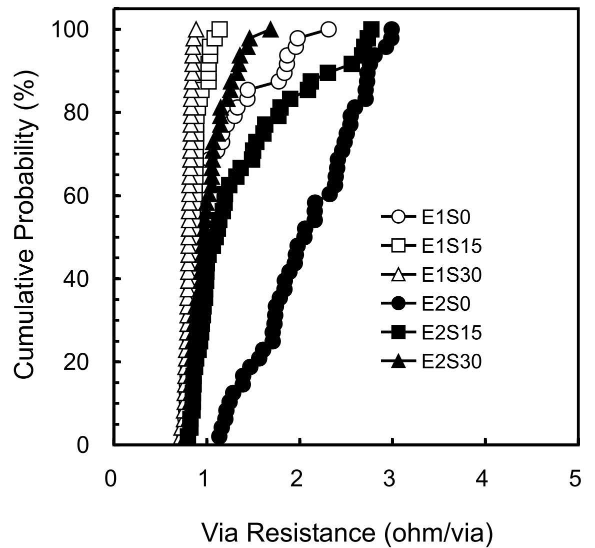

Fig. 2. The cumulative probability of via resistance of 0.38 μm via.

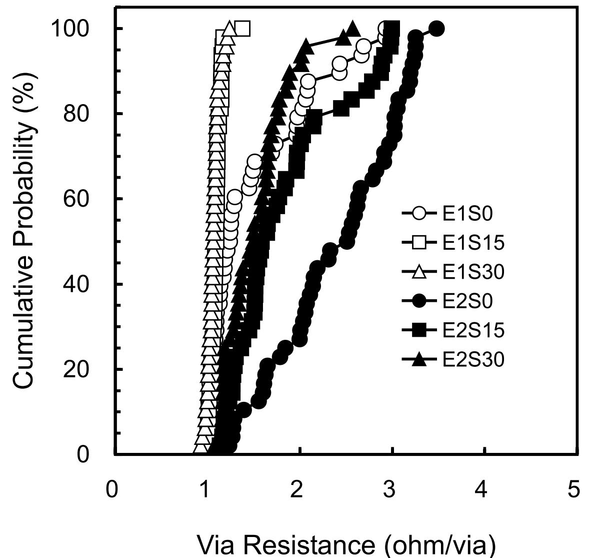

Fig. 3. The cumulative probability of via resistance of 0.34 μm via.

3. Electrical results

3.1. *Via size > 0.3 μm*

Figs. 2 and 3 show the cumulative probability of R_v of 0.38 and 0.34 μm vias, respectively. For samples without sputter clean prior to metal deposition, some high resistance vias were observed. By checking the wafer mapping, it is observed that the high resistance vias locate near the wafer center. A 15 or 30 s sputter clean reduces the percentage of high resistance vias of samples etched by E1 recipe effectively. For samples etched by E2 recipe, sputter clean can reduce the percentage of high resistance vias but some high resistance via still exist after 30 s sputtering. Longer sputtering time is required to remove the high resistance vias in this

Table 2
The sample ID and the process condition

	Sample ID					
	E1S0	E1S15	E1S30	E2S0	E2S15	E2S30
Via etch recipe	E1	E1	E1	E2	E2	E2
Sputter time (s)	0	15	30	0	15	30

case. These results indicate that no matter what kind of interfacial layer exists at via bottom, it can be reduced by Ar ions sputtering. Since the metallization process is identical for all samples, the difference in the percentage of high resistance vias between samples etched by E1 and E2 recipes should be attributed to the difference of etch recipe and will be discussed in the next section.

3.2. 0.2 μm < via size < 0.3 μm

Figs. 4–6 show the cumulative probability of R_v of 0.25, 0.23, 0.21 μm vias, respectively. The via resistance increases with the decreases of via size as expected. But the process dependence of R_v is quite different from that shown in Figs. 2 and 3. For samples etched by E1 recipe, the sputter clean condition almost does not affect via resistance and its variation in each figure. For samples etched by E2 recipe, the sputter clean even deteriorates the via resistance. The sample without sputter clean (E2S0) has the lowest R_v while it has the highest R_v when the via size is larger than 0.3 μm. By increasing the sputtering time, some high resistance vias occur. At the same sputter time, the larger the via size is, the more the high resistance vias are observed.

3.3. Via size < 0.2 μm

Fig. 7 shows the cumulative probability of via resistance of 0.16 μm via. Yield loss (opened via chain) is observed for this via size. This is not observed at larger via size. For samples etched by E1 recipe, the sputter clean almost does not affect the via resistance, but the yield was improved from 83% to 96% as sputter time was increased from 0 to 30 s. For samples etched by E2 recipe, the yield is very low as the sputter time is shorter than 15 s. A 30 s sputter clean can improve the yield but there is still a 15% yield loss (sample E2S30). The via resistance of sample E2S30 is 2 Ω lower than the via resistance of samples etched by E1 recipe.

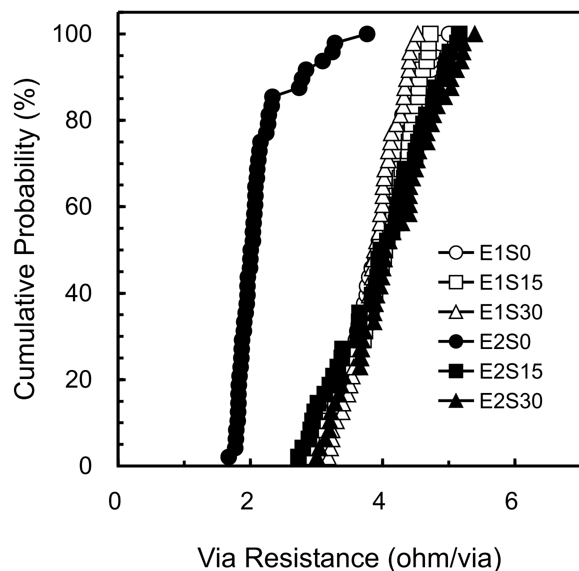

Fig. 4. The cumulative probability of via resistance of 0.25 μm via.

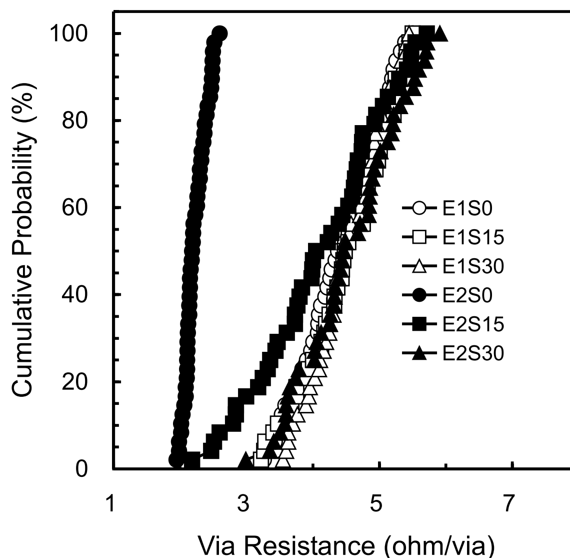

Fig. 5. The cumulative probability of via resistance of 0.23 μm via.

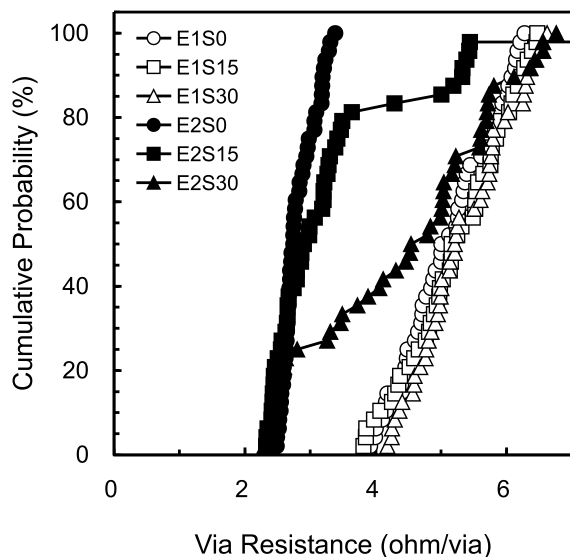

Fig. 6. The cumulative probability of via resistance of 0.21 μm via.

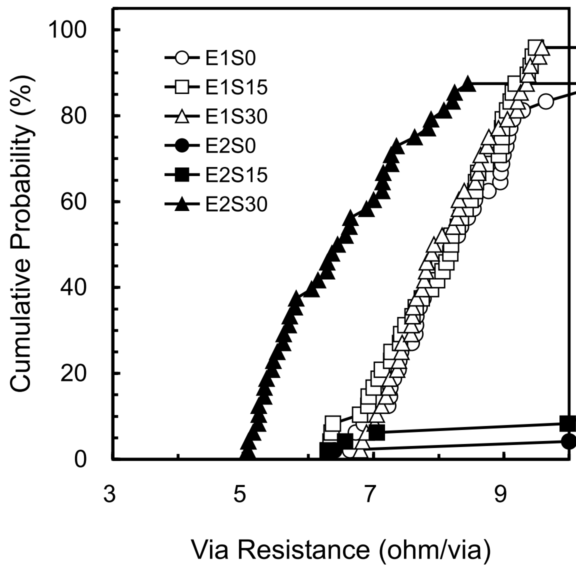

Fig. 7. The cumulative probability of via resistance of 0.16 μm via.

4. Discussion and analysis

Since the metallization processes are identical for all of the samples, the difference in via resistance must arise from the difference in interface nature. There are five factors which may affect the via resistance: (i) the formation of CF_x polymer; (ii) the formation of Al–F compound (AlF_x) or Al–O compound (Al_2O_3); (iii) the clean of CF_x; (iv) the sputter-off of the AlF_x or Al_2O_3; (v) the re-deposition of SiO_2 due to sputter clean. Several papers had reported that the typical post-etch cleaning process (O_2 ash + solvent rinse) can effectively remove the CF_x layer. In this work, no polymer residues were ever observed by SEM inspection after post-etch cleaning process. Thus, the factors related to CF_x were ruled out at first.

Aoki et al., have recognized that AlF_x layer may be the major contamination at Al surface after via hole over etch. It is reported that the AlF_x layer is very difficult to be removed by the typical cleaning process and an ion sputtering must be used to remove the AlF_x layer. Fig. 8(a) and (b) shows the transmission electron microscopic (TEM) micrographs of 0.16 μm via etched by E1 and E2 recipe, respectively. The sputter time is 15 s and a 50 nm thick Ti wetting layer and a 120 nm thick cold Al layer were deposited on both samples. The TiN layer was etched through by E1 recipe and a damaged layer was observed at the via/M1 interface as indicated in Fig. 8(a). The TiN layer still remained and no damaged layer was observed for the E2 recipe etched via. Several samples were thinned for TEM inspection. It was confirmed that E1 recipe etched through TiN layer

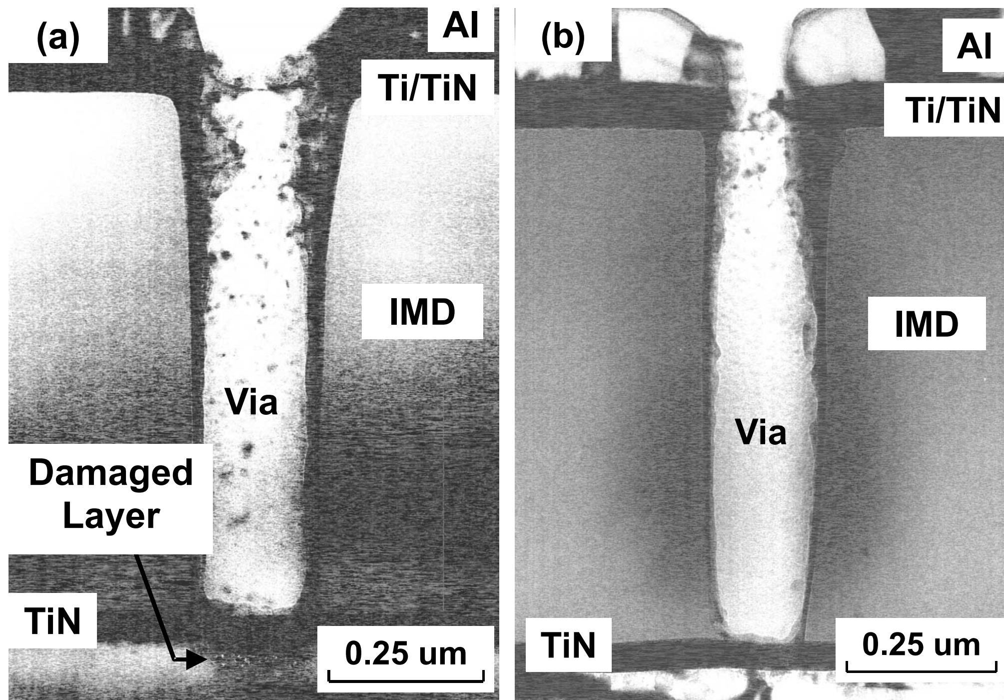

Fig. 8. The cross-sectional TEM micrographs of 0.16 μm via etched by (a) E1 recipe and (b) E2 recipe. Both samples experienced a 15 s sputter clean followed by a metal deposition of 50 nm thick Ti layer and 120 nm thick cold Al layer.

and left a damaged layer at via bottom. Fig. 9 shows the TEM micrograph of 0.38 μm via of sample E1S15. A damaged layer was also observed at the via/M1 interface. However, the damaged layer of 0.38 μm via is thinner than that of 0.16 μm via. Electron probe microanalysis (EPMA) was used to analyze the composition of the damaged layer. Fig. 10 shows the EPMA spectrum of the damaged layer of the 0.38 μm via. Fluorine signal was observed clearly and only relative a weak carbon signal was detected. The intensity of the carbon signal is close to the background signal. The EPMA spectrum of 0.16 μm via is similar to that of 0.38 μm via, i.e., fluorine but not carbon was detected. The observation of the fluorine signal and the lack of carbon signal indicates that the damaged layer consists of Al–F compound but not C–F polymer.

Based on the above structural and material analysis, the electrical results can be explained as follows. Since the over etch time of E1 recipe used in this work is sufficiently long to etch through the TiN layer of M1 at all via sizes, all of the E1 recipe etched samples have Al–F compound at via bottom. The apparent improvement of R_v by sputter clean as via size is larger than 0.34 μm implies the sputter clean can reduce the Al–F layer. This result is similar to those reported in previous [9,11].

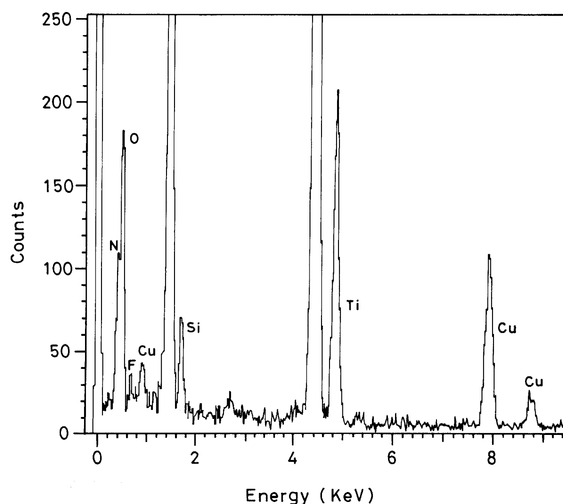

Fig. 10. The EPMA spectrum of the damaged layer at the bottom of the 0.38 μm via shown in Fig. 9.

However, as via size is smaller than 0.25 μm, the sputter clean almost does not affect R_v. It is postulated that the sputter yield degrades due to the increase of AR. The

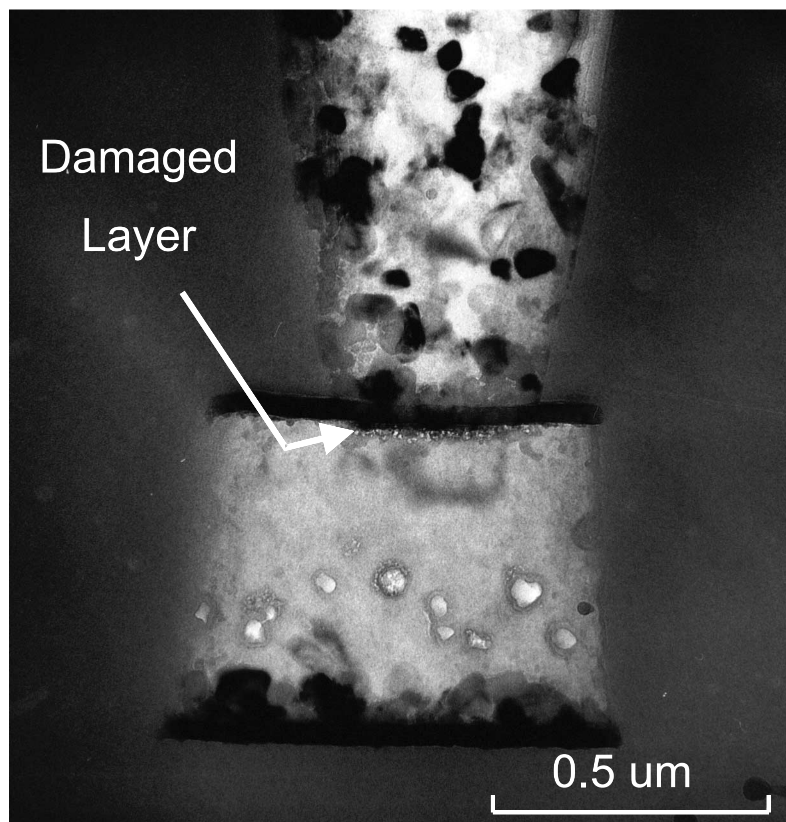

Fig. 9. The cross-sectional TEM micrograph of 0.38 μm via from sample E1S15.

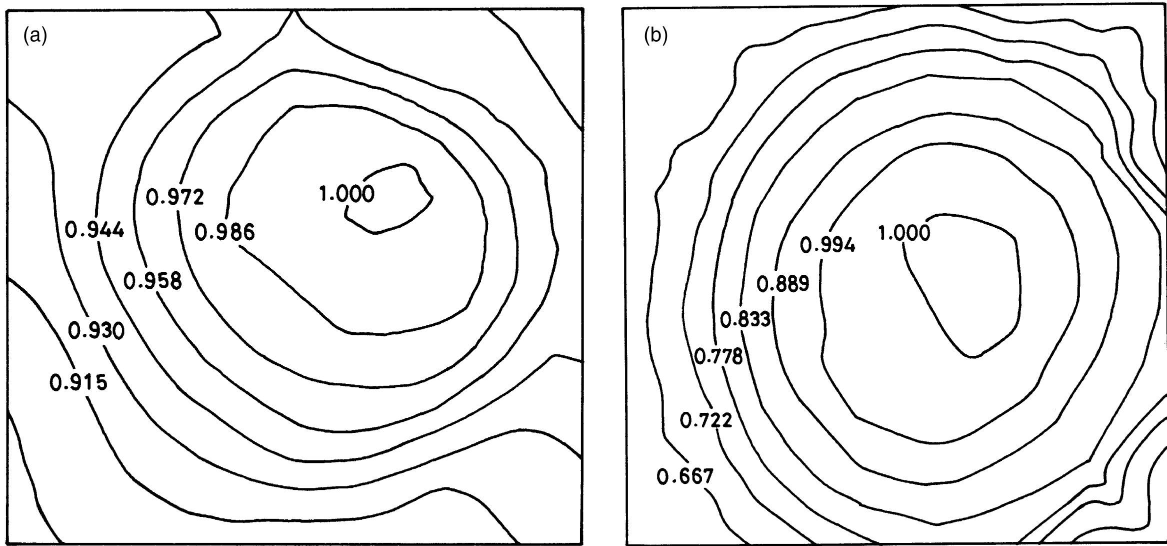

Fig. 11. The normalized wafer mapping of (a) oxide etch rate and (b) via resistance of 0.23 μm via of sample E1S15.

AlF_x layer cannot be removed effectively such that the benefit of sputter clean becomes diminished. In this case, the via resistance is dominated by the existence of AlF_x layer. Fig. 11 compares the wafer mapping of oxide etch rate Fig. 11(a) and the via resistance Fig. 11(b) of sample E1S15 with via size of 0.23 μm. The consistence of these two mappings make the following inference reasonable: higher etch rate results in longer over etch period which in turn results in more Al–F compound and higher via resistance. The damaged layer of 0.16 μm via is thicker than that of 0.38 μm via (as shown in Figs. 8(a) and 9) further supports the explanation.

The E2 recipe has a strong microloading effect. SEM inspection observed that the TiN layer was not etched through for via size smaller than 0.25 μm while it was etched through for via larger than 0.34 μm. The low R_v of E2 etched small vias (0.21–0.25 μm) without sputter clean (samples E2S0) are thus attributed to the clean interface due to lack of Al–F layer. The increase of R_v with the increase of sputter time is unexpected. It is speculated that although the TiN layer was not etched through during via etch, the remained thin TiN was sputtered off at the first several seconds and then some SiO_2 sputtered out from top corner of via was knocked-into M1 by Ar ions. This model can also explain the wafer mapping of via resistance. For the 0.21 μm via, sputter clean produced some high resistance vias. These high resistance vias are all located at the area of higher oxide etch rate. The larger the via size is, the thinner the TiN was remained after via etch. A slight sputter clean may break through the remained TiN and then knocked-in SiO_2 increases the via resistance. Therefore, the percentage of high resistance via increases with the increase of via size. For the 0.25 μm via, TiN was etched through at the region of the highest oxide etch rate. This results in some high resistance vias of sample E2S0 as shown in Fig. 4. Although no SiO_2 at via/M1 interface was visible by TEM inspection directly, the sputter-out of oxide is supported with the slightly rounded top corner of via as shown in Figs. 8 and 9. EPMA analysis was not able to detect the SiO_2 at the via/M1 interface because the IMD is also SiO_2.

Beyond 0.25 μm, TiN was totally removed during via etch. Since E2 recipe generates more Al–F compound than E2 does, the via resistance is higher and its distribution is broader for E2 recipe etched samples at each sputter time. There might be some CF_x residues remain in the 0.16 μm via hole after post-etch clean process because of its high AR. Again, E2 recipe generated more CF_x polymers than E1 recipe did, the yield loss is severer for E2 recipe etched sample. This also explains the apparent yield improvement by sputter clean as shown in Fig. 7.

5. Conclusion

In this work, the impact of interface nature on via resistance as via size is scaled down to 0.16 μm was studied. The AR dependent effect of sputter clean is reported for the first time. Polymer generated during via etch can be removed by typical post-etch clean process if the AR is lower than 4. For higher AR via hole, sputter clean may be needed. The optimum sputter condition depends on the via etch recipe. However, if tough compounds such as AlF_x are formed during via etch, it is

difficult to be removed by sputter clean when the AR is higher than 3.2 because the sputtering efficiency degrades at high AR. In this case, via resistance is increased and dominated by the AlF_x layer. On the other hand, the top corner and sidewall oxide of via hole may be sputtered out to the via bottom, which also increases the via resistance. This effect is more apparent at smaller via size.

According to these results, a via etch well stops on TiN layer and generates less CF_x polymer is strong recommended to obtain low resistance via. Otherwise, newly high-efficiency clean technology has to be developed. Thus, to control via etch process carefully becomes as important as to optimize pre-metal clean process.

The lowest via resistance of 0.16 μm via is about 5–8 Ω/via in this work. This value is still four times higher than the lowest Cu via resistance of the same diameter [12]. The higher via resistance of Al via obstruct Al via to be used in high performance circuits. However, before the maturity of Cu contamination control, Al via is an acceptable technology for memory circuits.

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