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Guest Editors' Introduction

This special issue includes nine (9) papers, which are extended versions of papers that received high scores when reviewed for SiPS99, the prestigious IEEE Workshop on the Design and Implementation of Signal Processing Systems, held in Taipei, Taiwan, ROC in October 1999. These papers report recent research spanning the algorithms, architectures, and applications for signal processing systems. All papers submitted to the special issue have been thoroughly reviewed and revised before acceptance.

The first paper, "Architecture Concepts for Multimedia Signal Processing," by Peter Pirch, Carsten Reuter, Jens Peter Wittenburg, Mark B. Kulaczewski and Hans-Joachim Stolberg, University Hannover, Germany, presents architectural concepts aimed at future multimedia processing schemes. As the increasing popularity of the multimedia signal processing, this paper discusses innovative architectural approaches that promise a more exhaustive exploration of parallelism and a more flexible utilization of processing resources.

The next two papers deal with DSP architectures and design methodology. It has been shown, in systems that involve multidimensional streams of signals such as images or video sequences, that the majority of the area and power cost is not due to the datapath or the controllers but due to the global communication and memory interactions. The former paper, "Memory Design and Exploration for Low Power, Embedded Systems," by Wen-Tsong Shiue and Chaitali Chakrabarti, Arizona State University, USA, describes a procedure to reduce the power consumption due to memory traffic. On the other hand, design for "reuse" is currently considered an important way for implementing complex DSP silicon hardware and reducing the time-to-market. The latter paper, "Design of Silicon IP Cores for Biorthogonal Wavelet Transforms," by Shahid Masud and John V McCanny, The Queen's University, Ireland, presents a methodology for rapid silicon design based on generic, scalable architectures for the forward and inverse wavelet filters.

The fourth paper, "A Methodology for Architecture Exploration of Heterogeneous Signal Processing Systems," by Paul Lieverse, Delft University of Technology, The Netherlands, presents a methodology, named SPADE, to distinguish between applications and architectures, and to use a trace-driven simulation technique for co-simulation of application model and architecture models.

The fifth paper and the sixth paper deal with the architecture for wireless applications. The fifth paper, "Finite Wordlength Analysis and Adaptive Decoding for Turbo/MAP Decoders," by Zhongfeng Wang, Hiroshi Suzuki and Keshab K. Parhi, University of Minnesota, Minneapolis, USA, discusses the very timely topic of Turbo-codes which are popular in the 3rd generation W-CDMA systems (IMT-2000) and thus require very low-cost and low-power decoder implementations. This paper was voted by the participants of SiPS99 to receive the Best Paper Award. The sixth paper, "Energy-Scalable Protocols for Battery-Operated Microsensor Networks," by Alice Wang, Wendi B. Heinzelman, Amit Sinha and Anantha P. Chandrakasan, MIT, USA, proposes techniques for low-power network protocols and data aggregation algorithms for wireless sensor networks, which can greatly improve environment monitoring for many civil and military applications.

The following paper, "Real-Time Software Video Codec with a Fast Adaptive Motion Vector Search," by Tatsuji Moriyoshi, NEC Corp. Japan, presents a fast adaptive motion estimation technique with dynamically changed search order in according with the motion of objects. The codec on a 450 MHz Pentium II processor can encode and decode 30 CIF frames in real-time.

The last two papers deal with architectures for audio decoding. The eighth paper, "MPEG-2 AAC 5.1 Channel Decoder Software for a Low-Power Embedded RISC Microprocessor," by Yuichiro Takamizawa, Kouhei Nadehara, Max Boegli, Masao Ikekawa, and Ichiro Kuroda, NEC Corp. Japan, presents fast processing methods for IMDCT. The Ninth paper, "A Cost-Effective Design for MPEG-2 Audio Decoder with Embedded RISC Core," by Tsung-

Han Tsai, Ren-Jr Wu, and Liang-Gee Chen, Fu Jen University, Taiwan, ROC, presents another effective method to implement MPEG-2 Audio Decoder with semi-ASIC design.

We would like to acknowledge all authors for submitting their extended papers and the reviewers for keeping up with the very tight schedule that allowed us to complete this special issue as planned in less than one year. We are grateful to Jennifer Evans for her invitation to organize a special issue dedicated to SiPS99. Special thanks to Kluwer Academic Publishers staff for helping us with the administration.

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