Thin Tunnel Oxide Grown on Silicon Substrate Pretreated by CF_4 Plasma

Jam Wem Lee, Tan Fu Lei, *Member, IEEE*, and Chung-Len Lee

***Abstract*—High tunneling current and large resistance against stress were the main issue of tunnel oxide for scaling down the operation voltage of EEPROMs. In this letter, thin-tunnel oxides grown on a CF_4 pretreated silicon substrate were prepared and investigated for the first time. The fabricated oxide has about three orders of tunneling current higher than that of control one; furthermore, the stress induced anomalous and low electric field leakage currents were greatly suppressed. The improvement could be contributed to F-incorporation in oxide. This type of oxide is suitable for fabricating low–voltage EEPROMs and less process complexity was added.**

***Index Terms*—Anomalous current, CF_4 fluorinated oxide, low-voltage EEPROM, plasma pretreatment, SILC, tunnel oxide.**

I. Introduction

FOR portable data assistant (PDA) systems, an EEPROM with high density and low power consumption was especially needed [1]. However, scaling voltage of a stacked gate EEPROM was strongly affected by capacitive coupling ratio of control gate to floating gate, silicon/silicon dioxide barrier height, stress induced leakage current (SILC), and anomalous leakage current of the tunnel oxides [2]–[4].

In order to lower the barrier height of silicon/silicon dioxide, many works were proposed [5]–[7]. Among them, rough silicon surfaces were needed and prepared by etching, oxidation or depositing a thin polysilicon film. Unfortunately, this approach of increasing the interface roughness will decrease the mobility of the devices. Therefore, the silicon dioxide with lower barrier height would be a good candidate to fabricate tunnel oxides of the EEPROMs.

The fluorinated oxides were investigated and found to have lower barrier height, especially for thin oxide [8]. Fluorinated oxides had been widely studied for their good resistance against ionized radiation and hot electron [9]–[12]; additionally, the nitride oxides grown on F-implanted silicon was found to be capable of suppressing anomalous leakage current [4]. In fabricating oxides, many methods were proposed, however, few can match the standard IC processes.

In this letter, CF_4 plasma, which is usually used as a reaction source in etching silicon and silicon dioxide, is used to pretreat silicon wafer in growing thin fluorinated oxides. This proposal is found to fabricate oxides not only with good SILC and anomalous current characteristics but also with a high tunneling current. These superior characteristics meet the requirements of the tunnel oxides without adding too much process complexity.

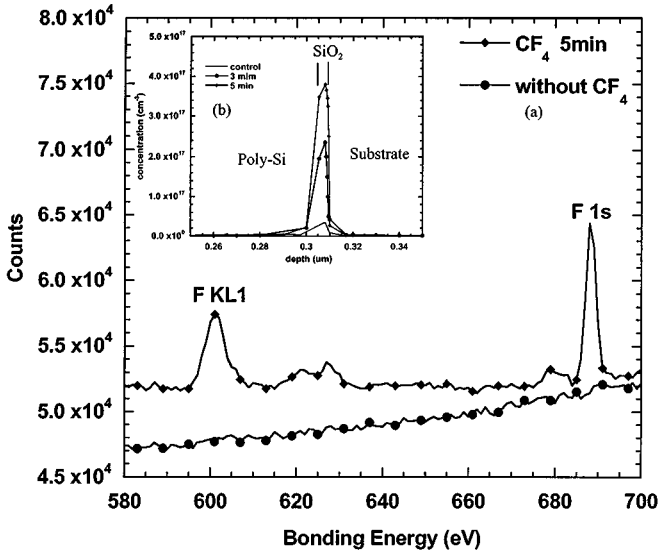

Fig. 1. (a) The XPS profiles of the CF_4 plasma treated by 10 W for 5 min. (b) SIMS profiles of F distributes in the control, 3 min, and 5 min samples.

II. Experiments

The n^+ polysilicon/oxide/P-type silicon MOS capacitors were fabricated and measured in this experiment. At first, p-type (100) wafers with sheet resistance of 15–20/square were RCA cleaned and then treated with CF_4 plasma at a temperature of 300 °C and a pressure of 600 mtorr in a plasma enhance chemical vapor deposition (PECVD) chamber. The power of the plasma was 10 W and the treatment time was 1 min, 2 min, 3 min, and 5 min, respectively. For comparison, the control sample was treated by RCA cleaning only, without any CF_4 plasma treatment.

The CF_4 plasma pretreated wafers were then grown with a thin oxide in an O_2 ambient at 900 °C for 5 min and then anneal in N_2O ambient at 900 °C for 5 min. Soon after the oxide growth, a 300-nm polysilicon film was deposited and doped with phosphorus to have a sheet resistance of 30/square. A 500-nm aluminum film was then deposited and, together with the n^+ polysilicon film, patterned to become the gate of the MOS capacitors. Finally, a 500- nm aluminum film was deposited on the backside of the wafers to act as the substrate contact.

Manuscript received June 18, 2001. This work was supported by the National Science Council, Taiwan, R.O.C. under Contracts NSC 89-2218-E-009-069 and NSC89-2215-E-009-095. The review of this letter was arranged by Editor A. Chatterjee.

The authors are with the Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: tflei@cc.nctu.edu.tw).

Publisher Item Identifier S 0741-3106(01)09569-6.

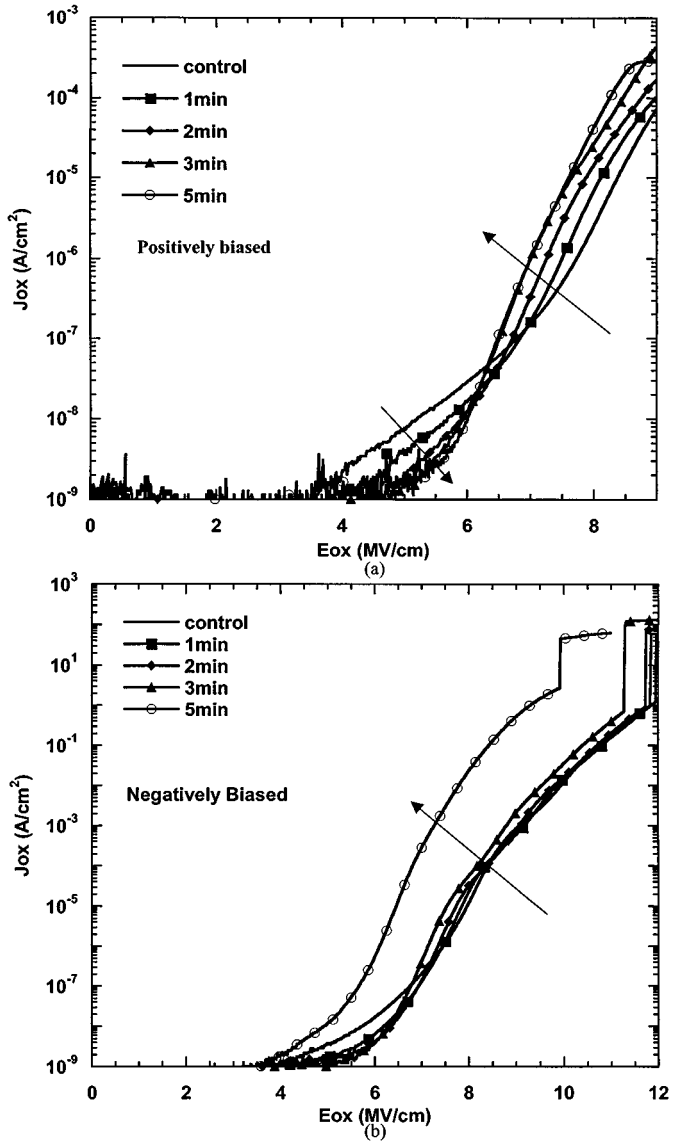

Fig. 2. (a) The positive and (b) the negative $J - E$ characteristics of the five samples. The 1 min, 2 min, 3 min, and 5 min samples were CF_4 plasma treated for 1 min, 2 min, 3 min, and 5 min, respectively.

The thickness of the oxides was determined by capacitance–voltage *(C-V)* measurement. In addition, current–voltage *(I-V)*, leakage, and reliability characteristics were measured by HP 4156B. The F incorporation was determined by using the SIMS and XPS analysis.

III. Results and Discussion

Fig. 1 shows (a) the XPS profiles of the silicon substrate treated by 10 W CF_4 plasma for 5 min, and (b) the SIMS profiles of F in the control, 3 min and 5 min samples. In the XPS profiles, it can be easily seen that strong signals of F bonds were detected. On the other hand, no F signals were detected in the control sample. In the SIMS profile, we can find that the 5 min sample has a much higher F incorporation than the control sample, by the way, the F concentration increased as the pretreatment time increased. The profiles also indicate that the F incorporates mainly in the oxides; this is superior to the F-implant method of which the high concentration of F can be incorporated in the channel region. The much higher F incorporation in the oxides could further explain the $J-E$ characteristics and the SILC shown in the Figs. 2 and 3. The profiles can also explain the slight increment in thickness of oxides because similar results were also found in the fluorinated oxides. In this work, the thickness of oxides is 5.0, 5.2, 5.4, 5.6, and 5.7 nm for the control, 1 min, 2 min, 3 min, and 5 min samples respectively.

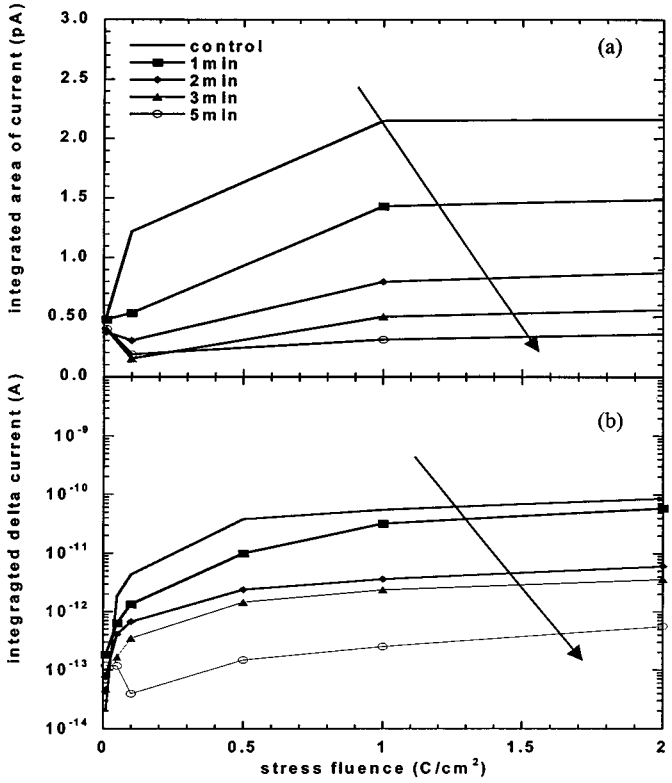

Fig. 3. The integration of the (a) anomalous and (b) incremental low electric field leakage currents under various stress fluence for all samples. The integration of (a) was done by summing the $I^*\Delta V$ from $V = 0.5$ to -0.5 V, and (b) was done by summing the $(I - I_0)^*\Delta V$ from $V = -0.5$ to -3.5 V. In the integration, V is the gate voltage, I is the gate current and the I_0 is the gate current in the fresh curves.

Fig. 2 shows (a) the positive and (b) the negative J–E characteristics of the five samples. The 1 min, 2 min, 3 min, and 5 min samples were CF_4 plasma treated for 1 min, 2 min, 3 min, and 5 min respectively. It can be seen that the tunneling current of the oxides is increased as the treatment time increases, especially for the 5 min sample with gate being negative biased. This sample has about three orders higher tunneling current than that of the control sample. Additionally, we can also find that when the gate was positively biased, the leakage current at lower electric field (3–6 MV) region was decreased with the increment of plasma treatment time. The improvement could be attributed to the F-incorporation in the oxides. Since higher F incorporation could reduce the defects and the dangling bonds in the oxides [4], [13], [14]; therefore, the leakage current at the low electric field regime is suppressed. Additionally, the barrier height of the oxide is also lowered [8] and a higher tunneling current will be observed.

Fig. 3 shows the integration of the (a) anomalous current and (b) incremental low electric field leakage currents under various

stress fluence for all the samples. The integration of (a) was done by summing the $I^*\Delta V$ from $V = 0.5$ to -0.5 V, and (b) was done by summing the $(I - I_0)^*\Delta V$ from $V = -0.5$ to -3.5 V. In the integration, V is the gate voltage, I is the gate current, and I_0 is the gate current in the fresh curves. From the Fig. 3(a) we can find that the anomalous leakage current of the control sample increases rapidly after constant current stress. On the other hand, the incremental anomalous leakage current of the CF_4 pretreated samples were largely suppressed. The improvement could be caused by the incorporation of F in the oxide interface since Ushiyama *et al.* [4] have demonstrated similar results. Fig. 3(b) indicates that the CF_4 samples have higher resistance against stress induced leakage current at low voltage regime (-0.5 to -3.5 V). This can be further contributed by higher F-incorporation. In fact, the higher tunneling current of the oxide should be another important factor when measuring wafers using constant current stress.

IV. Conclusion

In conclusion, fluorinated oxides using simple fabrication process have higher tunneling current but lower leakage current in addition to a higher resistance against both stress induced anomalous leakage and low electric field (3–6 MV/cm) leakage current. These outstanding properties are especially beneficial to fabricating low voltage EEPROMs.

References

[1] R. Versari, A. Pieracci, D. Morigi, and B. Ricco, "Fast tunneling programming memories," *IEEE Trans. Electron Devices*, vol. 47, p. 1297–1299, June 2000.

[2] E. F. Runnion, S. M. Gladstone, R. S. Scott, D. J. Dumin, L. Lie, and Mitros, "Limitations on oxide thicknesses in flash EEPROM applications," in *J. Reliab. Physics Symp., 1996. 34th Ann. Proc., IEEE Int.*, 1996, pp. 93–99.

[3] S. Lai, "Tunnel oxide and ETOX/sup TM/flash scaling limitation," in *Nonvolatile Memory Tech. Conf., 1998 Procs. Seventh Biennial IEEE*, 1998, pp. 6–7.

[4] M. Ushiyama, A. Satoh, and H. Kume, "Suppression of anomalous leakage current in tunnel oxides by fluorine implantation to realize highly reliable flash memory," in *Symp. VLSI Tech., 1999. Dig. of Tech. Papers.*, 1999, pp. 23–24.

[5] S. L. Wu, D. M. Chiao, C. L. Lee, and T. F. Lei, "Characterization of thin textured tunnel oxide prepared by thermal oxidation of thin polysilicon film on silicon," *IEEE Trans. Electron Devices*, vol. 43, pp. 287–294, Feb. 1996.

[6] K.-M. Chang, C.H. Li, B.-S. Sheih, J.-Y. Yang, S.-W. Wang, and T.-H. Yeh, "A new simple and reliable method to form a textured Si surface for the fabrication of a tunnel oxide film," *IEEE Electron Device Lett.*, vol. 19, pp. 145–147, May 1998.

[7] J. F. Buller, B. Bandyopadhyay, S. Garg, and N. Patel, "Improved EEPROM tunnel- and gate-oxide quality by integration of a low-temperature pre-tunnel-oxide RCA SC-1 clean," *IEEE Trans. Semiconduct. Manufact.*, vol. 9, pp. 471–476, Aug. 1996.

[8] G. Ghidini, D. Drera, and F. Maugain, "F contamination effects on intrinsic and extrinsic gate oxide reliability," in *Final Rep. Int. Integrated Reliab. Workshop*, 1995, pp. 92–97.

[9] G. Zhang, R. Yan, W. Gao, D. Ren, Y. Zhao, and Y. Hu, "Ionizing radiation effects of mobility in fluorinated NMOSFETS," in *4th Int. Conf. Solid-State and Integrated Circuit Tech.*, 1995, pp. 99–102.

[10] W.-S. Lu, J.-S. Chou, S.-C. Lee, and J.-G. Hwu, "Radiation hardness of fluorinated oxides prepared by liquid phase deposition method following rapid thermal oxidation," in *Int. Electron Devices and Mater. Symp.*, 1994, pp. 1-3-9–1-3-12.

[11] A. Balasinski, L. Vishnubhotla, T. P. Ma, H.-H. Tseng, and P. J. Tobin, "Fluorinated CMOSFET's fabricated on (100) and (111) Si substrates," in *1993 Int. Symp. VLSI Technol., Syst., and Applicat.*, 1993, pp. 95–99.

[12] G. Q. Lo, W. Ting, J. H. Ahn, D.-L. Kwong, and J. Kuehne, "Thin fluorinated gate dielectrics grown by rapid thermal processing in O_2 with diluted NF_3," *IEEE Trans. Electron Devices*, vol. 39, pp. 148–153, Jan. 1992.

[13] P. J. Wright and K. C. Sarawat, "The effect of fluorine in silicon dioxide gate dielectric," *IEEE Trans. Electron Devices*, vol. 36, pp. 879–889, May 1989.

[14] T. K. Nguyen, L. M. Landsberger, C. Jean, and V. Logiudice, "Effects of fluorine implants on induced charge components in gate-oxides under constant-current Fowler-Nordheim stress," *IEEE Trans. Electron Devices*, vol. 44, pp. 1432–1440, Sept. 1997.