A Programmable Pipelined Digital Differential Matched Filter for DSSS Receiver

Ching-Hung Chiou, Chao-Wang Huang, Kuei-Ann Wen, and Mau-Lin Wu

Abstract—A programmable pipelined digital differential matched filter (PDMF) implemented for a direct sequence spread spectrum receiver is proposed in this paper. To reduce the power consumption, the architecture PDMF is based on the synchronization combined PN code phase acquisition algorithm (Huang et al., 1999). Compared with the conventional PN code phase acquisition algorithm, the theoretical analysis result indicates that the PDMF acquires both power efficient and preferable detection. Depending on different applications, programmability allows the PDMF to implement 3-tap, 5-tap, or 11-tap Barker codes with the same hardware but different precisions for each tap coefficient. For short tap Baker codes, the architecture could adopt more precision on each tap coefficient to resist the channel noise. Simulation results also show that there are fewer errors of high sample precision with the same tape.

Index Terms—Baker code, DSSS, low power.

I. INTRODUCTION

IRECT sequence spread spectrum communication systems have been attached so much importance for possessing relatively more desirable features than the other communication schemes. Some of those fascinating attractions are multipath rejection, antijamming capability, low probability of interception, and so on [1]–[3]. However, in spread spectrum system design, the initial synchronization of the spreading waveforms is very significant. The uncertainty in the estimated propagation delay $\hat{\tau}_d$ contributes to a large number of symbols of code phase uncertainty, while the Doppler effect and the instability of the oscillator result in frequency uncertainty also have to be resolved. Among many PN code phase acquisition algorithms, the matched filter is regarded to be a very efficient measure to acquire the initial synchronization [4]. However, when the number of stages of a conventional digital matched filter (CDMF) increases, the amount of multiplications and accumulations will be greatly increased. In order to improve on such a major shortcoming of the CDMF, a modified structure, differential digital matched filter (DDMF), was proposed to reduce the complexity of spread spectrum correlators [5]–[7]. The numerical complexity of DDMF, measured as accumulate and multiply operations, was found to approach half of that of the CDMF.

In this paper, a programmable-pipelined digital differential matched filter (PDMF) based on the synchronization combined PN code phase acquisition algorithm (SCA) [9] is proposed

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TABLE I VALUES OF m AND t

$\overline{}$	Threshold Level: t						
\ [S	SCA				
	Conventional	$P_{\scriptscriptstyle D}$	P_{FA}				
m = 3	1.75	2.9	0.25				
m = 5	2.25	4.75	0.25				
m =11	7	10	0				

and presented. This newly developed programmable architecture can be programmed, from 12-bit precision for 3-tap Baker codes down to 4-bit precision for 11-tap Barker codes, which depends on the applications. And, using the SCA algorithm enables the PDMF to perform a better power efficiency than that of the CDMF. The programmable architecture of the PDMF is described in detail in Section II, and the numerical results of the PDMF are given in Section III in comparison with those of a CDMF. The comparisons between PDMF, CDMF, DDMF [6], and low complexity correlator [7] are shown and discussed in Section IV.

II. SCA ALGORITHM

The algorithm adopted for the programmable PDMF is the SCA [9]. Compared with the conventional PN code phase acquisition algorithm, SCA has a higher detection probability and a lower false alarm rate. Following is a brief description of the SCA algorithm.

- 1) Assume that there exists a set of Ω partitioned into two states of nature, ω_1 and ω_2 , with $P(\omega_1|_{X=1}) = P_1$ and $P(\omega_2|_{X=-1}) = P_2$. One of these two states prevails as the observations are made, and that prevailing state is unknown to observers.
- 2) Assume that the channel is an additive white Gaussian noise (AWGN) channel with the probability density function (pdf) of $N(0, \sigma^2)$. Consequently, the pdf of the received signal is either $Y_1 = X_1|_{X=1} + N(0, \sigma^2) = N(1, \sigma^2)$ or $Y_2 = X_2|_{X=-1} + N(0, \sigma^2) = N(-1, \sigma^2)$.
- $N(1, \sigma^2)$ or $Y_2 = X_2|_{X=-1} + N(0, \sigma^2) = N(-1, \sigma^2)$. 3) As the source data is X_i and it is spread into m-tuples $\vec{X}_i = (x_0, x_1, \dots, x_{m-1})$, then a real vector data $\vec{Y}_i = (y_0, y_1, \dots, y_{m-1}) = (x_0, x_1, \dots, x_{m-1}) + (n_0, n_1, \dots, n_{m-1})$, which is probabilistic in nature and represents a manifestation of the state of nature, can be obtained.
- 4) The cross-correlation function of the PN code phase synchronizer is depicted as $C = \vec{Y}_i \cdot \vec{B}$.
- 5) If the phase of the PN code were synchronized, the conditional pdf of the autocorrelation function becomes

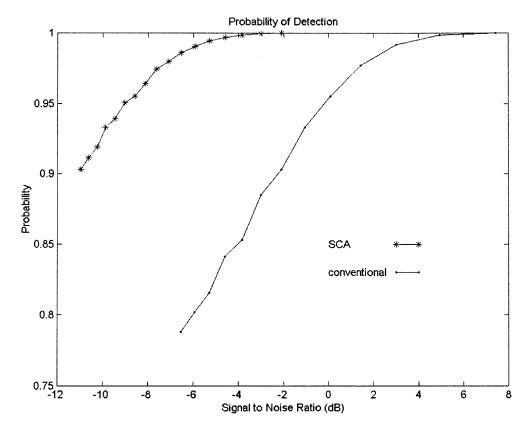


Fig. 1. Detection probability comparison.

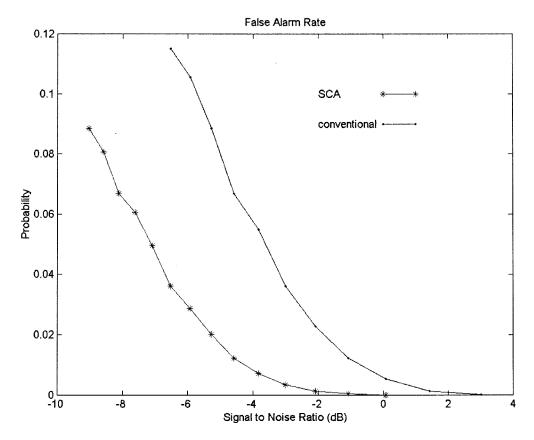


Fig. 2. False alarm rate comparison.

 $N(m,m\sigma^2)$ given ω_1 or $N(-m,m\sigma^2)$ given ω_2 . If not synchronized, the pdf of the autocorrelation function of

the PN code phase synchronizer becomes $N(1,\,m\sigma^2)$ or $N(-1,\,m\sigma^2).$

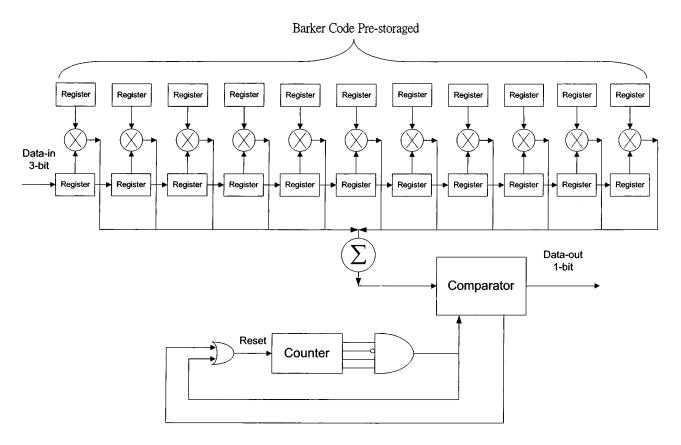


Fig. 3. The architecture of the SCA for 11-tap Barker codes with a 3-bit A/D.

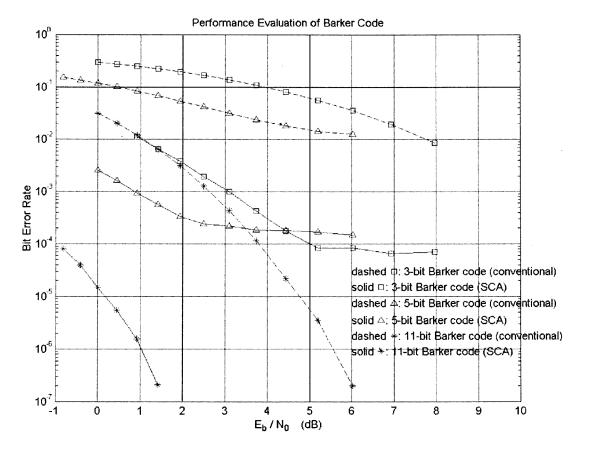


Fig. 4. Power efficiency comparison of SCA and conventional algorithm.

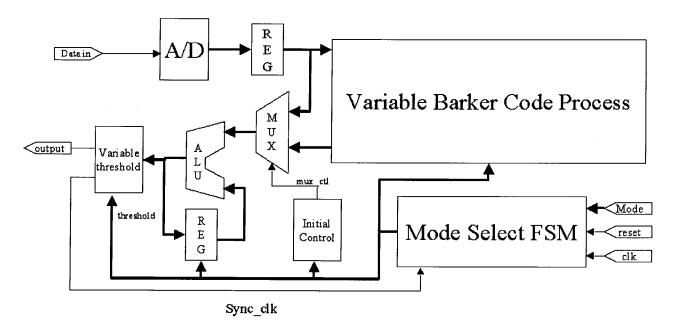


Fig. 5. Block diagram of the architecture of PDMF.

- 6) Assume that the decision function of the PN code phase synchronizer is $d(\vec{Y})$, whose domain is the set of all real valued m-tuples and range is Ω .
- 7) Define $P(\hat{\omega}_i, \, \omega_j) \equiv P[d(\overline{Y}) = \omega_i, \, \omega_j]$ and $P(\hat{\omega}_i, \, \omega_j)$ is the joint probability that the state of nature is ω_j . Based on \overline{Y} and the function d(.), the estimated or perceived state of nature is ω_i . If i=j, the decision is correct; if $i\neq j$, then an error happens and a penalty (cost) is incurred [10].

A. Detection Probability Analysis

Assume that $P_1 = P_2 = 0.5$, as analyzed in [9]; if the PN code phase were synchronized, the detection probability for PN code phase acquisition algorithm with m-tuples and a threshold t is given as

$$P_D = \frac{1}{2} \left[\int_t^{\infty} \frac{1}{\sqrt{2\pi \cdot m\sigma^2}} e^{-((x-m)^2/2 \cdot m\sigma^2)} + \int_{-\infty}^{-t} \frac{1}{\sqrt{2\pi \cdot m\sigma^2}} e^{-((x+m)^2/2 \cdot m\sigma^2)} \right]$$
$$= 1 - Q\left(\frac{m-t}{\sqrt{m \cdot \sigma^2}}\right). \tag{1}$$

B. False Alarm Rate Analysis

If the PN code phase were not synchronized, the false alarm rate for rapid PN code phase acquisition algorithm with m-tuples and a threshold t would be

$$P_{FA} = \frac{1}{2} \left[\int_{t}^{\infty} \frac{1}{\sqrt{2\pi \cdot m\sigma^2}} e^{-(x-1)^2/2 \cdot m\sigma^2} dx + \int_{-\infty}^{-t} \frac{1}{\sqrt{2\pi \cdot m\sigma^2}} e^{-(x+1)^2/2 \cdot m\sigma^2} dx \right]$$
$$= Q\left(\frac{t-1}{\sqrt{m \cdot \sigma^2}}\right). \tag{2}$$

TABLE II BARKER CODES

3-tap (a_3, a_2, a_1)	+,+,-
5-tap	+,+,+,-,+
$(a_5, a_4, a_3, a_2, a_1)$	
11-tap	+,+,+,-,-,
$(a_{11}, a_{10}, a_{9}, a_{8}, a_{7},)$	-,+,-,-,+,-
$(a_6, a_5, a_4, a_3, a_2, a_1)$	

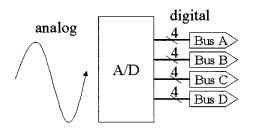
TABLE III COEFFICIENTS OF THE PDMF

3-tap coefficient	1,0,-2,1
$\begin{pmatrix} a_3, a_2 - a_3, \\ a_1 - a_2, -a_1 \end{pmatrix}$	$\left(b_{4}^{3},b_{3}^{3},b_{2}^{3},b_{1}^{3}\right)$
5-tap coefficient	1,0,0,-2,2,-1
$(a_5, a_4 - a_5, a_3 - a_4,)$	$\left(b_6^5,b_5^5,b_4^5,\right)$
$(a_2 - a_3, a_1 - a_2, -a_1)$	$\left(b_3^5,b_2^5,b_1^5\right)$
11-tap coefficient	1,0,0,-2,0,0,
$\left(a_{11}, a_{10} - a_{11}, a_{9} - a_{10},\right)$	2,-2,0,,2,-2,1
$a_8 - a_9, a_7 - a_8, a_6 - a_7,$	$(b_{12}^{11},b_{11}^{11},b_{10}^{11},)$
$a_5 - a_6, a_4 - a_5, a_3 - a_4,$	$b_9^{11}, b_8^{11}, b_7^{11},$
$\left(a_2-a_3,a_1-a_2,-a_1\right)$	$b_6^{11}, b_5^{11}, b_4^{11},$
	$\left(b_3^{11},b_2^{11},b_1^{11}\right)$

The values of code-length m and threshold level t are given in Table I.

The detection probability and false alarm rate of SCA for 11-tap Barker codes ($\vec{B}=(1,-1,1,1,-1,1,1,1,-1,-1,-1,-1)$), for example, are given as follows:

$$P_{D,SCA} = 1 - Q\left(\frac{11}{\sqrt{11 \cdot \sigma^2}}\right) \tag{3}$$



If (mode=3) then { {A/D is 16 bit}; Bus A=A/D[3:0]; Bus B=A/D[7:4]; Bus C=A/D[11:8]; Bus D=A/D[15:12] } Else if (mode=5) then { {A/D is 8 bit}; Bus A=A/D[3:0]; Bus B=A/D[7:4]; Bus C=A/D[3:0]; Bus D=A/D[7:4] } Else if (mode=11) then { {A/D is 4 bit}; Bus A=A/D[3:0]; Bus B=A/D[3:0]; Bus C=A/D[3:0]; Bus D=A/D[3:0];

Fig. 6. Block diagram and behavior of A/D converter.

$$P_{FA,SCA} = Q\left(\frac{9}{\sqrt{11 \cdot \sigma^2}}\right). \tag{4}$$

Figs. 1 and 2 illustrate the detection probability and false alarm rate of SCA with 11-tap Barker codes compared with the conventional algorithm.

The architecture of SCA for 11-tap Barker codes with a 3-bit A/D converter [9] is illustrated in Fig. 3. The incoming signal was sampled and quantized into eight levels, (4, 3, 2, 1, -1, -2, -3, -4), convenient for code phase acquisition and storage in the 11 shift registers. Thus, after being multiplied with the prestorage PN code and cumulated, the cross-correlation value of the incoming signal and PN code will be between 44 and -44. The threshold level was set to ≥ 24 or ≤ -24 for a conventional PN code phase acquisition algorithm and > 36 or < -36 for the SCA. If the clock of the SCA counts to 11 and the cross-correlation value is between 36 and -36, the clock will be reset and the threshold level will be adjusted to 0.

The power efficiency of the SCA and the conventional algorithm is illustrated in Fig. 4. In this figure, it can be observed that the bit–error rate (BER) decreases as a result of the length of the Barker code increase. The application of the SCA algorithm can improve the power efficiency of the conventional algorithm and the range of improvement differs with the length of the Barker code. For example, the SCA can reform the BER of 3-tap and 5-tap Barker codes in an order of two. However, for 11-tap Barker codes, the SCA performs 4~5 dB better than the conventional algorithm.

III. ARCHITECTURE OF PDMF

According to the CDMF, the result of the direct-form finite impulse filter (FIR) configuration could be expressed as follows:

$$f_{C, n-1} = a_N x_0 + a_{N-1} x_1 + \dots + a_2 x_{N-2} + a_1 x_{N-1}$$
 (5)

$$f_{C,n} = a_N x_1 + a_{N-1} x_2 + \dots + a_2 x_{N-1} + a_1 x_N.$$
 (6)

The N indicates the length of the PN code, a_i is the PN code coefficient, and x_i is the received signal. To reduce the number of multiplications and summations, a differential PN code scheme was proposed in [6]. The expression of the pipeline digital differential match filter can be described as follows:

$$f_{D,n} = f_{C,n} - f_{C,n-1} + f_{D,n-1}$$

$$= b_{N+1}x_0 + b_Nx_1 + \dots + b_2x_{N-1} + b_1x_N + f_{D,n-1}$$

$$= -a_Nx_0 + (a_N - a_{N-1})x_1 + (a_{N-1} - a_{N-2})x_2$$

$$+\cdots + (a_2 - a_1) x_{N-1} + a_1 x_N + f_{C, n-1}$$

where a_i are either 1 or -1 ,
 $b_i = a_i = a_{i-1}$ are either 2, -2 , or 0
except b_1 and b_{N+1} . (7)

For the coefficient 0, there is no demand for multiplication. Therefore, the switching activity of the multiplier could be minimized, and the dynamic power dissipation of the multiplier would also be reduced.

In order to figure out the synchronized problem and to minimize the power consumption, a new architecture PDMF using the SCA algorithm was proposed. Besides using a differential PN code coefficient number to minimize the switch activity of those multipliers, the architecture also applies the strategy to share the same hardware for processing different PN codes. In Table II, the well-known Barker code with 3-, 5-, and 11-taps is listed. After differential processing, the entire coefficients for the PDMF were acquired and have been listed in Tables II and III.

A. Block Diagram of PDMF

According the measure described in the previous paragraphs, the complete function block of the proposed PDMF architecture has been developed and illustrated in Fig. 5, which processes differential 3-tap, 5-tap, and 11-tap Barker codes in the same equipment. The system architecture of the present architecture consists of an A/D unit, a variable barker code processor, a variable threshold unit, an initial control unit, a mode select FSM unit, and some random logic units. In order to provide a better illustration of the mechanism, the whole block was decomposed into many subblocks and a more detailed operation is presented in the figures.

Fig. 6 shows block diagram and the behavior of an A/D converter. In the application of 3-tap Baker codes, the incoming signal would be sampled and quantized into 16 bits. In that case, the register latches the result and passes it to the FIR filter for further processing. However, for 5-tap Baker codes, the A/D converter will quantize the signal into 8 bits and allocate it into Bus BA and Bus DC. With the same method, Bus DCBA carries the same 4-bit quantized signal for 11-tap Baker codes processing. Basically speaking, the "initial control" block is used to look up the initial value from the item $f_c(T-1)$ from (5). When the incoming data is fed into the input port, the control signal mux_ctl will go low to start up the input data accumulation. The control signal mul_ctl will go high right after the value of $f_c(T-1)$ reached the Baker code tap length, and the data input will go on but be fed from the Variable Baker Codes

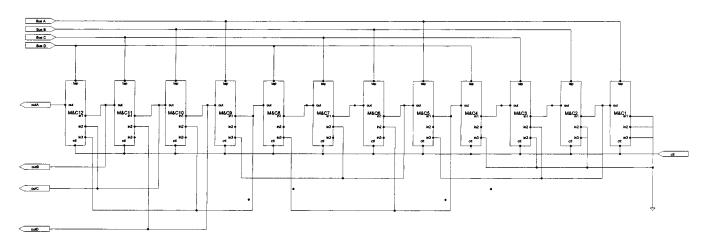


Fig. 7. Circuit design of Variable Barker Code process.

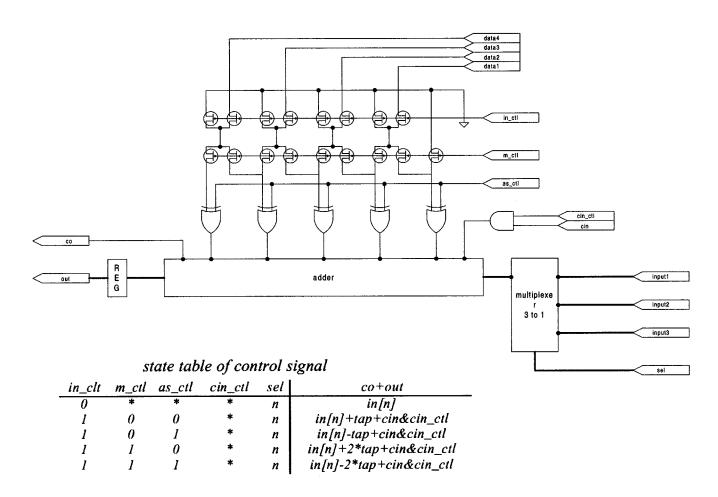


Fig. 8. Circuit design and state table for M&C unit of 0, 1, -1, -2, 2.

Process block instead of directly from the register. The Mode Select FSM unit based on the SCA algorithm is to generate the proper threshold value for the Variable Threshold unit. With the

application of this mechanism, it will reduce the synchronization time of the correlator and also lessen the power consumption.

Coefficient Tap	B ₁₁	B ₁₀	B ₉	B ₈	B_7	B ₆	B ₅	B_4	B ₃	B ₂	B ₁	B ₀
Sequence 11	b ₁₂	b ₁₁	b ₁₀	b ₉ 11	b ₈ ¹¹	b ₇ ¹¹	b ₆ ¹¹	b ₅ ¹¹	b ₄ ¹¹	b ₃ 11	b_2^{11}	b _i ii
	1	0	0	-2	0	0	2	-2	0	2	-2	1
Sequence 5	b ₆ 5	b_6^5	b_5^5	b ₅	b_4^5	b_4^5	b_3^5	b_{3}^{5}	b_2^5	b_2^5	b ₁ 5	b_1^5
	1	1	0	0	0	0	-2	-2	2	2	1	1
Sequence 3	a_3^3	a_3^3	a_{3}^{3}	a_3^3	a_2^3	a_2^3	a_2^3	a_2^3	a_1^3	a_1^3	a_1^3	a_1^3
	1	1	1	1	1	1	1	1	-1	-1	-1	-1

TABLE IV COEFFICIENT $B_0,\ B_1,\ B_2,\ B_3\cdots B_{11}$ for Each M&C Unit

B. Variable Barker Code Process Block

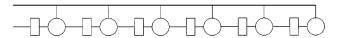
The variable barker code process block is the major block of the PDMF architecture shown in Fig. 7. The block is designed to despread the incoming sequences based on a programmable FIR filter equation with binary coefficient (0, -1, +1, -2, and +2) along with the 12-M&A (multiplier and adder) to complete the functionality. Manipulated by proper control signals, the 3-tap, 5-tap, or 11-tap correlation results can be well obtained.

In order to lessen the hardware, a specialized M&A unit must be developed to feature in taking advantage of multiplying simple coefficient and adding selected input. According to the type of Baker codes, the control activities follow the state table shown in Fig. 8. If the multiplication coefficient $b_i = 2$, the in_ctl and m_ctl are all set to logic 1 and as_ctl is set to logic 0. Otherwise, as_ctl is set to 0 for $b_i = -2$. In the same way, if $b_i = -1$, 1 or 0 could be implemented as the state table shown in Fig. 8. In addition to the coefficient control of multiplication, the sel signals manipulate the selection of the adder's summand. All of the observations infer that a binary ripple adder appears to be the better choice for hardware minimization.

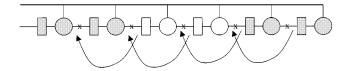
Twelve sets of basic M&C elements are applied to construct the variable Baker code processor. The previous stage M&C's co port was connected to the next stage M&C's cin port, and the Variable Barker Code Process block is constructed with a similar connection. For processing different coefficient taps, Table IV covers the reference values of coefficient $B_0, B_1, B_2, B_3 \cdots B_{11}$ for each M&C unit.

The operation of the M&C unit is illustrated in the diagrams in Fig. 9. As shown in Fig. 9(a), if the tap of the Barker codes is 11, the register of all M&C units could not be bypassed and the *sel* signals of all M&C units are set to logic 0. Thus, the total latency of the Variable Barker Code Processing is a 12-clock cycle. Fig. 9(b) shows another case for 5-tap Baker codes. In order to be the summand of the M&C3s, the M&C1's output must be connected to the multiplexer's input of the M&C3. Similarly, the output of M&C2 is connected to M&C4's multiplexer. Therefore, all of the signals at the control pin *cin_ctl* of the M&C unit are set to (0, 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, 1), then the total latency of the Variable Barker Code Processing is derived to be a 6-clock cycle. Fig. 9(c) shows the connecting method for 3-tap Baker codes. And, the total latency will reduce to 3-clock cycle with *cin_ctl* set to (0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1).

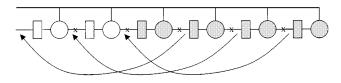
By the same method, some different spreading signals for different protocols such as 802.11, IS-95 could be combined into the same match filter to share the hardware. For more analysis,



(a) 11-tap Baker codes operation



(b) 5-tap Baker codes operation



(c) 3-tap Baker codes operation

Fig. 9. Different Baker code operation example.

the affect of the sampling precision has been performed. Fig. 10 displays the simulation results of 3-tap Baker codes root mean square (rms) errors between source data and received data (4 and 16 precision bits) on different E_b/N_0 . From the observation, a higher precision will reduce the error of received data from the simulation results. If the coefficient taps are 3, 16-bit precision would be good enough to resist noise disturbance. More coefficient tap is required to deal with high noise disturbance in the environment since variable spreading code takes advantage to get better channel efficiency and to resist noise.

IV. COMPARISON

In comparison with CDMF, DDMF [6], and low complexity correlator [7], the architecture of the PDMF has those features. First, the PDMF can reduce propagation delay of the summation compared with the CDMF. Second, the function of the PDMF could be reconfigured to change the precision bit width of the samples it can handle, from 16-bit precision for 3-tap Barker code, down to a 4-bit precision 11-tap Barker code. Although PDMFs have more propagation time compared with DDMF by 3-tap Baker codes, they will have the advantage of high precision to resist channel noise. These features make the PDMF more suitable for variable tap coefficient direct

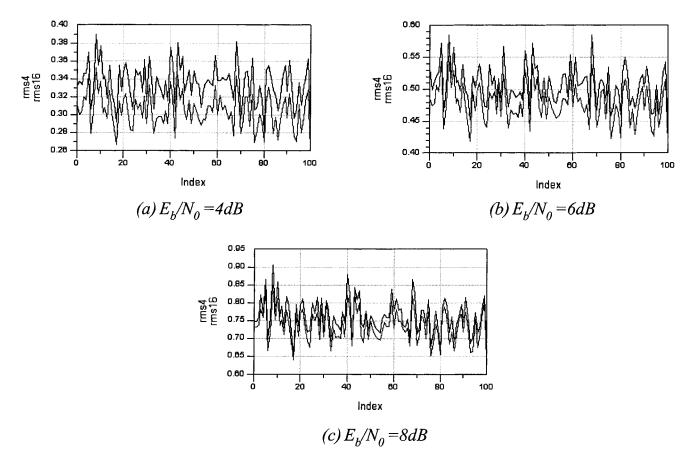


Fig. 10. Correlation error E_b/N_0 .

TABLE $\,\,$ V Comparisons Between PDMF CDMF, DDMF, and Low-Complexity Correlators

	PDMF	CDMF	DDMF	MC [7]	LCC [7]
Multiply	2 ⁿ⁻¹ +1	2 ⁿ -1	2 ⁿ⁻¹ +1	0	0
Add	2 ⁿ⁻¹ +1	2"-1	2 ⁿ⁻¹ +1	2 ⁿ⁻¹ +3	2 ⁿ⁻¹
Shift	o	o	0	1	o
Mux	n	О	0	О	o
Tap coefficient precision	$B_{bit}/2*B_{bit}/4*B_{bit}^{\{Note1\}}$	B _{bit}	B_{bit}	\mathcal{B}_{bit}	B _{bit}
Summation circuit signal delay	Tadder/2* Tadder/3* Tadder	n* T _{adder}	T_{adder}	$(n+1) * T_{adder} + T_{shift}$	(n-1)* T _{adder}

[Note1]: The field shows the precision bit for different tap coefficient, as 11-tap, 5-tap and 3-tap coefficient.

sequence spread spectrum (DSSS) communication systems. The comparisons between PDMF, CDMF, DDMF, and low complexity correlators are summarized in Table V.

V. CONCLUSION

A new architecture-PDMF-adopted SCA algorithm is proposed. The theoretical analysis indicates that the PDMF acquires both power efficient and preferable detection. In particular, the PDMF could operate different PN codes in the same hardware with different precision bits depending on the applications.

REFERENCES

- M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread Spectrum Communications*: Maryland Computer Science Press, 1985, vol. I-III.
- [2] R. L. Peterson, R. E. Ziemer, and D. E. Borth, *Introduction to Spread-Spectrum Communications*. Englewood Cliffs, NJ: Prentice Hall. 1995.
- [3] A. J. Viterbi, CDMA Principles of Spread Spectrum Communication. New York: Addison-Wesley, 1995.
- [4] Y. T. Su, "Rapid code acquisition algorithms employing matched filter," IEEE Trans. Commun., vol. COM-36, June 1988.
- [5] G. J. R. Povey and P. M. Grant, "Simplified matched filter receiver design for spread spectrum communication applications," *Electron. Commun. Eng. J.*, pp. 59–64, 1993.

- [6] W. C. Lin, K. C. Liu, and C. K. Wang, "Differential matched filter architecture for spread spectrum communication systems," *Electron. Lett.*, vol. 32, no. 17, pp. 1539–1540, 1996.
- [7] B. S. E. Tan and G. J. R. Povey, "Low complexity spread spectrum correlator," *Electron. Lett.*, vol. 33, no. 14, pp. 1204–1205, 1997.
- [8] D. Garrett and M. Stan, "Power reduction techniques for a spread spectrum based correlation," in *Proc. Int. Symp. Low Power Electronics and Design*, 1997.
- [9] C.-W. Huang, K.-A. Wen, and M.-L. Wu, "Synchronization combined PN code phase acquisition algorithm (SCA) for DSSS receiver," in *IEEE* 42nd MWSCAS Conf., 1999.
- [10] H. Stark and J. W. Woods, Probability, Random Process, and Estimation Theory for Engineers. Englewood Cliffs, NJ: Prentice-Hall, 1994
- [11] D. Wiggert, Codes for Error Control and Synchronization. New York: Artech, 1988.



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