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Surface-Processing-Enhanced Copper Diffusion into Fluorosilicate Glass

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This study investigated copper diffusion into processed fluorosilicate glass (FSG). It is observed that the surface process enhances the flatband voltage shift of the Cu/FSG/Si capacitor structure under bias-temperature stress. Secondary-ion mass spectroscopy analysis confirmed that the flatband voltage shift was due to Cu diffusion into the FSG film. Thermal desorption spectrometer analysis indicated that the surface damage layer took up more moisture. A surface-damage-layer-enhanced Cu ionization model was then proposed to explain the observation. The investigation concludes that the diffusion of Cu into FSG is strongly dependent on the surface condition of the FSG film. The proposed model also provides explanation for the inconsistent results reported in previous literature.
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With the progress of microelectronics technology, the feature size of the integrated circuit has scaled down rapidly. The smaller cross section of metal lines and the narrower space between the metal lines results in significant signal delay along multilevel interconnections.[1] It is well accepted that copper (Cu) and low dielectric constant (low-*k*) materials are inevitable at the sub-0.13 micrometer technology nodes.[2,3] Because Cu is a serious contamination source in silicon and most of the dielectrics, Cu lines must be sealed with suitable diffusion barriers, and Cu contamination during processing must be monitored and controlled.[4-7] Therefore, understanding of the mechanism of Cu diffusion into the dielectric is twofold. First, if the dielectric shows a good barrier property, diffusion barrier layers can be eliminated. The process can be simplified and the performance can be further improved. Second, if Cu can diffuse into the dielectric, the diffusion behavior must be understood such that contamination during processing can be monitored and controlled.

Many low-*k* materials have been proposed in the past ten years to reduce interconnect capacitance. Among them, fluorosilicate glass (FSG) is the most desirable because of its good thermal and chemical stability and its similarity to silicon dioxide (SiO_2). Hence, it can be readily integrated into the fabrication process.[8-11] Recently, Cu and FSG had been successfully integrated together.[12-14] However, only a few articles in the literature examined the diffusion behavior of Cu into FSG film.[15-19] Furthermore, quite different results were reported in those articles. It was even reported that Cu does not diffuse into FSG film under bias-temperature stress (BTS) at 200°C and 3.5 MV/cm for 30 min.[18]

The major drawback of the previous studies is that they all used as-deposited FSG film to examine the behavior of Cu diffusion in FSG film. This is not appropriate for the following reasons. In the damascene process, FSG film would experience several processes, such as dielectric etching, ion-sputtering clean before metal deposition, and chemical mechanical polish (CMP).[20] Figure 1 describes the major steps of the Cu dual-damascene process. After the first Cu-interconnect layer is finished, intermetal dielectric (IMD) Cu interconnect is deposited as the next layer (Fig. 1a). The sequential photolithography process and dielectric etch processes are performed twice to form the via holes and trenches in the IMD (Fig. 1b). After premetal deposition cleaning, barrier metal and Cu are then deposited in the via holes and trenches followed by a CMP process to finish the second layer Cu interconnect (Fig. 1c). Although the CMP process is employed to remove the Cu and barrier metal, the surface of FSG film is also polished during the overpolishing period. It is the behavior of the Cu diffusion into processed FSG film that affects the integration scheme and contamination control. Therefore, it is important to examine the effects of surface processing on the Cu/FSG interface reaction and the diffusion of Cu into FSG film, which is the focus of this study.

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Experimental

Simple metal-insulator-silicon (MIS) capacitor structures were used. The starting material is a (100)-oriented p-type silicon wafer. A 10 nm thick oxide was thermally grown before the FSG deposition to minimize the dielectric/silicon interface state density. FSG film of about 750 nm thickness was deposited in a high-density plasma chemical vapor deposition system. An inductively coupled plasma (ICP) source was used to generate plasma. The frequency and power of the radio-frequency (rf) generator for the top electrode were 200 MHz and 350 W, respectively. The rf power of the bottom electrode was turned off such that no ion bombardment occurred. It should be noted that substrate bias is not necessary for the damascene process because IMD is deposited on a CMP-planarized flat surface. The gases and corresponding flow rates were SiH_4 (17 sccm), SiF_4 (96 sccm), O_2 (190 sccm), and Ar (125 sccm). The chamber pressure was 15 mTorr during deposition.

Wafers were then divided into three categories: without surface processing (the as-deposited sample), argon ion sputtering in an ICP chamber for 1 min (the ICP sample), and CMP partial polish (the CMP sample). The ICP chamber is the pretreatment chamber of a clustered metal deposition system. Both the top and bottom powers were set at 300 W. This is the typical surface sputtering condition before metal deposition. The sputter rate of FSG film is about 200 nm/min. The CMP partial polish is to simulate the damage that arises during the overpolish period of the Cu CMP process. Clean

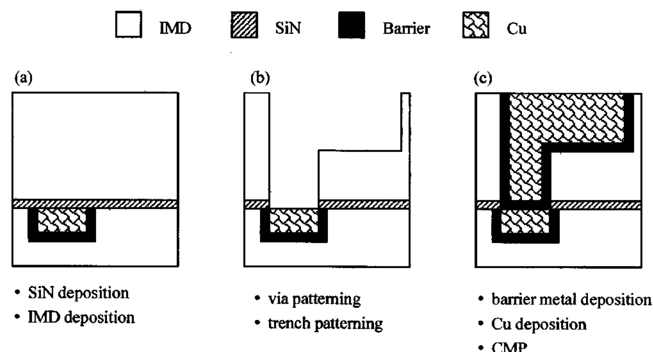

Figure 1. The major process steps of the dual-damascene process: (a) after IMD deposition, (b) after dual-damascence patterning, and (c) after Cu CMP.

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Table I. Process conditions of samples used in this work.

Sample ID	FSG surface processing	Gate material
Al-1	As-deposited	Al
Al-2	CMP	Al
Al-3	ICP	Al
Cu-1	As-deposited	Cu
Cu-2	CMP	Cu
Cu-3	ICP	Cu

pad and fresh slurry of model ECC-1403-1 were used to avoid Cu contamination from pad or slurry. The pad pressure was set at 2 psi and the polishing time is 50 s. The thickness of the FSG film was reduced by 200 nm after the ICP process and by 50 nm after the CMP process. Copper film of 500 nm thickness was then deposited in an ionized metal plasma chamber without substrate bias. A gate electrode was then patterned by the wet process. Samples with Al gate were also prepared as reference. The Al film was deposited in a typical high-vacuum dc sputter system.

After the metal gate patterning, a 30 nm thick SiN film was deposited to passivate the MIS structure. This layer is used to avoid moisture absorption in the MIS structure and to prevent the Cu gate from oxidation during high-temperature measurement. A 30 min anneal in N_2 ambient at 300°C, to reduce the process-induced charges in the dielectrics, finalized the sample processing. The temperature of this step is generally at 400°C, but in our experiment it is reduced to 300°C to avoid Cu diffusion into the FSG during annealing. Table I summarizes the process condition of the six samples.

The total dielectric thickness of each sample was measured by optical interference methodology. The high-frequency capacitance-voltage (HFCV) characteristics of all the samples were measured at 100 kHz. The dielectric constant of each sample was calculated from the measured capacitance at the accumulation mode and the total dielectric thickness was again determined by optical methodology. The flatband voltage (V_{FB}) was also extracted from the HFCV characteristic.

A BTS at +1 MV/cm and 200°C was performed to drive Cu into the FSG film. Secondary ion mass spectroscopy (SIMS) was employed to determine the distribution of Cu in the FSG film. To avoid surface roughness and knock-on effect during SIMS analysis, the capping SiN was removed by CF_4 plasma, and the metal gate was selectively removed by warm HNO_3 before SIMS analysis. Transmitted Fourier transform infrared (FTIR) spectroscopy and thermal desorption spectroscopy (TDS) were also used to analyze the properties of the surface-processed FSG film.

Results and Discussion

The fluorine concentration of the deposited FSG film determined by FTIR is about 4.6%. Table II lists the dielectric thickness, effective dielectric constant, and flatband voltage of the six samples. Although ICP and CMP treatments reduced the film thickness, the dielectric constant is unchanged. These results imply that the two surface processes did not change the composition and structure of the bulk of the FSG film. The magnitudes of V_{FB} of Al-gate devices are small. The slight difference between the samples may be due to surface process-induced damages or the fixed charges in the deposited FSG film.

Table II. Dielectric thickness, effective dielectric constant, and flatband voltage of all six samples.

	Al-1	Al-2	Al-3	Cu-1	Cu-2	Cu-3
Thickness (nm)	788	523	589	761	519	575
Dielectric constant	3.62	3.65	3.69	3.54	3.63	3.55
Flatband voltage (V)	−1.41	+0.57	−2.38	−18.95	−14.18	−27.59

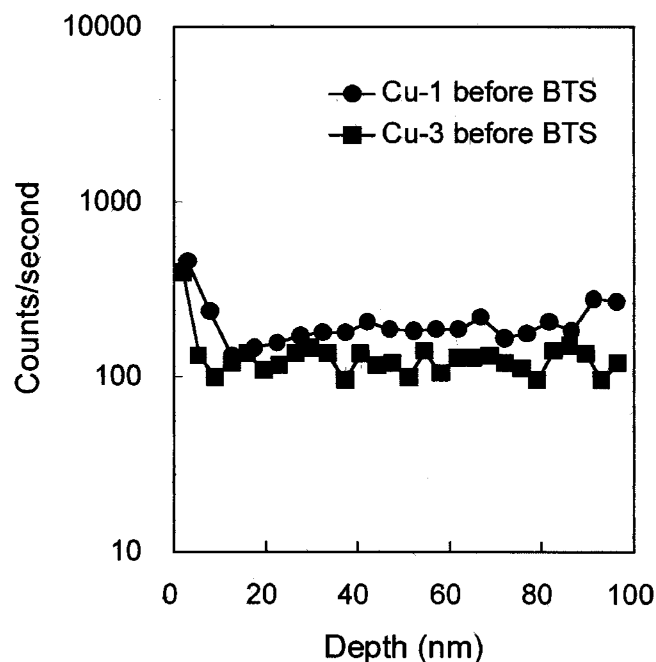

Figure 2. The SIMS depth profiles of Cu in FSG film of Cu-1 and Cu-3 samples just after sample preparation. The capping SiN and Cu gate have been removed.

An obvious V_{FB} shift toward the negative voltage axis is observed for the Cu-gate devices. One obvious hypothesis to explain this is Cu contamination during the Cu deposition or thermal processes. Figure 2 shows the SIMS depth profiles of Cu in the FSG film of the Cu-1 and Cu-3 samples. Depth profiles of the Cu-1 sample and the Cu-3 sample are almost identical, and only a small amount of Cu atoms were detected at the surface. These results indicated that the trace amount of Cu atoms comes from the residual Cu at the FSG surface after the stripping of the Cu gate. The concentration of typical mobile ions, such as Na+ and K+, were below the detection limit of SIMS analysis. Therefore, the negative V_{FB} is explained by the residual fixed charges in the FSG film generated during Cu deposition.[21] These charges are immobile and will not change at temperatures lower than the final annealing temperature of 300°C.

To drive Cu into FSG film, BTS tests were performed at +1 MV/cm and 200°C for various periods. To exclude the possible instability of the FSG film itself and contamination during the surface processing, Al-gate MIS capacitors were also measured. The flatband voltage shift (ΔV_{FB}) of the Al gate and the Cu gate samples after BTS were extracted and denoted $\Delta V_{FB,Al}$ and $\Delta V_{FB,Cu}$, respectively. The ΔV_{FB} relevant to Cu was then corrected by subtracting $\Delta V_{FB,Al}$ from $\Delta V_{FB,Cu}$. Figure 3 shows the corrected ΔV_{FB} of the three Cu-gate samples after various BTS periods. The $\Delta V_{FB,Al}$ of the Al-1, Al-2, and Al-3 samples are also shown in Fig. 3. A slightly positive shift of V_{FB} was observed on all three Al-gate samples, but the magnitudes of $\Delta V_{FB,Al}$ of the three samples were similar. This phenomenon is attributed to the slight instability of the FSG film itself.[18] A net negative ΔV_{FB} was observed on all three Cu-gate samples. Since the flatband voltage shift due to the instability of the FSG film and contamination other than Cu after the surface treatment had been subtracted, ΔV_{FB} should be relative to Cu only. It is obvious that the ICP sample (Cu-3) had the largest ΔV_{FB} and the as-deposited sample (Cu-1) had the least ΔV_{FB}. Furthermore, the rates of the V_{FB} shift of the three Cu gate samples are Cu-3, Cu-2, and Cu-1 in the sequence from high to low. These phenomena imply that Cu is more easily driven into surface-processed FSG films than

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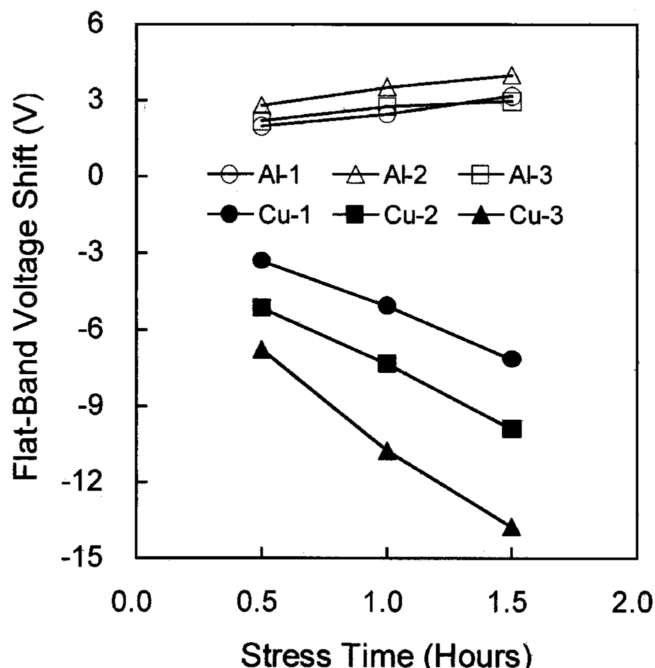


Figure 3. The corrected flatband voltage shifts of Cu-1, Cu-2, and Cu-3 samples after BTS treatment at +1 MV/cm and 200°C for various time periods. The flatband voltage shifts of Al-1, Al-2, and Al-3 samples were also shown.

driven into unprocessed FSG film. Since the ICP-sputtered sample (Cu-3) shows the most severe Cu diffusion, the following discussion and analysis focuses on the Cu-3 sample, with the Cu-1 sample as reference.

Figure 4 shows the SIMS depth profiles of Cu in the FSG film of the Cu-1 and Cu-3 samples before and after BTS for 30 min. Apparent Cu diffusion into the FSG film to a depth of about 40 nm was observed from the Cu-3 sample after BTS. According to the SIMS

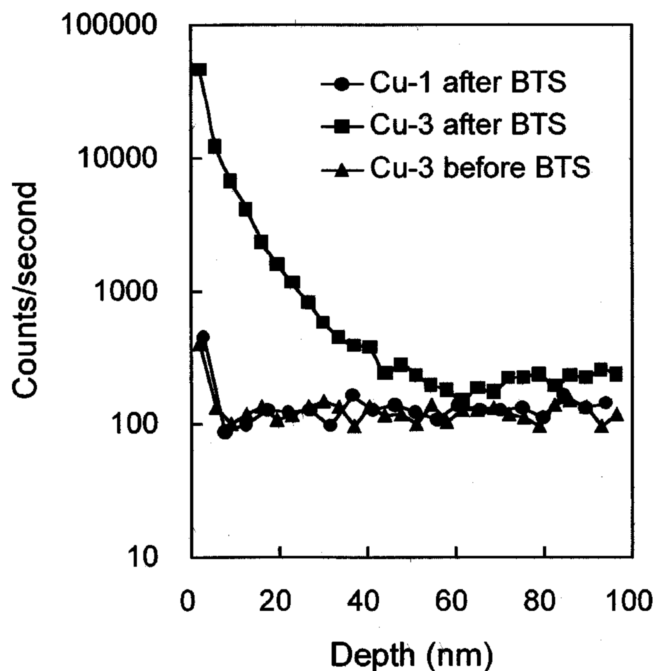
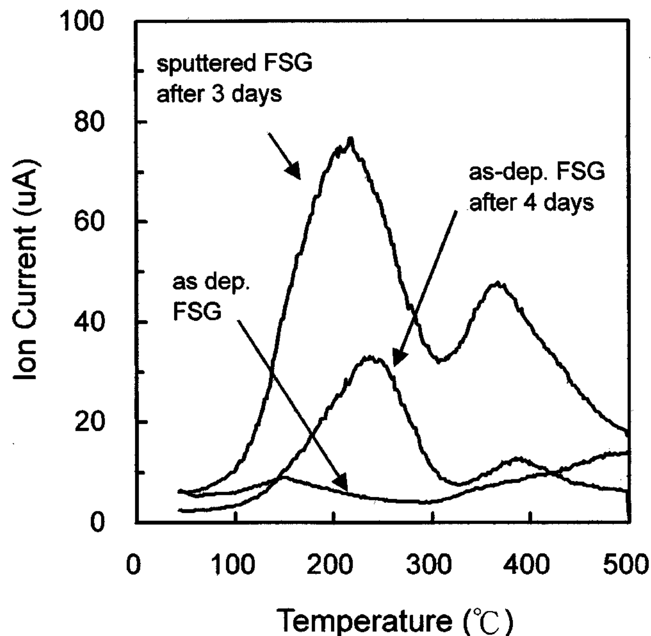


Figure 4. The SIMS depth profiles of Cu-1 and Cu-3 samples before and after BTS treatment at +1 MV/cm and 200°C for 30 min.



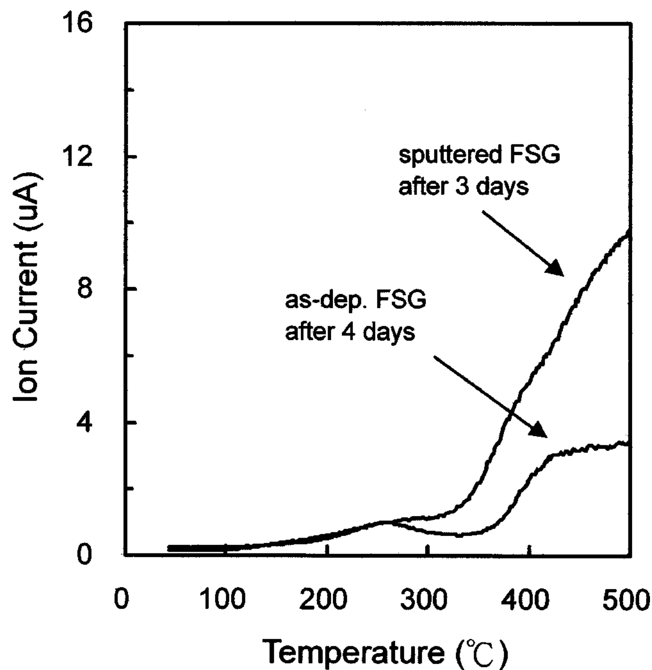


Figure 5. The (a) top H_2O and (b) bottom HF desorption spectra measured by TDS analysis on as-deposited FSG film, FSG film 4 days after deposition, and FSG film 3 days after surface sputtering.

analysis, it is definitely confirmed that the ΔV_{FB} observed after BTS is due to Cu diffusion into the FSG. The amount of Cu in the FSG film of the Cu-1 sample after BTS is much lower than that of the Cu-3 sample after BTS. This is consistent with the trend of V_{FB} shown in Fig. 3. Because the diffusion behavior of Cu in all FSG films should be the same deep inside the FSG films, the only difference among the FSG films is the surface characteristic for Cu diffusion through the Cu/FSG interface. It is thus suspected that the surface processing either increases the Cu ionization rate or reduces the diffusion barrier height and then enhances the Cu diffusion into the FSG film.

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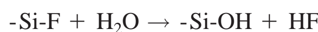
FTIR analysis was performed to clarify the FSG property after the surface processing. The transmitted absorption spectrum was detected and the spectra of as-deposited and surface-processed FSG films are identical. This confirms the previous postulation based on the dielectric constant and the SIMS profile of Cu that surface processes modify the properties of only the surface layer of FSG film. Figure 5a and b shows the H_2O and HF desorption spectra analyzed by TDS, respectively, of as-deposited FSG film, FSG film at 4 days after deposition, and FSG film at 3 days after ICP sputtering. The surface-sputtered FSG film shows the strongest H_2O desorption signal. This indicates that the surface sputtering enhances the moisture absorption of the FSG surface layer. It is also observed from Fig. 5b that HF desorption of the ICP-sputtered FSG film is more serious than that of the as-deposited FSG film. The controversial result that FTIR does not detect differences between as-deposited FSG film and ICP-sputtered FSG film may be attributed to the weak sensitivity of transmitted FTIR on the surface layer property change. In our experience, moisture uptake of as-deposited FSG film cannot be detected by FTIR until 2 weeks after deposition.

It has been reported that FSG film with a higher fluorine concentration has a lower dielectric constant but becomes more easily hygroscopic.[22,23] The FSG film after moisture absorption induces a hydrolysis reaction, which is represented by the following chemical formula[22-24]



$$\text{-Si-F} + H_2O \rightarrow \text{-Si-OH} + HF$$

The results obtained indicate that all FSG films have a probability of hydrolysis reaction occurrence for the Si-F bonds. The increase in the amount of Si-OH bonds slightly increases the dielectric constant for their low polarity. Moreover, the HF generated from Si-F bonds would damage other contacted films. Referring to the TDS result, it is postulated that the surface processing produces a surface-damaged layer. The enhanced moisture absorption at the surface-damaged layer causes increased hydrolysis reactions. There can be more Si-OH bonds and HF generation to enhance the copper ionization and erosion rate, and thus more copper ions are generated. This effect, combined with the structural damage due to the CMP and ion sputtering, caused the barrier height for Cu penetration into FSG to roll off and more Cu ions to be driven into FSG under the same BTS condition. Since the FSG film is very thick, it is possible that the increase of the dielectric constant at the surface-damaged layer does not affect the effective dielectric constant of the whole film.

Conclusions

Our investigation discovered that surface processing enhances Cu ion diffusion into FSG film. A surface-damage-layer-enhanced Cu ionization model was proposed. According to the model, the moisture uptake ability of the FSG film greatly affects the Cu diffusion behavior. This may explain the inconsistent reports in the published literature. Furthermore, even if the as-deposited FSG film shows good barrier properties against Cu diffusion, the damascene process produces a surface-damaged layer to enhance the Cu diffusion. Thus, in the Cu/FSG integration process, the processed FSG surface must be isolated from any Cu contamination. Therefore, a suitable barrier layer is still necessary because the FSG film has been processed before Cu deposition. Furthermore, it is strongly recommended that the surface-processed film, instead of as-deposited film, be used to evaluate the behavior of Cu diffusion into dielectric films.

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