Active Circuits Under Wire Bonding I/O Pads in 0.13 μm Eight-Level Cu Metal, FSG Low-K Inter-Metal Dielectric CMOS Technology$^+$

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***Abstract*—Active circuits in terms of ring oscillator are moved to the place under the wire bonding pads in 0.13 μm full eight-level copper metal complementary metal–oxide–semiconductor process with fluorinated silicate glass low-k inter-metal dielectric. The bond pad with the 12 KÅ thick aluminum metal film as a bonding mechanical stress buffer layer is deposited on the topmost copper metal layer. No noticeable degradations in gate delay or cycle time of ring oscillator are detected in a variety of test structures subjected to bonding mechanical stress and thermal cycling stress. This indicates that the underlying process technology may be reliable and manufacturable in placing active circuits under the bonding pads and thereby the die area utility is recovered fully. More evidence is created from transmission line pulsing experiments as well as capacitive-coupling experiments.**

***Index Terms*—Aluminum metal film, copper metal, fluorinated silicate glass, I/O bond pad, inter-metal dielectric, low-k, ring oscillator.**

I. Introduction

OWING to rapid progress made in complementary metal-oxide-semiconductor (CMOS) technology scaling, state-of-the-art integrated circuit design is significantly being driven toward high-density and high-complexity applications. The accompanying gate counts as large as more than 100 million gates per die are now requiring much more input/output (I/O) and power/ground pads in the range of 750 to 1000 pads for bonding wires to package. Consequently, significant growth in the number of bond pads leads to considerable consumption of active chip area and such situation would become worse in next generation nodes when the chip size stops scaling up according to ITRS roadmap [1]. To recover or improve active chip area utility, reducing bond pad pitch may be a solution; however, small bond pads mean much damage created under the mechanical stress inherent in the bonding force. This issue could be alleviated by moving circuits, such as part of internal circuitry and electrostatic discharge (ESD) protection, to the place under bonding pads [2]–[4]. However, design rules available for handling circuits under bonding pads (CBP) are very limited to date, due to the susceptibility of the underlying active circuits to bonding force. It is therefore urgent to devise technologies that would satisfy high-density requirements for advanced integrated circuit design while being able to resist bonding mechanical stress. To meet this goal, additional insulating films [2] and buffer metal layers [3], [4] were proposed. In this letter, we demonstrate the implementation of CBP in 0.13 μm full eight-layer Cu metal/fluorinated silicate glass (FSG) low-k inter-metal dielectric (IMD) CMOS process [5], achieved without accounting for the traditional treatments [2]–[4].

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II. Experimental

A 1.2-V, 201-stage unloaded inverter-type ring oscillator with aspect ratio of $W_{\rm p}/L_{\rm p} = 1.8\ \mu$m$/0.13\ \mu$m and $W_{\rm n}/L_{\rm n} = 1.2\ \mu$m$/0.13\ \mu$m was fabricated in 0.13 μm eight-level Cu metal/FSG low-k IMD CMOS process [5]. The gate oxide thickness was 2 nm. The size of the bond pad was $70\ \mu$m $\times$ $70\ \mu$m. Four kinds of ring oscillators were drawn

1) Structure A, the ring oscillator under the bond pad and single metal-eight layer;
2) Structure B, the ring oscillator under the bond-pad/metal-8/via-7/metal-7 layers;
3) Structure C, the ring oscillator under the bond-pad/metal-8/via-7/ metal-7/via-6/metal-6/via-5/metal-5 layers;
4) Standard structure, the ring oscillator without the bond pad or metal layers above it.

Note that two Cu-interconnect levels were used for the wiring of the ring oscillator underneath the pad structure. Aluminum metal film formed on the topmost copper metal film serves as a buffer layer against bonding stress and its thickness is the key to effective buffering. To determine the adequate thickness of the aluminum buffer layer prior to manufacturing, a bonding mechanical stress simulation was performed involving tensile stress (Sx), normal stress (Sz), shear stress (Sxz), arbitrary angle tensile and normal stress (Sl) and total equivalent shear stress (Seqv), all evaluated on the etching stop layers. Simulation results given in Fig. 1 revealed that all stresses are decreased with increasing aluminum metal film thickness, as expected and suggested a specific range of 12 to 16 KÅ for being free from damage during the bonding process at room temperature. However, 16 KÅ was too thick to etch in the undertaken manufacturing process. Thus, only 12 KÅ thick aluminum metal film was deposited on the 10 KÅ topmost copper metal layer for aluminum wire bonding with different bonding power and force. Al-wedge bonding, which produces more bonding stress than Au-ball bonding, was used. The bond

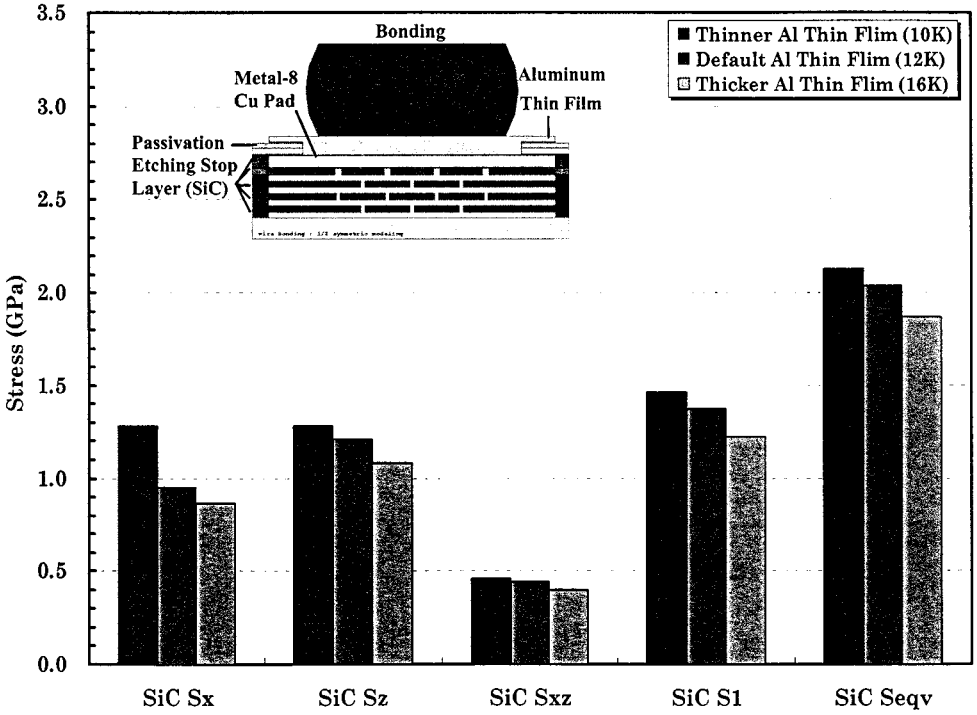

Fig. 1. Bonding mechanical stress simulation results on the bond pad with different aluminum metal film thicknesses. All are evaluated on the etching stop layers (SiC).

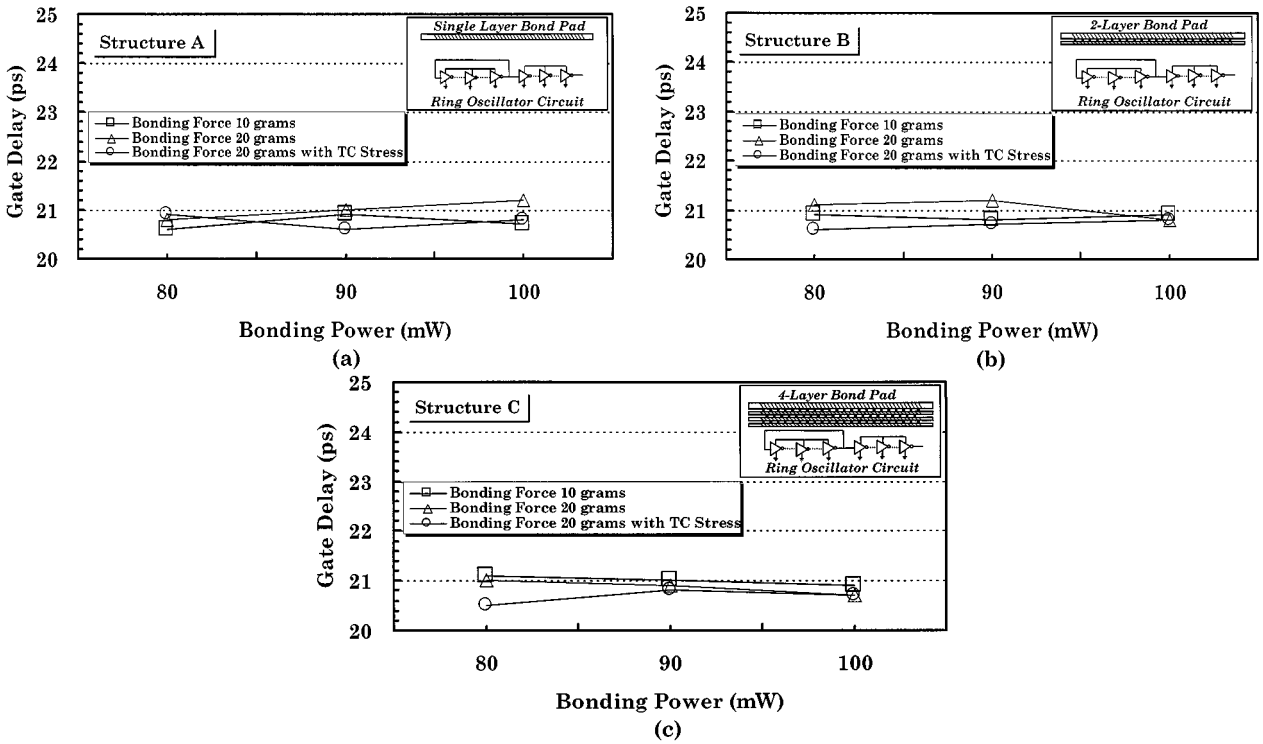

Fig. 2. Measured postbonding gate delay versus bonding power for (a) structure A, (b) structure B, and (c) structure C, each with different bonding force and thermal cycling conditions. The inset is schematic cross section of the corresponding structure.

pad pitch was 95 μm according to a loose design rule. The assembled test die was exposed to temperature cycling (TC) of -65 °C to 150 °C with a maximum of 500 cycles to examine inter-layer thin films damage from thermal mismatch stresses between aluminum metal film, topmost copper metal film and inter-layer films. Transmission line pulsing (TLP) in terms of a 100-ns current pulse was performed as well, followed by the leakage test between bond pads and underlying active circuits. Finally, a 1.2-V, 50% duty cycle voltage pulse with frequencies of up to 100 MHz was applied on the I/O pad to evaluate the

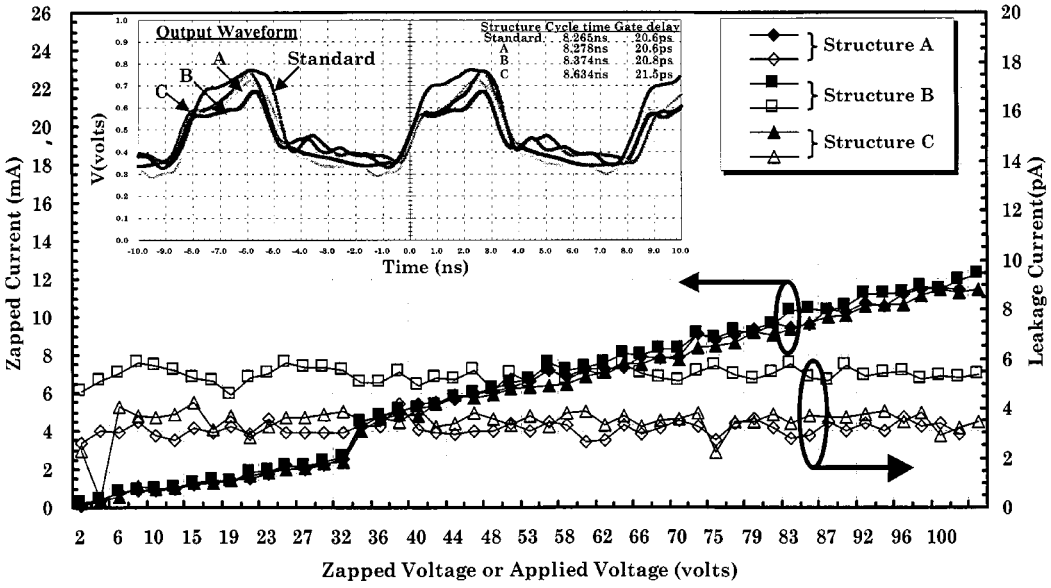

Fig. 3. Measured *I-V* characteristics from 100-ns TLP waveforms of the zapped I/O pads for structure A, B, and C. Together plotted is the monitored leakage versus applied voltage on the I/O pads for zapped structures. Inset shows output waveforms along with cycle times (i.e., oscillating periods) and gate delays of standard structure and the zapped structure A, B, and C.

sensitivity of underlying active circuits to capacitive coupling from the bond pad.

III. Experimental Results

The gate delay time per stage of ring oscillator measured prior to bonding was 20.9, 20.9, 20.6, and 21.0 ps for standard structure, structure A, structure B, and structure C, respectively. These prebonding ring oscillator gate delays are likely comparable to each other and thus the involved structures can all be considered as "control" samples, regardless of the number of Cu metal layers used. The measured gate delay versus bonding power is shown in Fig. 2 for structure A, B, and C each with different bonding force and thermal cycling. Also shown together is the inset of the cross section view of the corresponding CBP. From these demonstrations it can be seen that the bonding mechanical and thermal stresses do cause no significant degradations on electrical properties of CBP relative to "control" data. This confirms the feasibility of the 0.13 μm full eight-layer Cu metal/FSG low-k IMD CMOS process technology [5] in fabrication of CBPs, without accounting for any extra mechanically firm insulating films [2] or buffer metal layers [3], [4]. This indicates that the goal of recovering die area utility is reached. Strictly speaking, to make sure the underlying process technology is reliable and manufacturable in placing active circuits under the I/O pads, regardless of bonding force and power, more works are needed; for example, more rigorous reliability testing to qualify a product and/or process, more statistically meaningful data to address the manufacturability issue, etc.

During the TLP experiment for zapping (i.e., electrically sudden stressing) structure A, B, and C, the transient waveforms of the current through and voltage on the pad were monitored, from which a steady-state zapped current versus zapped voltage point was gotten. Adjusting pulse current height to around 12 mA (the corresponding pad voltage monitored was over 100 V), more such I–V data were created as displayed in Fig. 3. After each of TLP stresses, a leakage characterization was carried out. The measured leakage versus applied voltage is together plotted in the same figure. It can be seen that leakage currents between bond pad and CBP are relatively very low, merely 2 to 6 pA for structure A, B, and C. Inserted in Fig. 3 are the ring oscillator output waveforms of the standard structure as well as the zapped CBPs, along with the corresponding cycle time and gate delay labeled. Apparently, TLP stress does not produce noticeable performance degradation in the CBPs.

Finally, the oscillating period of the CBP while applying signal frequencies of 0, 1, 10, 50, and 100 MHz on I/O pad was measured: 8.2, 8.2, 8.4, 8.0, and 8.2 ns for structure A, respectively; 8.3, 8.3, 8.1, 8.0, and 8.3 ns for structure B, respectively; and 8.4, 8.4, 8.3, 8.3, and 8.6 ns for structure C, respectively. This data is not significantly different from each other. Thus, it is conclusively drawn that CBPs in our letter are not sensitive to signal coupling from the upper I/O pads.

IV. Conclusion

Placing active circuits under wire bonding I/O pads with a thick aluminum metal film as a bonding mechanical stress buffer layer is implemented in 0.13 μm eight-level Cu metal/FSG low-k IMD CMOS process and exhibits excellent performances in the mechanical, thermal, and electrical test.

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