

Enhanced Degradation in Polycrystalline Silicon Thin-Film Transistors Under Dynamic Hot-Carrier Stress

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Abstract—We address the mechanisms responsible for the enhanced degradation in the polysilicon thin-film transistors under dynamic hot-carrier stress. Unlike the monotonic decrease of maximum transconductance ($G_{m\max}$) in static stress, $G_{m\max}$ in dynamic stress is initially increased due to the channel shortening effect by holes injected into the gate oxide near the drain region and then decreased due to tail states generation at the gate oxide/channel interface and grain boundaries. The threshold voltage variations are dominated by two degradation mechanisms: 1) breaking of weak bonds and 2) breaking of strong bonds to obey the power-time dependence law with a slope of 0.4. The degradation of the sub-threshold slope is attributed to intra-grain bulk states generation.

Index Terms—Channel shortening effect, intra-grain bulk states, polysilicon thin-film transistors (poly-Si TFTs), tail states, transconductance ($G_{m\max}$).

I. INTRODUCTION

POLYSILICON thin-film transistors (poly-Si TFTs) have received increasing attention for application in active matrix liquid crystal displays (AMLCDs) and static random-access memories (SRAMs). Reliability is one of the major concerns, especially when a device is operated under high drain and high gate voltages. Hot carrier stress under high drain and high gate voltages decreases the transconductance, turn-on current, sub-threshold slope and increases the threshold voltage [1], [2]. Although the study of device aging with stress time under static hot-carrier stress has been systematically reported [3], to our knowledge, a study of the degradation in poly-Si TFT performance under dynamic hot-carrier stress has not been reported. Moreover, dynamic stress is closer to real operational conditions than static stress [4]. In this letter, we study the degradation mechanism by analyzing the evolution of device parameters including transconductance, threshold voltage, and sub-threshold slope.

II. EXPERIMENT

First, an undoped 100-nm-thick amorphous Si film was deposited on 500-nm-thick thermal oxide by decomposition of

Si_2H_6 at 460 °C in a low-pressure chemical vapor deposition system and then crystallized at 600 °C for 24 h. The measured average grain size is 1.1 μm . After defining the active channel region, a 50-nm-thick plasma-enhanced chemical vapor deposition SiO_2 film was deposited at 350 °C to serve as the gate dielectric. A 300-nm-thick amorphous Si gate layer was then deposited and patterned. Source and drain regions were formed by ion implantation of P^+ ($5 \times 10^{15} \text{ cm}^{-2}$, 50 KeV) and then activated at 600 °C for 12 h. Finally, passivation oxide and metal layers were deposited and patterned. Channel length and width are 10 μm and 5 μm , respectively. No hydrogenation step was performed on the poly-Si TFTs.

For dynamic stress, the drain is biased at $V_{\text{DS}} = 22 \text{ V}$ and the gate bias V_{GS} is square waveform switching from 0 V to 20 V with rise time 100 ns, fall time 100 ns and duty cycle 50%. For static stress, $V_{\text{DS}} = 22 \text{ V}$ and $V_{\text{GS}} = 20 \text{ V}$ were used. Threshold voltage is extracted by extrapolation of the $I_{\text{DS}} - V_{\text{GS}}$ curve from the point of $G_{m\max}$ in the linear regime ($V_{\text{DS}} = 0.1 \text{ V}$).

III. RESULTS AND DISCUSSION

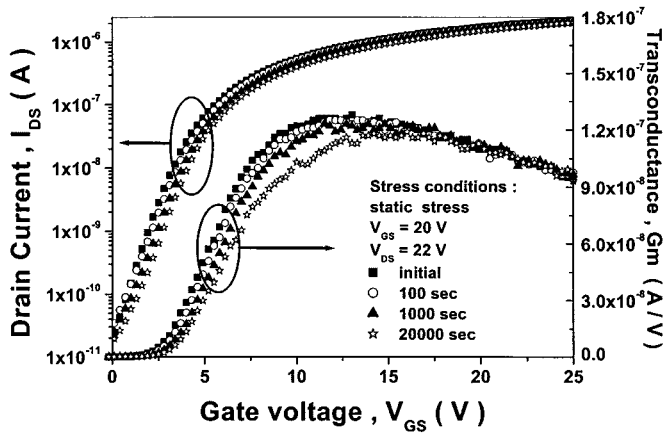
Fig. 1(a) and (b) show the different degradation behaviors of drain current and transconductance under static and dynamic stress, respectively. For static stress, $G_{m\max}$ decreases monotonically with the increase of the stress time at V_{GS} in the range of 0 V \sim 17 V and remains unchanged for $V_{\text{GS}} > 17 \text{ V}$. For dynamic stress, the curve of the transconductance shows a parallel shift in the positive direction, while $G_{m\max}$ is initially increased and then it starts to decrease after 1000 s stressing.

Fig. 2 shows the degradation of the $G_{m\max}$ defined as $-\Delta G_{m\max}/G_{m\max,o}$, where $\Delta G_{m\max} = G_{m\max,s} - G_{m\max,o}$, $G_{m\max,o}$ is the initial $G_{m\max}$ and $G_{m\max,s}$ is the $G_{m\max}$ for each stress time. For dynamic stress, $G_{m\max}$ initially increases, then saturates and finally starts to decrease after the turnaround point (as indicated by the arrow in Fig. 2). $G_{m\max}$ rising is attributed to channel shortening effect by holes injected into the gate oxide region near drain [5]. In the ON state, impact ionization will occur to generate hot electrons and hot holes near the drain. Once the device is switched from ON state to OFF state, the channel electrons will be repelled quickly into the drain side to gain additional energy and cause serious impact ionization near the drain. During the OFF state stress period, the electric field near the drain is very suitable ($V_{\text{GS}} - V_{\text{DS}} = -22 \text{ V}$) for holes injecting into the gate oxide. When the injected holes reach saturation at the turnaround point, tail states generation in the grain boundaries and gate

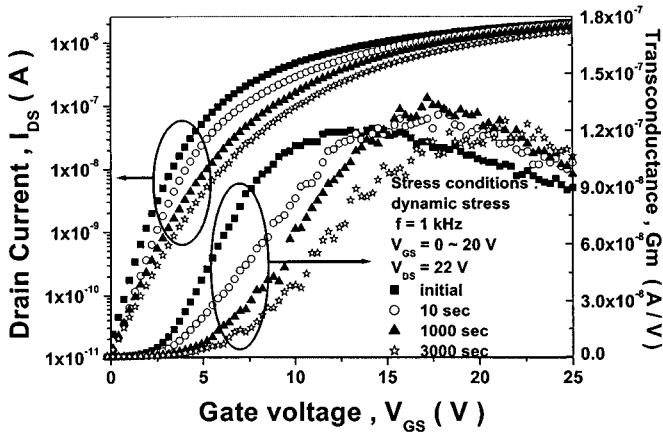
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(a)



(b)

Fig. 1. Degradation of drain current and trans-conductance by (a) static stress and (b) dynamic stress.

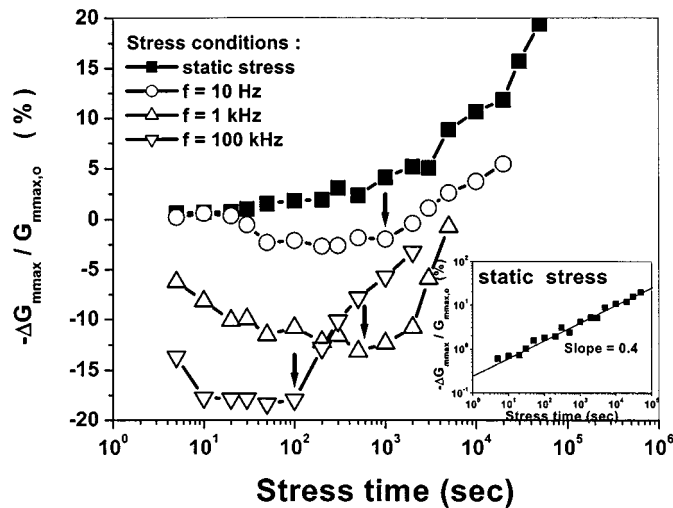


Fig. 2. Degradation of maximum trans-conductance as a function of the stress time under static and dynamic stress.

oxide/channel interface start to dominate $G_{m\max}$ degradation [3]. As the stress frequency increases, hole concentration will increase [6] and cause more serious channel shortening effect. However, for static stress, $G_{m\max}$ decreases monotonically and the insert plot of Fig. 2 shows that $G_{m\max}$ degradation

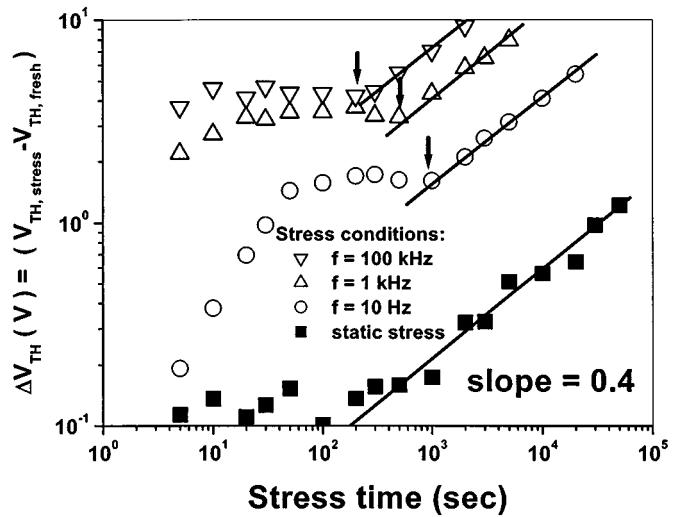


Fig. 3. Threshold voltage variations as a function of stress time under static and dynamic stress.

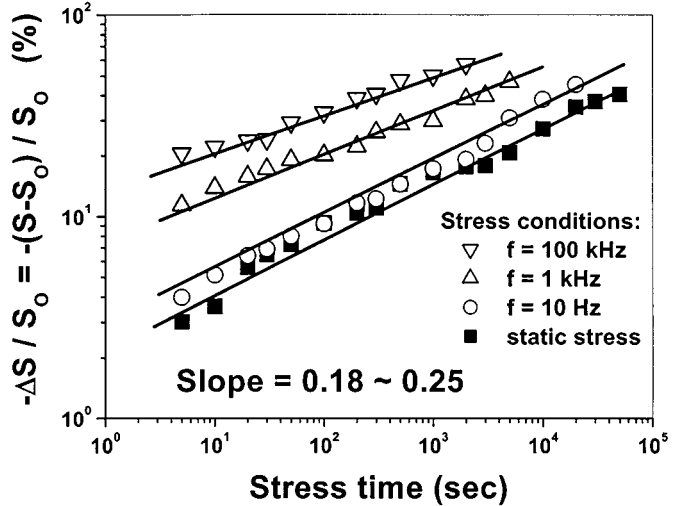


Fig. 4. Subthreshold slope variations as a function of stress time under static and dynamic stress.

exhibits a power-time dependence with a slope of 0.4 which is due to the tail states generation in the grain boundaries and at the gate oxide/channel interface [3], [7].

Fig. 3 shows the threshold voltage variations ΔV_{th} after stressing. Clearly, ΔV_{th} for static stress exhibits a power-time dependence with a slope of 0.4 and is much smaller than that of dynamic stress. For the dynamic stress, ΔV_{th} first saturates (first stage) and then it shows a power-time dependent law with a slope of 0.4 (second stage). The degradation in the first stage is due to deep states generation in the grain boundaries and at the gate oxide/channel interface by breaking the weak Si-H and Si-Si bonds. Once all of the available weak bonds are broken, ΔV_{th} saturates. The additional increase in ΔV_{th} after the turnaround point indicated by the arrows in Fig. 3 is due to the strong Si-Si bonds breaking [7], [8].

Fig. 4 shows the evolution of the sub-threshold slope variation $-\Delta S/S_0$, where $\Delta S = S - S_0$, S_0 is the initial sub-threshold slope and S is the sub-threshold slope for each stress time. A power-time dependence with a slope of 0.18~0.25 is

observed for both static and dynamic stress. Unlike in laser-annealed poly-Si TFTs where the sub-threshold slope remains unchanged after stressing [3], in solid-phase crystallized poly-Si TFTs, the sub-threshold slope varies with stress time indicating that intra-grain bulk states are generated in the poly-Si film [9]. Because the poly-Si film was formed by solid-phase crystallization method in this letter, intra-grain bulk state density is much higher and Si-Si bonds are weaker than those in laser-crystallized poly-Si film. Some more detailed study of the fall time and stress temperature effects on the device degradation is in progress.

IV. CONCLUSION

Poly-Si TFT degradation mechanisms under dynamic hot-carrier stress were studied. $G_{m\max}$ rising is due to channel shortening effect by hole injection into the gate oxide near the drain. As the stress frequency increases, the degradation becomes more serious. ΔV_{th} is dominated by two degradation mechanisms: breaking of weak bonds initially and breaking of strong bonds to obey a power-time dependence law in the second stage. The degradation of the sub-threshold slope is attributed to intra-grain bulk states generation in the poly-Si film.

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