Improving the RF Performance of 0.18 μm CMOS With Deep n-Well Implantation

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***Abstract*—The radio-frequency (RF) figures of merit of 0.18 μm complementary metal-oxide-semiconductor (CMOS) technology are investigated by evaluating the unity-current-gain cutoff frequency (F_t) and maximum oscillation frequency ($F_{\max}$). The device fabricated with an added deep n-well structure is shown to greatly enhance both the cutoff frequency and the maximum oscillation frequency, with negligible dc disturbance. Specifically, 18% increase in F_t and 25% increase in $F_{\max}$ are achieved. Since the deep n-well implant can be easily adopted in a standard CMOS process, the approach appears to be very promising for future CMOS RF applications.**

***Index Terms*—CMOS, deep n-well, maximum oscillation frequency, radio-frequency, unity-current-gain cutoff frequency.**

I. Introduction

In recent years complementary metal-oxide-semiconductor (CMOS) technologies have become viable for radio-frequency (RF) circuit implementations due to aggressive scaling, progress on high-speed performance and reduction in cost. Considerable research is still in progress today to explore CMOS for improving various RF figures of merit (FOM), such as, SiGe notched gate [1], thin gate-bird's-beak [2], T-shaped metal gate [3], cobalt-salicided raised gate/source/drain [4], epitaxial channel [5], [6] and silicon-on-insulator (SOI) wafers. Most of these investigations attempted to optimize the RF FOM with minimum disturbance to the static behavior, as well as to be compatible with standard logic process. Since silicon wafers have relatively low substrate resistivity, compared with GaAs wafers, the substrate coupling is significant in Si-based technologies. Previously, the use of a deep n-well implant has been shown to be effective in suppressing the cross-talk in bipolar-CMOS (BiCMOS) technology [7]. However, RF characteristics of a MOSFET with a deep n-well structure have, to the best of our knowledge, never been reported. In this letter, we report, for the first time, the effects of incorporating a deep n-well structure, on the two major RF FOMs: cutoff frequency (F_t) and maximum oscillation frequency ($F_{\max}$).

Manuscript received June 1, 2001; revised June 3, 2001. This work was supported in part by the Mixed-signal/RF CMOS Project, Research Development, Taiwan Semiconductor Manufacturing Co. and in part by National Science Council, Taiwan, R.O.C., under Contract NSC89-2218-E009-071. The review of this letter was arranged by Editor K. De Meyer.

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Publisher Item Identifier S 0741-3106(01)08856-5.

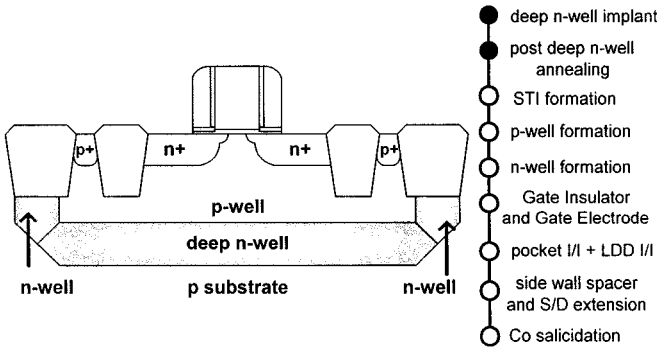

Fig. 1. Cross section and key process flow of n-channel MOSFET with deep n-well structure. The deep n-well was formed underneath the p-well and together with the regular n-well implant, completely surrounds the p-well region.

II. Device Structure, Fabrication, and Measurements

The schematic cross section of an n-type MOSFET with the proposed deep n-well structure and its key process flow are shown in Fig. 1. The process adopts a 0.18 μm logic CMOS technology, with the addition of the deep n-well process and mask. To minimize the disturbance to the dc behavior of MOS transistors, high-energy ion implantation (I/I) steps, followed by postimplant annealing, was used to form the deep n-well. Specifically, I/I steps consist of a 2 MeV I/I with an arsenic dose of 2×10^{13} cm^2 to form a deep enough n-well so as not to disturb the doping profile of inner p-well and a 1 MeV I/I with lower arsenic dose was used together with the regular n-well implant and a flat plateau of deep n-well. The postimplant annealing was performed at 1000 °C. As a result, the resultant n-well (i.e., regular n-well and deep n-well combined) completely surrounds the p-well region for junction isolation. The resultant p-well and deep n-well depth are about 0.8 μm and 2.2 μm, respectively, as obtained by two-dimensional (2-D) process/device simulation as shown in Fig. 2, which has been further confirmed by the SIMS profile. For comparison, standard MOSFETs without deep n-well structure were also fabricated on the same wafers.

The gate length of the transistors is 0.18 μm. To simultaneously optimize the gate resistance and gate to bulk capacitance, finger-gated device structure with a total width of 160 μm and a finger number of 16 is used in this study. Both the standard device and the new device with deep n-well share the same layout, the geometry-dependent parasitic capacitance and resistance are expected to be identical. The pads of these testing devices are configured in ground-signal-ground with ground-shielding signal pads and the deep n-well was floating. All the

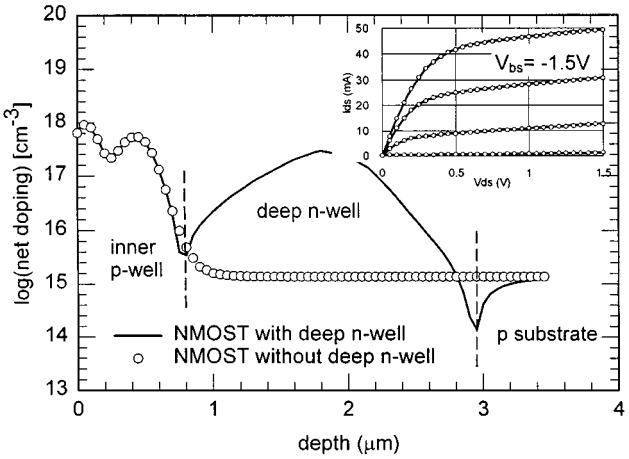

Fig. 2. Simulated 2-D net doping profiles of a conventional transistor and a transistor with deep n-well structure. Inset shows essentially identical dc behaviors of both devices. The line is represents the MOSFET with deep n-well and circle symbol is represents the counterpart.

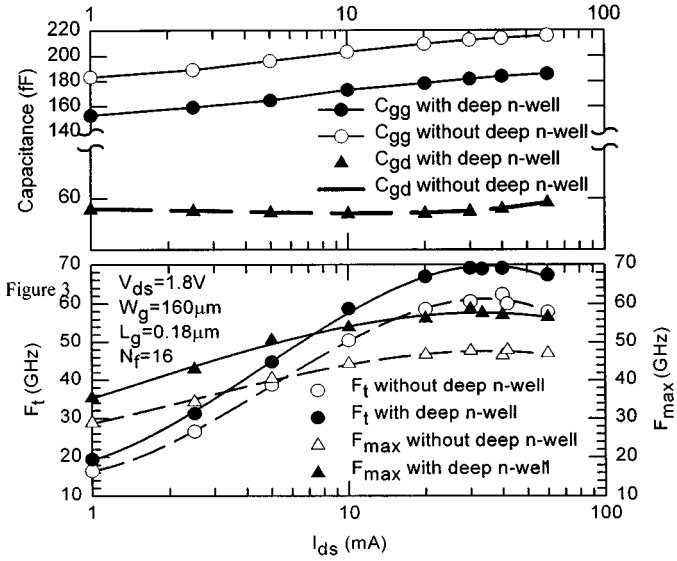

Fig. 3. Top figure shows gate capacitance and gate-to-drain capacitance of conventional MOSFET and MOSFET with deep n-well. $C_{\rm gg}$ is reduced by MOSFET with deep n-well structure, while minimal $C_{\rm gd}$ difference is observed. The lower parts depicts F_t and $F_{\rm max}$ of devices with conventional and deep n-well structure.

extracted F_t and $F_{\rm max}$ from S-parameter measurements were based on "two-step de-embedding" procedure [8].

III. Experimental Results and Discussion

The deep n-well CMOS technology gives minimal discrepancy on dc characteristics, as confirmed from the identical $I_{\rm d}-V_{\rm ds}$ (with $V_{\rm bs}=-1.5$ V) characteristics shown in the inset of Fig. 2. The result implies the fact that depletion charges that correspond to the intrinsic part of MOSFET (i.e., under the channel) are essentially identical in both devices. F_t and $F_{\rm max}$ are the two most important high-frequency FOMs. The device with deep n-well shows not only better F_t but also $F_{\rm max}$. As shown in the lower part of Fig. 3, about 10% to 18% improvements in F_t and 20% to 25% improvements in $F_{\rm max}$ can be observed. The peak F_t of the device with deep n-well is about 70 GHz and the peak $F_{\rm max}$ is about 58 GHz with $V_{\rm gs}$ biased at the maximum transconductance. F_t can be estimated from the terminal admittance matrix [9], [10] and can be approximated as

$$F_t \cong \frac{g_m}{2\pi\sqrt{C_{\rm gg}^2 - C_{\rm gd}^2}} \tag{1}$$

where $C_{\rm gd}$ is the gate-to-drain capacitance and $C_{\rm gg}$ is the total gate capacitance which includes all the intrinsic and extrinsic capacitance as seen from the gate (i.e., $C_{\rm gg}=C_{\rm gs}+C_{\rm gd}+C_{\rm gb}$). The upper part of Fig. 3 shows $C_{\rm gg}$ and $C_{\rm gd}$ versus the drain current. All of the capacitance in Fig. 3 was extracted from the imaginary part of y-parameter (i.e., $C_{\rm gg}={\rm Im}(y_{11})/\omega$ and $C_{\rm gd}=-{\rm Im}(y_{12})/\omega$) as proposed in [9], [11]. It can be seen that $C_{\rm gg}$ of the device with deep n-well is reduced by about 30 fF, compared to the conventional counterpart, while $C_{\rm gd}$ of both structures show minimal discrepancy. Since the dc behavior of the control device and the new device with deep n-well are almost identical as aforementioned and their transconductance is the same, the F_t improvement of MOSFET with deep n-well structure is mainly attributed to the reduction of $C_{\rm gg}$.

Since the intrinsic $C_{\rm gd}$ is nearly zero in saturation region [10], the extracted $C_{\rm gd}$ in Fig. 3 is mainly attributed to extrinsic $C_{\rm gd}$. This implies the fact that extrinsic $C_{\rm gs}$ and $C_{\rm gd}$ of both devices are identical. Besides, $C_{\rm gb}$ is extremely small for short channel device and hence, the reduction of $C_{\rm gg}$ is mainly attributed to the reduction of intrinsic $C_{\rm gs}$ as shown in Fig. 4. The intrinsic $C_{\rm gs}$ in Fig. 4 were obtained by performing the ac analysis of the 2-D device simulation [12], with $C_{\rm gs}$ derived from the imaginary part of terminal admittance $y_{\rm gs}$. Calculation of $y_{\rm gs}$ is by forcing small-signal voltage (i.e., 50 mV in this study) to the source electrode ($\nu_{\rm s}$) and sensing the current at the gate electrode ($i_{\rm g}$), calculating $y_{\rm gs}=\partial i_{\rm g}/\partial \nu_{\rm s}$. To investigate the $C_{\rm gs}$ reduction, the small-signal equivalent circuit of substrate network for a MOSFET with deep n-well is sketched in Fig. 4. Node bi refers to the intrinsic body of the inner p-well and $C1$, $C2$, and $C3$ refer to the series junction capacitance of inner p-well to deep n-well and from deep n-well to p substrate on source side, drain side and bottom side respectively. There exists a capacitive loop that the signal propagates from the intrinsic source end to the gate electrode. The other capacitive loop is that the signal propagates from intrinsic source through node bi, through deep n-well junction capacitance (i.e., $C1$, $C2$, and $C3$) and then through substrate resistance ($R_{\rm psub}$) to the ground. This added capacitive path that passes through $C1$, $C2$, and $C3$ lowers the imaginary part of $y_{\rm gs}$ due to the lowering of $i_{\rm g}$ and hence the intrinsic $C_{\rm gs}$. For further confirmation, devices without pads being de-embedded were also compared (data not shown), it was found that the F_t improvement and ${\rm Im}(y_{11})$ reduction still hold, confirming that the F_t improvement and ${\rm Im}(y_{11})$ reduction are not artifacts of de-embedded technique.

The reduction of $C_{\rm gg}$ also directly increases $F_{\rm max}$, as $F_{\rm max}$ is proportional to the cut-off frequency [10]

$$F_{\rm max}=\frac{F_t}{2\sqrt{g_{\rm ds}\left(R_{\rm g}+R_{\rm s}\right)+2\pi F_t R_{\rm g} C_{\rm gd}}}. \tag{2}$$

Furthermore, both $|S_{21}|$ and $|S_{12}|$ of MOSFET with deep n-well increase by the similar ratio, compared to their counter-

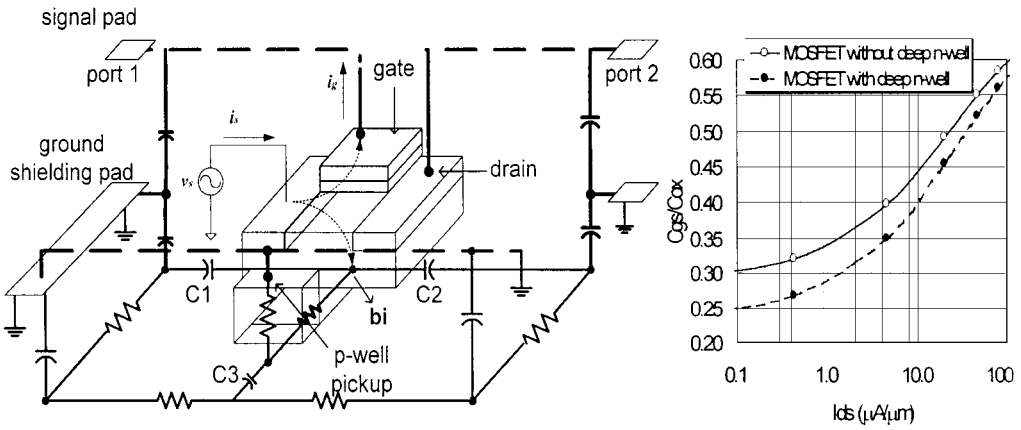

Fig. 4. Lumped substrate network of MOSFET with deep n-well, used to illustrate the intrinsic $C_{\rm gs}$ reduction of MOSFET with deep n-well structure. The arrows with dot line represent the capacitive loops of RF signals that generated from the source toward the gate and substrate. The intrinsic $C_{\rm gs}$ is equal to the imaginary part of $i_{\rm g}/\nu_{\rm s}$. $R_{\rm psub}$, $R_{\rm pw}$, and $C_{\rm p}$ represent the p substrate resistance, inner p-well resistance and ground pads to p substrate capacitance, respectively.

parts. This is because the deep n-well reduces the effective junction capacitance of source/drain by nearly 25% from 120 fF to 90.4 fF on the MOSFET with $W/L = 160\ \mu{\rm m}/0.18\ \mu{\rm m}$ at 1.5 V reversed bias and, hence, provides high impedance at port-2. This high impedance can prevent the high frequency signal loss from the drain to the substrate and thus, increases the power delivered to the drain electrode, increasing S_{21} [13]. This also enhances power from drain to gate, increasing S_{12}. This results in the same maximum stable power gain for both devices in the frequency range where k-factor < 1. However, under the frequency range of k-factor > 1, MOSFET with deep n-well exhibits better maximum available power gain than its counterpart due to the smaller k-factor (because of reduced $C_{\rm gs}$ [14]).

IV. Conclusion

The incorporation of a deep n-well implantation to a standard CMOS technology is shown the fact that F_t and $F_{\rm max}$ can be increased by about 18% and 25% respectively, giving a 70 GHz peak F_t and 58 GHz peak $F_{\rm max}$ of MOSFETs addition with the deep n-well. The deep n-well appears to be useful for enhancing the performance of CMOS-based RF circuits without disturbing the dc characteristics.

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