Impact of Silicide Formation on the Resistance of Common Source/Drain Region

Bing-Yue Tsui, *Member, IEEE*, Ming-Da Wu, and Tian-Choy Gan

***Abstract*—Silicide had been used to reduce the sheet resistance of diffusion region for almost 20 years. However, as the silicided region becomes small, the contact resistance of silicide/silicon interface becomes higher than the resistance of the Si diffusion region such that current may not flow into the silicide layer. The effect of silicide thickness and contact resistivity on the total resistance of the silicided diffusion region was studied by two-dimensional simulation. It is observed that below a threshold length, the resistance of silicided diffusion region is higher than the unsilicided diffusion region if the silicon consumption during silicide formation is taken into consideration. Thinner silicide and lower contact resistivity reduce total resistance and threshold length but the threshold length is still much longer than the typical design rule of poly-Si to poly-Si distance. It is thus recommended to inhibit silicide formation at the common source/drain region at the metal-gate generation.**

***Index Terms*—Contact resistance, silicide, simulation.**

I. Introduction

SALICIDE technology had been used for all high–performance integrated circuit process [1]. Using salicide technology, the high–resistance diffusion region and poly-Si gate are shunted by a low resistivity metal silicide layer. Because silicide is formed by direct reaction of metal with silicon, the contact resistance of silicide-silicon interface is also reduced by the clean interface and large contact area. The advantages of silicide had been analytically analyzed by D.B. Scott, *et al.* [2]. It was shown that the resistance of silicided diffusion region with metal contact could be reduced effectively. However, this is not the case at silicided diffusion region without metal contact, e.g., two MOSFETs connected in serial with a common diffusion region (CDR). At this region, current flows in Si originally. To take the advantage of silicide, current must flow into silicide at first and flow into Si again. As the length of CDR becomes shorter and shorter, current does not flow into silicide because of the high–contact resistance.

In the previous work, the consumption of heavily doped Si layer by silicide was not considered. With the progress of processing technology, the scale-down of silicide thickness lags behind the scale-down of junction depth [3]. Therefore, the sheet resistance of diffusion region under silicide may be increased by silicide formation apparently. The role of silicide layer at CDR becomes interesting. In this work, two-dimensional (2–D) simulation was performed to study the impact of silicide thickness and contact resistivity on the resistance of CDR without metal contact. A brief discussion on the feasibility of unsilicided CDR is provided at last.

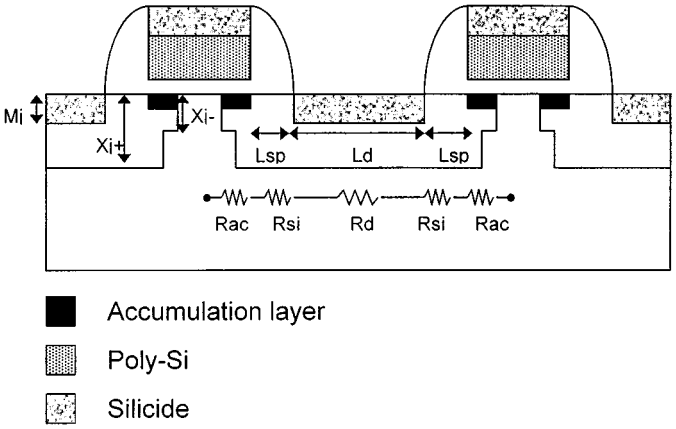

Fig. 1. Schematic cross-sectional view of the structure used for two-dimensional simulation. Resistance components are also indicated. $R_{\rm ac}$ is accumulation layer resistance at the gate to source/drain overlap region. $R_{\rm si}$ consists of spreading resistance and diffusion resistance of diffusion region under spacer. R_d is the resistance of common diffusion region.

II. Simulation Procedure

Fig. 1 shows the cross-sectional view of the structure used for simulation. Two MOSFETs with typical drain structure are connected in serial through a CDR without metal contact. A box shape is used for the junction. It had been reported that the simplified box shape does not affect the validity of simulation results of the diffusion region [4]. The carrier concentration is estimated by the Gaussian-distribution with peak concentration at surface. The lateral diffusion is assumed to be 70% of the vertical junction depth. The carrier concentration of the accumulation layer underneath the gate is assumed to be identical to the surface concentration of the heavily doped region (1×10^{20} cm^{-3}) and the thickness of this layer is 10 nm [5]. The bulk concentration and the surface concentration of source/drain extension region is 2×10^{18} cm^{-3} and 1×10^{19} cm^{-3}, respectively. The silicide thickness is assumed to be equal to the contact interface depth (M_j). The right boundary of the accumulation layer at right side is kept at V_0 and the left boundary of the accumulation layer at left side is kept at 0 V. The structure is partitioned into resistor network. The node voltage and branch current were solved numerically by applying Kirchhoff's current law to the resistor network. The total resistance (R_t) is defined

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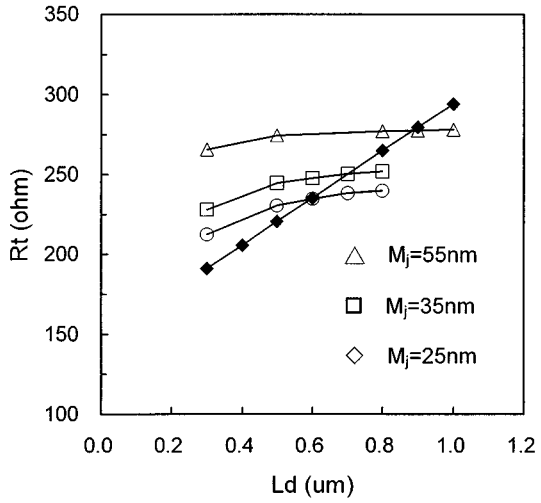

Fig. 2. Total resistance (R_t) versus length of common diffusion region (L_d) with M_j of 25 nm, 35 nm, and 55 nm. The ρ_c was kept at 10 ohm$-\mu$m^2.

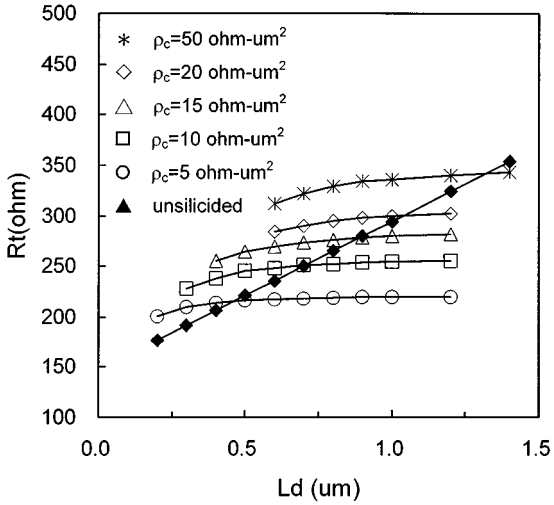

Fig. 3. Total resistance (R_t) versus length of common diffusion region (L_d) with ρ_c of 5, 10, 15, 20, and 50 ohm$-\mu$m^2. The M_j was kept at 35 nm.

as the V_0 divided by the total current. It consists of all resistance components between the two accumulation layers as shown in Fig. 1.

The effect of contact resistivity (ρ_c) and silicide thickness (M_j) on the total resistance of silicided and unsilicided CDR were simulated. The spacer length ($L_{\rm sp}$) is assumed to be 0.1 μm. The junction depth of heavily doped region and source/drain extension region is 0.11 μm and 0.07 μm, respectively. The channel width is fixed at 1 μm throughout the work.

III. Results and Discussion

Fig. 2 shows the simulated R_t as a function of the distance between spacers (L_d) with M_j of 25 nm, 35 nm, and 55 nm. The ρ_c was fixed to be 10 ohm$-\mu$m^2. The silicide thickness of 25–35 nm is generally used in the current 0.18 μm or 0.13 μm technology, while the thickness of 55 nm is the upper limit suggested by ITRS roadmap [3]. In the case of unsilicided CDR, R_t decreases linearly with L_d as expected. In the case of silicided CDR, nonlinear R_t-L_d phenomenon is observed and it is surprising that thicker M_j results in higher R_t at all L_d. Cross point of the R_t-L_d characteristics of unsilicided CDR and silicided CDR is observed. The crosspoint is defined as the threshold length ($L_{\rm th}$) of the CDR. As L_d is longer than $L_{\rm th}$, R_t of the silicided CDR is lower than that of the unsilicided CDR and vice versa. It should be noted that the $L_{\rm th}$ (0.89 μm as $M_j = 55$ nm and 0.6 μm as $M_j = 25$ nm) is much longer than the general design rule of poly-Si to poly-Si distance.

The simulated results can be understood by considering the two current paths: silicide layer and diffusion layer. If $L_d/2$ is much longer than the transfer length (L_t) of the silicide-silicon contact interface [6], the contact resistance is lower than the diffusion resistance and current prefers to flow through the silicide layer. In this case, R_t is composed of the sheet resistance of silicide layer and contact resistance across silicide-silicon interface. On the other hand, once $L_d/2$ becomes close to L_t, the contact resistance is higher than the diffusion resistance and current tends to flow in the diffused layer. Unfortunately, the sheet resistance of diffused layer under silicide is higher than that at unsilicided region because the high–concentration layer was consumed by the silicide. The R_t is then the result of two high–resistance paths in parallel and the sheet resistance of silicide layer plays minor role. Therefore, thicker silicide thickness results in higher R_t and longer $L_{\rm th}$.

Fig. 3 shows the simulated R_t as a function of L_d with ρ_c of 5, 10, 15, 20, and 50 $\Omega\,\mu$m^2. The M_j was fixed at 35 nm. The R_t-L_d relation of unsilicided CDR is also shown. The R_t increases with the increase of ρ_c as expected. Again, the $L_{\rm th}$ is much longer than the typical design rule of poly-Si to poly-Si distance.

To prove the existence of $L_{\rm th}$, test structures with two MOSFETs connected in serial were fabricated with standard 0.18 μm cobalt-salicide CMOS technology. Only NMOS test structure was designed. The gate length is 0.18 μm and the spacer length is 0.1 μm. A set of test structures employed a silicide-blocking mask to inhibit silicide formation at the CDR. The other set of test structures has typical salicide structure. These structures were measured at linear region ($V_{\rm bs} = 0$, $V_{\rm ds} = 0.1$ V and $V_{\rm gs} = 0 \sim 1.8$ V). The difference of transconductance (g_m) between silicided and unsilicided test structures is defined as

$$\Delta g_m = \frac{g_m(\text{silicided}) - g_m(\text{unsilicided})}{g_m(\text{unsilicided})} \times 100\%.$$

Fig. 4 shows the measured Δg_m as a function of L_d. A $L_{\rm th}$ of 0.24 μm was observed. Below 0.24 μm, the silicided test structures show lower g_m than the unsilicided test structure. This result confirms the existence of $L_{\rm th}$. The low Δg_m of 3% and the short $L_{\rm th}$ of 0.24 μm arises from the unusual structure of deep junction depth (0.25 μm) and thin silicide thickness (28 nm).

IV. Conclusion

The impact of silicidation on the resistance of CDR was studied using 2-D simulation. A threshold length $L_{\rm th}$ was observed. As L_d is shorter than $L_{\rm th}$, silicided CDR shows higher resistance than the unsilicided CDR. Thinner silicide layer and lower contact resistivity can reduce the $L_{\rm th}$. However, the $L_{\rm th}$ is still much longer than typical design rule of poly-Si to

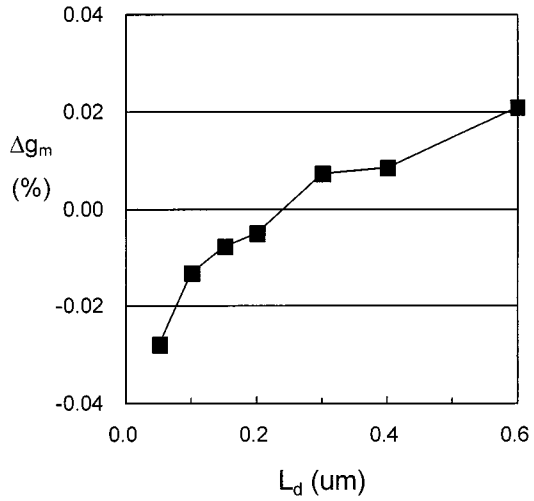

Fig. 4. Measured transconductance difference (Δg_m) versus length of common diffusion length (L_d) between test structures with silicided and unsilicided common diffusion region.

poly-Si distance. The series resistance between the two devices must not be estimated using the sheet resistance of silicide layer. To block the CDR is unacceptable at current poly-Si gate technology because part of the poly-Si gate will also be blocked. Polycide gate allows silcide blocking at CDR but polycide process is seldom used in high–performance deep–submicron products. Beyond 0.07 μm technology node, metal gate may replace poly-Si gate. Then, silicide is only needed at diffusion region but not at gate region. Inhibiting silicide formation at CDR becomes easy. It is, thus, recommended to neglect silicide at CDR in the future metal-gate technology node.

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