A Novel High-Performance Poly-Silicon Thin Film Transistor With a Self-Aligned Thicker Sub-Gate Oxide Near the Drain/Source Regions

Kow Ming Chang, Yuan Hung Chung, Gin Ming Lin, Jian Hong Lin, and Chi Gun Deng

***Abstract*—In this letter, a novel high-performance poly-silicon thin-film transistor (poly-Si TFT) with a self-aligned thicker sub-gate oxide near the drain/source regions is proposed. Poly-Si TFTs with this new structure have been successfully fabricated and the results demonstrate a higher on-off current ratio of 5.9×10^6 and also shows the off-state leakage current 100 times lower than those of the conventional ones at $V_{\rm GS} = -15$ V and $V_{\rm DS} = 10$ V. Only four photo-masking steps are required and fully compatible with the conventional TFT fabrication processes. This novel structure is a good candidate for the further high-performance large-area device applications.**

***Index Terms*—On–off current ratio, photo-masking steps, poly-silicon thin-film transistor, self-aligned thicker sub-gate oxide.**

I. Introduction

POLY-SILICON thin-film transistors (poly-Si TFTs) have received increasing attention for high-performance large-area active matrix liquid crystal display (AMLCD) applications as compared to conventional amorphous-Si TFTs [1], [2]. However, the undesired off-state leakage current for a poly-Si TFT is much higher than that of an amorphous-Si TFT. It has been reported that the conduction mechanism for the off-state leakage current is the field emission via grain boundary traps due to high electric field in the drain depletion region [3]. Thus, to reduce the drain electric field, suppressing the off-state leakage current is required. Several methods have been proposed to achieve this purpose, such as offset gated structure [4], lightly doped drain structure [5] and field induced drain structure [6], [7]. The implant damage in the lightly doped offset drain structure can cause an undesired degradation in the drain junction, especially for low-temperature processed poly-Si TFTs [8]. In the field induced drain structure, an additional photo masking step is required and unavoidable photo masking misalignment error will occur [6], [7].

In this letter, we propose a novel TFT structure with a self-aligned thicker sub-gate oxide near the drain/source regions which has a much lower off-state leakage current and higher on-off current ratio than those of a conventional structure. Only four photo-masking steps are required and it is fully compatible with the conventional TFT processes. Poly-Si TFTs with the new structure are successfully demonstrated.

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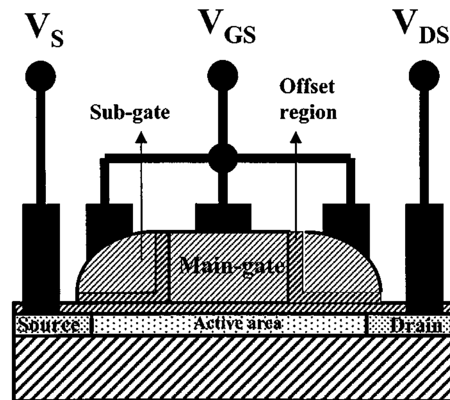

Fig. 1. Schematic diagram of the proposed new TFT structure.

II. Experiments

Fig. 1 shows the schematic diagram of the proposed TFT structure. The top view of the proposed TFT structure is shown in Fig. 2(a) and the cross-sectional view along the line AA' is shown in Fig. 2(b). A conventional top gate TFT structure was formed with 200-nm poly-Si active layer, 50-nm plasma enhanced chemical vapor deposition (PECVD) gate oxide layer deposited at 350 °C, 400-nm poly-Si main gate electrode and 10 μm channel length. The 200-nm poly-Si active layer is formed by silicon amorphous layer deposition in low pressure chemical vapor deposition (LPCVD) system using Si_2H_6 gas at 460 °C and then crystallized at 600 °C for 24 h. The average grain size measured by transmission electron microscopy and the trap state density determined using Levinson's method [9] are 1.1 μm and 6×10^{12} cm^{-2}, respectively. After main gate electrode patterning and blanket deposition of 100-nm PECVD oxide and 350-nm poly-Si layers, a reactive ion etching process was used to anisotropically etch the poly-Si and PECVD oxide layers. Therefore, self-aligned offset region (PECVD oxide) and self-aligned poly-Si spacers were formed [Fig. 2(b)]. The self-aligned poly-Si spacers are also noted as the sub-gates of the TFT. The gate oxide for the sub-gate region with length 300 nm is thicker than the main-gate region and is almost 150 nm. For n-channel transistors, P^+ implant with a dosage of 5×10^{15} at 40 KeV was used and then activated in N_2 at 600 °C for 24 h. To apply the voltage source on the sub-gates, new contact windows were opened as shown in Fig. 2(c), which

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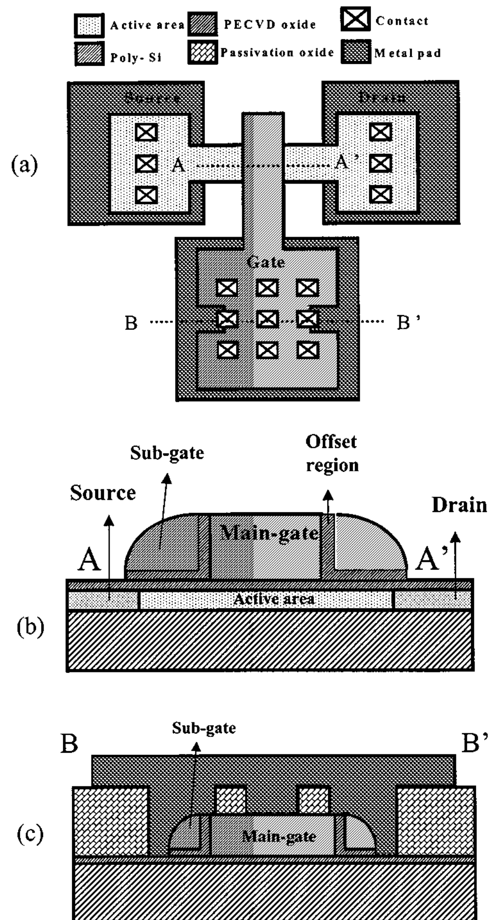

Fig. 2. (a) Top view of the proposed TFT structure. (b) Cross-sectional view along the line AA'. (c) Cross-sectional view along the line BB'.

is the cross-section BB'. Poly-Si TFTs with conventional structure, e.g., without the sub-gates, were also fabricated to serve as a control. The channel length of the proposed TFT ($L = 10.8\ \mu$m) is the summation of the main gate length (10 μm), the thickness of two self-align offset PECVD oxides (0.2 μm) and the length of the two sub-gate lengths (0.6 μm).

It should be mentioned here that the current-voltage *(I-V)* characteristics of the proposed TFT have not been optimized because the electric characteristics are very sensitive to the length of the sub-gate. The study of the optimization of the sub-gate length for the proposed TFT structure is still under investigation.

III. Results and Discussion

As shown in Fig. 3, the off-state leakage current of the new TFT is much lower than that of the conventional TFT control. The off state leakage current at $V_{\rm GS} = -15$ V is 100 times smaller than that of the conventional TFT control ($L = 10\ \mu$m). The on-off current ratios of the conventional and proposed TFTs are 1.1×10^6 and 5.9×10^6, respectively. The on-off current ratio is defined as that ratio of the maximum on state current to the minimum off– state current. The main reason for much lower off-state leakage current of the new TFT is that the drain electric field is greatly reduced for the thicker gate oxide in the sub-gate regions and the self-aligned offset PECVD oxide. The

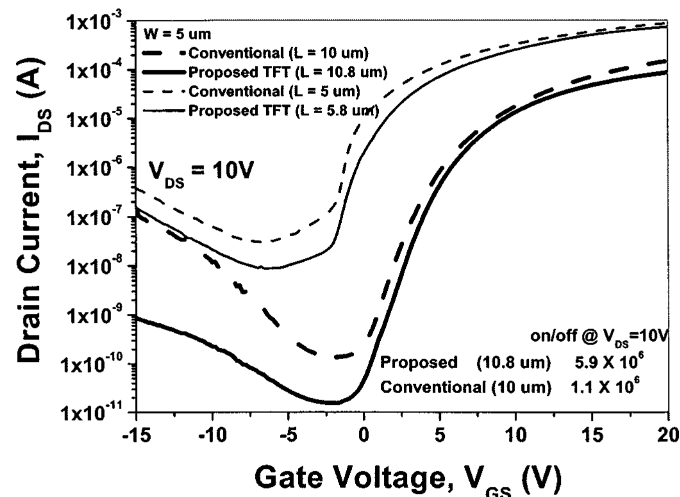

Fig. 3. $I_{\rm DS}-V_{\rm GS}$ transfer characteristics of the conventional and new TFTs.

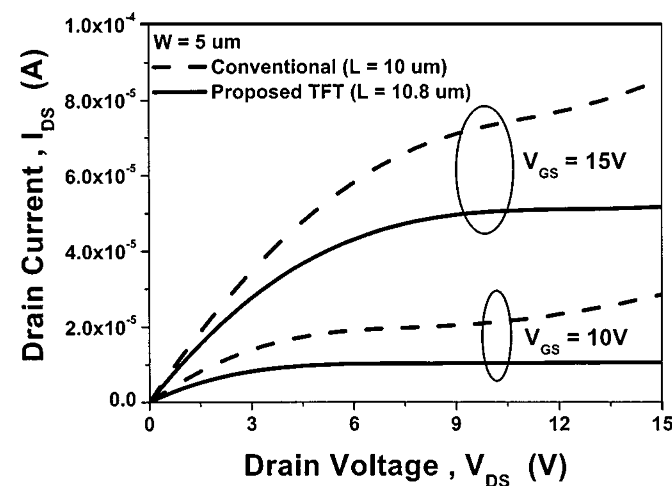

Fig. 4. $I_{\rm DS}-V_{\rm DS}$ characteristics of the conventional and proposed TFTs.

$I_{\rm DS}-V_{\rm GS}$ characteristics of a short channel device ($L = 5\ \mu$m) are also shown in Fig. 3. It can be observed that the leakage current improvement in the short channel device is not as good as in the long channel device. This is because the electric field in a short channel device is so high that it is not easy to reduce the electric field and make the decreasing of leakage current effectively. In Fig. 4, less kink effect can be observed in the new TFT to further confirm that the drain electric field can be effectively reduced in the proposed TFT. Although the off-state leakage current can be reduced, the turn-on current is slightly degraded due to the higher source/drain series resistance caused by the thicker sub-gate oxide and the self-aligned offset PECVD oxide. The optimization of the sub-gate length is still under investigation to have an acceptable series resistance for on-state and off-state characteristics.

IV. Conclusion

In this letter, a novel high-performance TFT with a self-aligned thicker sub-gate oxide near the drain/source regions has been proposed and successfully demonstrated. Much lower off-state leakage currents and a higher on-off

current ratio can be obtained for the proposed TFT. The TFT fabrication processes are fully compatible with the conventional four-mask ones. This new TFT structure may be an attractive device structure for future high-performance large-area device applications.

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