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Large-scale "atomistic" approach to discrete-dopant-induced characteristic fluctuations in silicon nanowire transistors

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Nanowire fin-typed field effect transistors (FinFETs) are ultimate structures and potential candidates for next generation nanoelectronic devices. Due to the limitation of manufacturability, nanowire transistors with a perfect gate structure (i.e., a surrounding gate with 100% gate-coverage ratio) theoretically are not always guaranteed. Impact of the discrete dopants on device performance is crucial in determining the behaviour of nanoscale semiconductor devices. The immunity of nanowire transistor against random discrete-dopant-induced fluctuation may suffer from the variation of gate-coverage-ratio. Therefore, in this paper, we for the fist time study the impact of non-ideal gate coverage on immunity against random-dopant-induced fluctuations for nanowire FinFETs. A 3D statistically sound "atomistic" approach for analyzing random-dopant effect in nanodevice is presented. Discrete dopants are statistically positioned into the channel region to examine associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". Our results confirm that the influence of non-ideal gate coverage disturbs the channel controllability of nanowire FinFETs and thus decreases the immunity against discrete-dopant-induced fluctuation. This study provides an insight into the problem of fluctuation in nanowire transistors and shows the importance of gate-coverage ratio on device's immunity against discrete-dopant-induced fluctuation.

1 Introduction Ion implantation, diffusion and thermal annealing induce significant random fluctuations in the physical and electrical characteristics of nanometer scale metal–oxide–semiconductor field effect transistors (MOSFETs). Effects of different randomness on device characteristics have recently been studied both experimentally and theoretically [1–20]. Fluctuations of characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. Moreover, fluctuations are particularly pronounced as the spatial scale of doping and oxide thickness variations become comparable with the dimensions of devices [3, 10, 11]. The International Technology Roadmap for Semiconductors has forecasted a transition from conventional bulk devices to silicon-on-insulator (SOI) devices, and then to multiple-gate SOIs as high-performance devices [21]. Consequently, nanoscale devices with vertical channel structures, such as double-, triple- and surrounding-gate fin-typed FETs (FinFETs) are of great interest [22–24]. Among them, nanowire FinFETs are ultimate structures and potential candidates for next generation high-speed and high-power electronic devices. However, due to the manufacturability, nanowire transistors with a perfect gate structure (i.e., a surrounding gate with 100% gate-coverage ratio) theoretically are not always guaranteed. Therefore, impact of non-ideal nanowire gate-coverage ratio on immunity against discrete-dopant-induced fluctuations is crucial in determining the behaviour of nanoscale semiconductor devices and results in a compromise between the device performance and manufacturability.

Diverse computational approaches, such as small-signal analysis [1–3], drift-diffusion (DD) [4–6] and

Monte Carlo simulation [7–9] have recently been reported to study fluctuation-related issues in semiconductor devices. Unfortunately, the effect of the number and position of discrete dopants on the characteristics of the aforementioned devices has not been clearly investigated yet. This study thus tries to employ a statistically sound "atomistic" approach to analyze the random impurity effect in nanoscale device, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". The statistically generated large-scale doping profiles are similar to the physical process of ion implantation and the number of impurities inside channel follows normal distribution. Based on the statistically generated large-scale doping profiles, each device simulation is performed by solving a set of 3D DD equations with quantum corrections by the density gradient method [25, 26]. Thus, the intrinsic physical variation and characteristic fluctuations can be examined properly. All statistically generated discrete dopants are incorporated into the large-scale 3D device simulation running on our parallel computing system [27–29]. It has been known that very similar DC characteristics of nanowire transistor could be maintained whenever the gate-coverage-ratio varies from 70% to 100% [23]. Nevertheless, the immunity of nanowire transistor against random-dopant-induced characteristic fluctuation may significantly suffer from the variation of gate-coverage-ratio. Our results show that the influence of non-ideal gate-coverage ratio disturbs the channel controllability of nanowire transistors and thus decreases the immunity against discrete-dopant-induced fluctuation. Increase of characteristic fluctuation reveals the importance of gate-coverage ratio on nanowire device's immunity against discrete-dopant-induced fluctuation.

The paper is organized as follows. In Section 2, a statistically sound "atomistic" approach for analyzing the random impurity effect in nanoscale device is introduced. In Section 3, discrete-dopant-induced characteristic fluctuations of nanowire transistor with surrounding- and omega-gate structures are examined. Finally we draw conclusions.

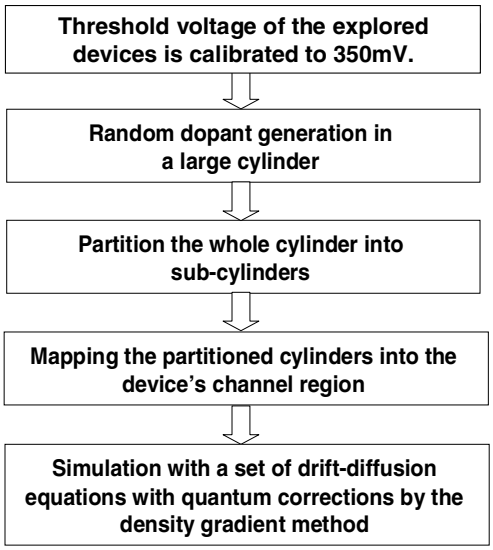

Figure 1 A simulation flow of the presented 3D statistically sound "atomistic" approach to analyze random dopant effect in nanodevices. The physical parameters used in the 3D DD equations are quantitatively verified with the experimental data of planar and nanowire devices [10, 11, 22, 30]. The large-scale computation is conducted in our cluster system [29].

2 Simulation techniques The simulation flow is shown in Fig. 1; to have the same device's operation point, the threshold voltage of the explored devices is calibrated to 350 mV. The nominal channel doping concentration of the studied is 1.48×10^{-18} cm^{-3}. They have a 16 nm gate, an 8 nm diameter and a gate oxide thickness of 1.2 nm. Outside the channel, the doping concentrations in the source and drain are 3×10^{20} cm^{-3}. This study considers the n-type silicon nanowire transistors, where boron dopants are used in the p-type channel. For the simplicity, only those dopants within the channel region are treated discretely. Inside the discrete dopant region, to include the effect of random fluctuation of the number and position of discrete dopants, we first generate a large number of dopants in a long cylinder solid, in which the equivalent doping concentration is equal to 1.48×10^{-18} cm^{-3}. The long cylinder solid is then partitioned into sub-cylinders with 16 nm gate. Each partitioned sub-cylinders are mapped into device channel region for the 3D "atomistic" device simulation. Characteristics of each device with discrete dopants are calculated by solving a set of 3D DD equations with quantum corrections by the density gradient method [25, 26]. In "atomistic" device simulation, the resolution of individual charges within a conventional DD simulation using a fine mesh creates problems associated with singularities in the Coulomb potential. The density gradient approximation is used to handle discrete charges by properly introducing the related quantum mechanical effects [26].

Figure 2(a) shows 149 dopants randomly generated in a 2000 nm length cylinder, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}. The whole cylinder is then partitioned into 125 sub-cylinders, where each sub-cylinder is with 16 nm length. The number of dopants in the sub-cylinder may vary from zero to five, and the average number is equal to one, as shown in Fig. 2(b)–(d), respectively. These 125 sub-cubes are then mapped into the channel region of the device with different gate-coverage-ratio for the discrete dopant simulation, as shown in Fig. 2(e)–(g). All statistically generated discrete dopants are incorporated into the large-scale 3D device simulation running on the parallel computing system [27–29]. According to this analyzing scenario, only channel dopants are treated discretely. The doping concentrations remain continuous in the source/drain region because the volume of source/drain region is two-order magnitude greater than that of channel region. With this respect the present simulations give a qualitative result. Nevertheless, this approach

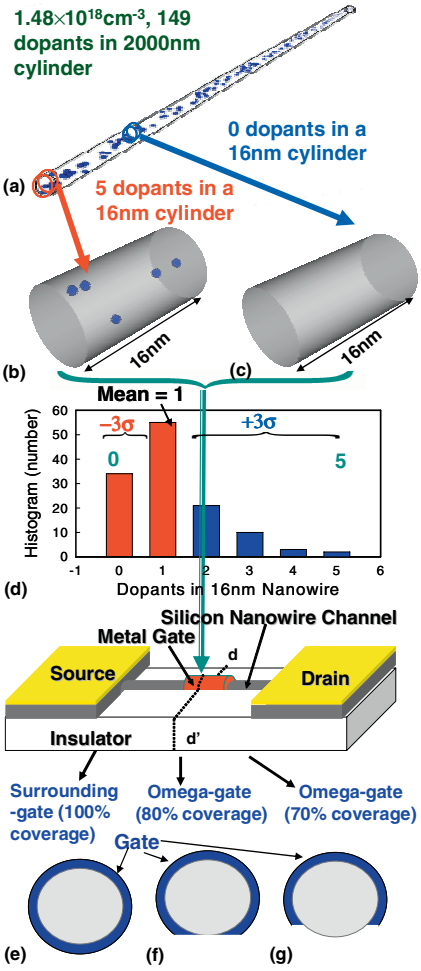

Figure 2 (online colour at: www.pss-a.com) (a) Discrete dopants randomly distributed in the 2000 nm length cylinder with the average concentration of 1.48×10^{18} cm^{-3}. There will be 149 dopants within the cylinder and the number of dopants may vary from 0 to 5 (the average number is 1) within its 125 sub-cylinders of 16 nm length (plots of (b), (c), and (d)). These sub-cylinders are then equivalently mapped into the channel region (plots of (e), (f), and (g)), for discrete dopant simulation. We notice that the explored device now has different gate-coverage-ratios, they are (e) the surrounding-gate (i.e., 100% coverage), (f) the omega-gate with 80% coverage-ratio, and (g) the omega-gate with 70% coverage-ratio.

allows us to focus on the study of characteristic fluctuations induced by the randomness of the number and position of dopants in the channel simultaneously. The statistically sound 3D "atomistic" device simulation technique is also computationally cost-effective. We notice that the mobility model used in the device simulation, according to Mathiessen's rule [31, 32], is expressed as:

$$\frac{1}{\mu} = \frac{D}{\mu_{\text{surf-aps}}} + \frac{D}{\mu_{\text{surf-rs}}} + \frac{1}{\mu_{\text{bulk}}}, \tag{1}$$

where $D = \exp(x/l_{\text{crit}})$, x is the distance from the interface and l_{crit} is a fitting parameter. The mobility consists of three parts: (i) The surface contribution due to acoustic phonon scattering

$$\mu_{\text{surf-aps}} = \frac{B}{E} + \frac{C(N_i/N_0)^{\tau}}{E^{1/3}(T/T_0)^K}, \tag{2}$$

where N_i is the total concentration of ionized impurities, $T_0 = 300$ K, E is the transverse electric field normal to the interface of semiconductor and insulator, B and C are parameters which are based on physically derived quantities, N_0 and τ are fitting parameters, T is lattice temperature, and K is the temperature dependence of the probability of surface phonon scattering. (ii) The contribution attributed to surface roughness scattering is

$$\mu_{\text{surf-rs}} = \left(\frac{(E/E_{\text{ref}})^{\Xi}}{\delta} + \frac{E^3}{\eta} \right)^{-1}, \tag{3}$$

where $\Xi = A + (\alpha(n+p)\, N_{\text{ref}}^{\nu})/((N_i + N_1)^{\nu})$, $E_{\text{ref}} = 1$ V/cm is a reference electric field to ensure a unitless numerator in $\mu_{\text{surf-rs}}$, $N_{\text{ref}}^{\nu} = 1$ cm^{-3} is a reference doping concentration to cancel the unit of the term raised to the power ν in the denominator of Ξ, δ is a constant depending on the details of the technology, such as oxide growth conditions, $N_1 = 1$ cm^{-3}, A, α and η are fitting parameters. (iii) The bulk mobility is

$$\mu_{\text{bulk}} = \mu_{\text{L}} \left(\frac{T}{T_0} \right)^{-\xi}, \tag{4}$$

where μ_{L} is the mobility due to bulk phonon scattering and ξ is a fitting parameter. The mobility model is quantified with measured data of different FETs in our earlier work [10–13, 22, 29, 30] for the best accuracy.

3 Results and discussion This section first discusses the fluctuations of potential and current density due to discrete dopants; and then the impact of non-ideal nanowire gate-coverage ratio on immunity against discrete-dopant-induced fluctuations is studied. The on-state (the device is with the drain voltage $V_{\text{D}} = 1$ V and the gate voltage $V_{\text{G}} = 1$ V) potential distribution of the discretely doped case, shown in Fig. 3(a), and (b), are investigated to elucidate the effect of discrete dopant on the potential and current distributions of the device. The potential fluctuations, shown in Fig. 3(b), are associated with the corresponding dopants in Fig. 3(d).

Comparison between Fig. 3(e) and (f) reveals that the current conducting path is disturbed and impeded by the discrete dopants locating at the channel. Since the potential distribution near the dopant is relatively negative in the channel, the dopant acts as a centre of a whirlpool-like electric field to repel electrons. As electrons transport from the end of source to the drain side, some of them will encounter a negative electric field that is induced by the discrete dopants. The lateral electric field between the source

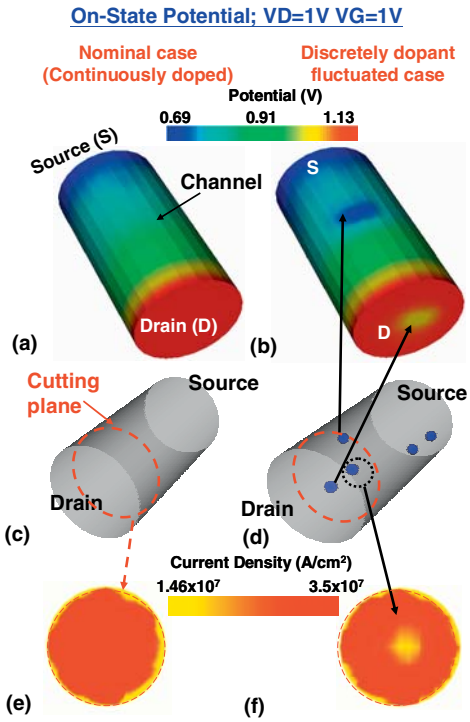

Figure 3 (online colour at: www.pss-a.com) Comparison of the on-state potential (a), (b) and the current density distributions (e), (f) of (c) the nominal case and (d) discretely doped cases. The potential fluctuations are induced by corresponding dopants in (d).

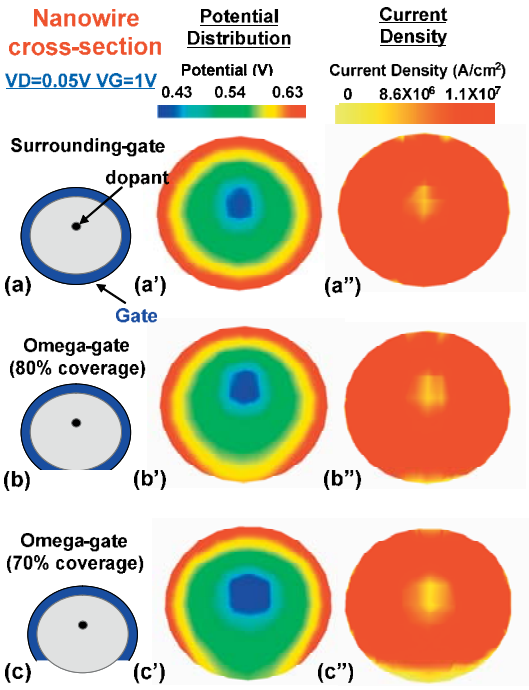

Figure 4 (online colour at: www.pss-a.com) Comparison of potential (plots of (a′), (b′), and (c′)) and current density distribution (plots of (a″), (b″), and (c″)) in nanowire transistors with surrounding-gate (100% gate-coverage-ratio) and omega-gate (80% and 70% gate-coverage-ratio) structures.

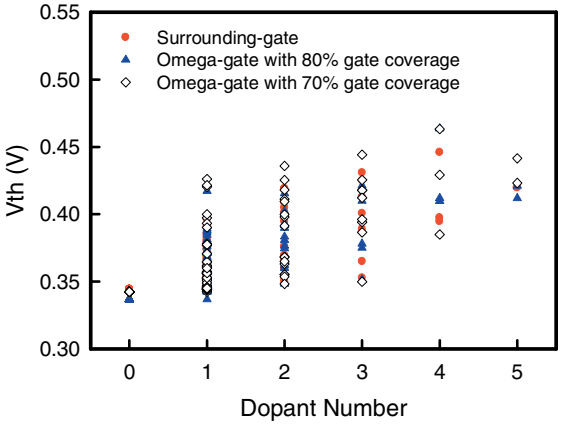

Figure 5 (online colour at: www.pss-a.com) Comparison of the threshold voltage (V_{th}) fluctuation of the 16 nm gate silicon nanowire FET with surrounding-gate, omega-gate with 80%, and 70% gate-coverage-ratio.

and the drain, combined with the repulsion of the dopants, twists the electric field and increases the electron velocity near the dopants. The potential fluctuations not only alter the electric field and current conducting path, but also the electron velocity, and carrier mobility.

Figure 4 shows the comparisons of potential and current density distributions, respectively, for the nanowire transistors with the surrounding-gate (i.e., 100% gate-coverage-ratio) and the omega-gate (i.e., 80% and 70% gate-coverage-ratios) structures. The discrete dopants positioned in the channel induce a potential fluctuation and substantially disturbs the current density distribution and the corresponding conduction path. The magnitude of potential and current density fluctuations is increased as the gate-coverage-ratio decreases. The non-ideal gate-coverage disturbs the channel controllability of the explored nanowire transistors and thus decreases the immunity against discrete dopant induced fluctuation.

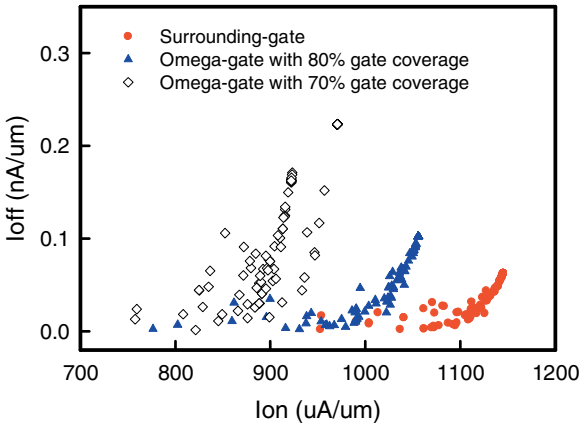

Figure 6 (online colour at: www.pss-a.com) Comparison of the on−off state current ($I_{on} - I_{off}$) fluctuation of the 16 nm gate silicon nanowire FET with surrounding-gate, omega-gate with 80%, and 70% gate-coverage-ratio.

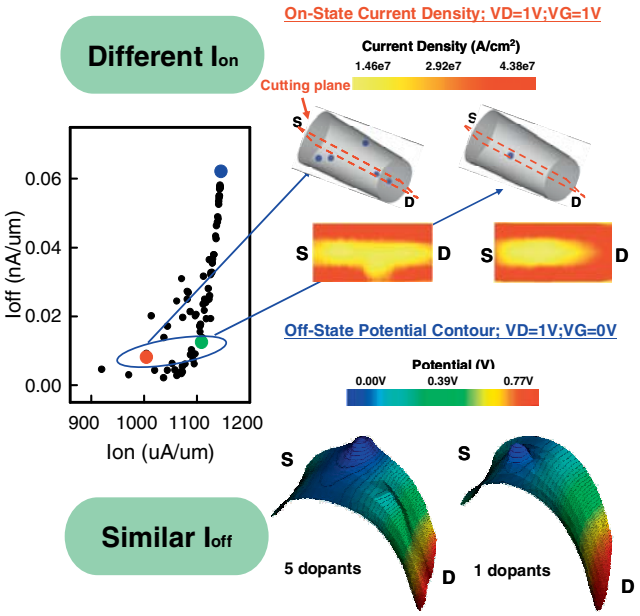

Figure 7 (online colour at: www.pss-a.com) Effect of Discrete-Dopant-Position in silicon nanowire FET, where the devices are with different I_{on} but similar I_{off}.

In our study, for a 16 nm gate silicon nanowire transistor, the threshold voltage fluctuations of the omega-gate devices with 80% and 70% gate-coverage are 1.04 and 1.19 times larger than that of the surrounding-gate structure, as shown in Fig. 5. For current fluctuations, the ratio is 1.75 and 4.5 times larger than that of the surrounding-gate one, as shown in Fig. 6. The results confirm that the influence of non-ideal gate-coverage on the disturbances of the channel controllability of nanowire transistors. The immunity against discrete dopant induced fluctuation is thus decreased.

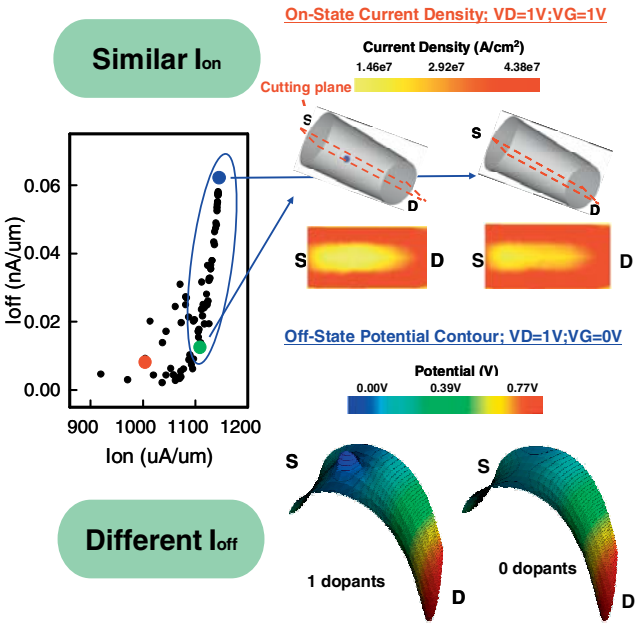

Figure 8 (online colour at: www.pss-a.com) Effect of Discrete-Dopant-Position in silicon nanowire FET, where the devices are with similar I_{on} but different I_{off}.

Figure 7 shows the characteristics of the on-state and off-state currents ($I_{on} - I_{off}$). For those cases with similar I_{on}, the maximum fluctuation of I_{off} is within 0.05 nA/um. This figure discloses three different discrete-dopant channels, having similar values of I_{on} or I_{off} but with various dopant positions. The cross-sectional on-state current density and off-state potential distributions extracting from the centre of channel are examined. Due to the difference of discrete dopant position, the different conduction paths of devices result in different on-state currents even we have very similar off-state currents, shown in Fig. 7. For the device having very similar on-state current with different off-state situations, Fig. 8 shows the off-state potential distribution at device's channel. However, due to the effect of discrete dopant position, there is no potential barrier located in the channel region.

4 Conclusion In this study, a 3D statistically sound cost-effective "atomistic" approach for analyzing random dopant effect in nanowire devices has been presented. Discrete dopants are statistically positioned into the channel region to examine the associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". This study also investigated the impact of non-ideal nanowire gate-coverage ratio on immunity against discrete-dopant-induced fluctuations. The results have confirmed that the influence of non-ideal gate-coverage disturbs the channel controllability of nanowire transis-tors and thus decreases the immunity against discrete dopant induced fluctuation. The increase of fluctuation shows that the importance of gate-coverage ratio on nanowire device's immunity against discrete-dopant-induced fluctuation.

As dimension of device scales, the particular distribution of dopants in channel is not so obvious. Thus, we assumed a uniform distribution of dopants in this study. Moreover, we noted that the simulation results will be more accurate and give more physical insight if the positions of Si atoms are replaced with Boron dopants in device simulation. However, this may require huge computation time; for example, the adopted large-scale 3D simulation had cost about three months. The more physical assumption requires much more huge computation time. We are planning to conduct such an investigation in our future work.

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