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The Enhancement of Nitrogen Incorporation in RTN_2O Annealed TEOS Oxide Fabricated on Disilane-Based Polysilicon Films

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Disilane-based stacked structures were first proposed to demonstrate that the nitrogen incorporation was enhanced in the RTN_2O annealed tetraethylorthosilicate (TEOS) oxide fabricated on disilane-based polysilicon films. Compared with the oxide fabricated on the silane-based polysilicon film, the nitrogen incorporation in the disilane-based oxides is six times higher. To study the nitrogen incorporation effects on the RTN_2O annealed TEOS oxides, the disilane-based polysilicon stacked on the silane-based polysilicon film structure was proposed. We found that the oxide quality was largely improved by the same surface morphology of bottom polysilicon films. We think the this approach could be used in fabricating dynamic random access memory (DRAM) to have better data retention characteristics and to improve the reliability of DRAM and flash memory devices.
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Polyoxide with a low leakage current and a high stress endurance capability is essential in obtaining good data retention characteristics of the novel dynamic random access memory (DRAM) and flash memory devices. However, polyoxide has a higher leakage current and a relatively lower breakdown field than oxides grown on single crystalline silicon.[1-4]

Recently, the ONO (oxide/nitride/oxide) stacked films were widely used as an interpoly dielectric in fabricating DRAM and flash memory devices because of its low leakage current and good electrical endurance capability. Unfortunately, the stacked structure suffers a scaling down problem.[5] To obtain a highly reliable thin polysilicon insulator, the tetraethylorthosilicate (TEOS) oxides being nitrided in N_2O ambient by rapid thermal process were proposed.[6] The quality of the nitrided TEOS oxides, however, was found to be highly dependent on the surface morphology of the polysilicon films on which they were deposited. According to this correlation, the polysilicon films with a smooth surface were fabricated to produce highly reliable polyoxides. Discouragingly, reducing the surface roughness of the polysilicon will reduce the capacitance of the capacitor, therefore limiting its application to fabricating DRAM devices. The nitrogen incorporation also strongly affected the quality of the oxides; that is, increasing the nitrogen incorporation increased the reliability of the nitrided TEOS polyoxides. Therefore, in order to improve the quality of TEOS oxide without changing the surface morphology of polysilicon, a higher nitrogen incorporation is needed.

The nitrided oxides fabricated on the disilane-based polysilicon films were proposed in our previous work.[7] In that work, we found that the fabricated polyoxides had better reliability than the conventional ones. The improvement could be due to the smoother surface of the bottom disilane-based polysilicon films and the higher nitrogen incorporation of the prepared oxides; however, the effects of those factors were mixed together.

In this paper, the disilane stacked polysilicon film structures are proposed to demonstrate higher nitrogen incorporation. As a result, the proposed oxide was found to have better reliability without changing the surface morphology of bottom polysilicon films, mainly with the much higher nitrogen incorporation.

Experimental

At first, two conventional polysilicon films 2000 Å thick were prepared by two different deposition conditions. The polysilicon with a rough surface was deposited using silane gas at 620°C in low pressure ambient and the smooth polysilicon was deposited by using disilane gas at 470°C. Then the polysilicon films were implanted with a phosphorus dose of 5×10^{15} at energy of 30 keV and annealed at 950°C in a rapid thermal N_2 ambient for 30 s. The sheet resistance for conventional polysilicon films deposited by silane and disilane were 130 and 70 Ω/□, respectively. In addition, the surface roughness (rms) measured from atomic force microscope (AFM) indicated that it is 30 Å for silane deposited film and 3 Å for disilane deposited film.

The stacked polysilicon films were fabricated by depositing a 300 Å nondoped polysilicon film on the previous prepared conventional polysilicon films by using disilane gas at 470°C in a low pressure furnace ambient. The sheet resistance and the surface roughness of the stacked films were the same with the conventional films (*i.e.*, 130 Ω/□ and 30 Å of disilane stacked on silane polysilicon film, 70 Ω/□ and 3 Å of disilane stacked on disilane polysilicon film, respectively.)

The two conventional polysilicon films and two kinds of stacked polysilicon films were prepared as the polyIs of the capacitors. After the polyIs was prepared, they were RCA cleaned and deposited on a 100 Å TEOS oxide. After the oxide deposition was completed, all samples were annealed at 950°C in a rapid thermal N_2O ambient (RTN_2O) and the final thickness of the oxides was 130 Å.

All samples were then deposited with a 3000 Å polysilicon film to be used as the gate material (polyII) by using silane gas at 620°C in a low pressure ambient. Then, the polysilicon films were $POCl_3$ doped at 850°C in a N_2 ambient for 1 h to achieve a sheet resistance of 40 Ω/□. The polyIIs were then patterned and grown with a 1000 Å passivation oxide. After contact holes of polyIs and polyIIs were opened, Al film was deposited, patterned, and sintered at 350°C for 40 min in an N_2 ambient to be used as the electrodes of the capacitors.

The sheet resistance was measured by using the four-point probe method, the surface rms was measured by atomic force microscopy (AFM) and thickness was determined by capacitance voltage (CV) measurement. Finally, we used HP 4145b to measure the J-E, E_{bd},Q_{bd}, and the electron trapping characteristics.

Results and Discussion

Figure 1 shows the AFM images of the polyI surfaces of the nonstacked polysilicon films and the stacked ones. They are (a) S the polysilicon deposited by using silane, (b) D the polysilicon deposited by using disilane, (c) SD the silane-based polysilicon stacked with disilane-based polysilicon, (d) DD the disilane-based polysilicon stacked with disilane-based polysilicon, (e) SS the silane-based polysilicon stacked with silane-based polysilicon, and (f) DS the disilane-based polysilicon stacked with silane-based polysilicon. We can easily find that the surface roughness (rms) of the nonstacked films, graphs (a) and (b), and the disilane-stacked films, graphs (c) and (d) are nearly the same, respectively. This implies that the top disilane film does not affect the surface roughness of the polysilicon films. On the other hand, the surface roughness of the DS sample is rougher than the DD and the D samples. The increase

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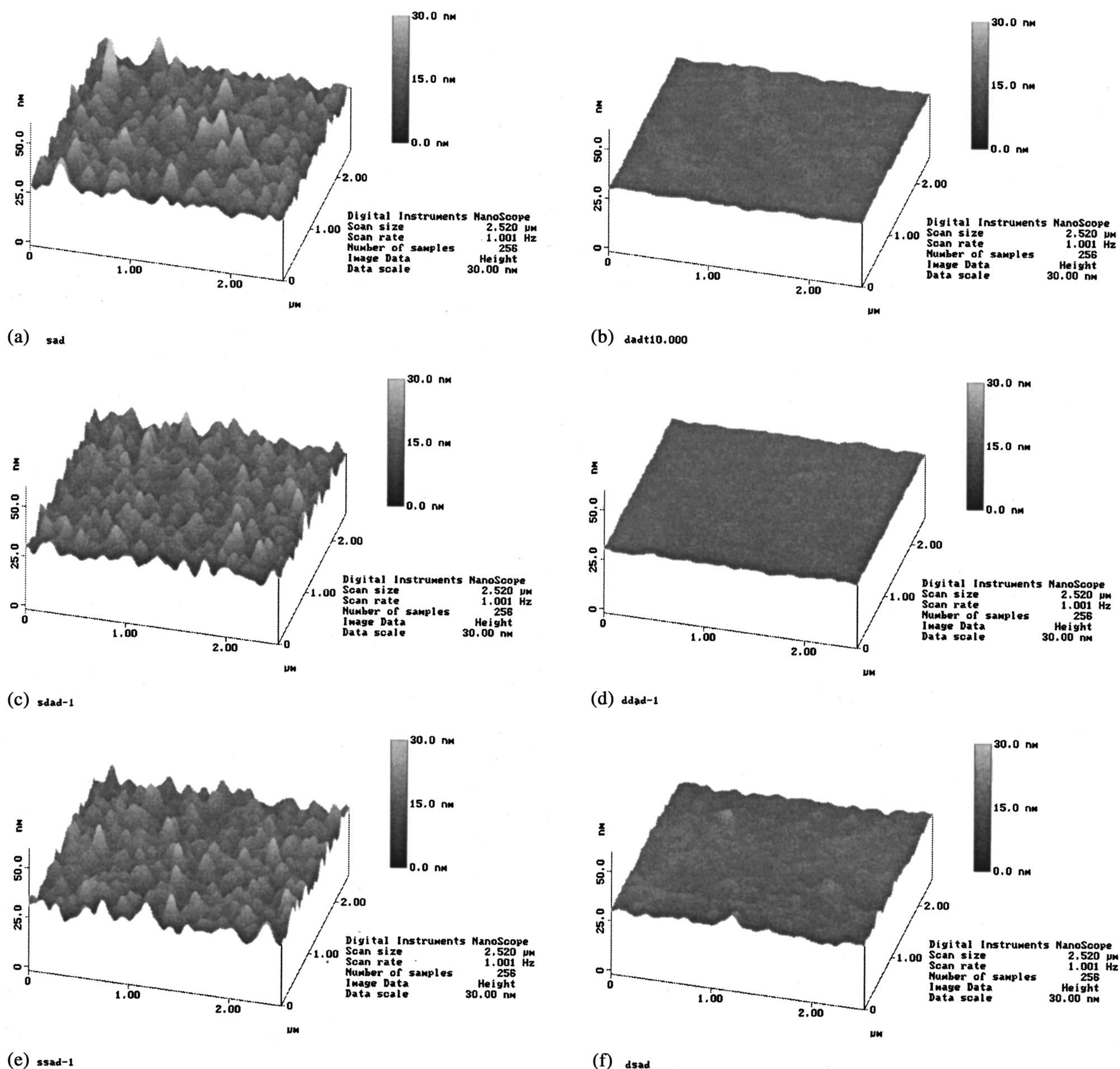

Figure 1. AFM images of the (a) S (silane), (b) D (disilane), (c) SD (silane stacked with disilane), (d) DD (disilane stacked with disilane), (e) SS (silane stacked with silane) and (f) DS (disilane stacked with silane). The rms of the surface roughness is 3, 0.3, 3, 0.3, 3, and 1.3 nm, respectively.

of the roughness resulted from the higher nucleation rate occurring during the polysilicon deposition at higher temperature. It can be seen that the surface roughness of disilane polysilicon increases from 3 to 13 Å after adding a 300 Å silane-based polysilicon as shown in (f). Nevertheless, to maintain the integrity of polyoxide, the stacked films (e) and (f) deposited by using silane were not performed in this research.

Figure 2 shows the nitrogen (N) and phosphorus (P) SIMS profiles of the stacked and the nonstacked samples. The P concentration in the top disilane-based films was slightly higher than that in the lower conventional polysilicon films. This means that the top disilane films could be unintentionally doped during the following thermal process. The N profiles are also presented in this figure. The N concentration in the disilane (D), the disilane/disilane (DD), and the silane/disilane (SD) samples is much higher than that of the silane (S) sample. The result indicates that the N atoms are easier to incorporate into the disilane-based polysilicon film than into the silane-based polysilicon film. This should be due to the fact that relatively lower activation energy is enough to form bonding between silicon and nitrogen impurities for the disilane-based polysilicon. The variation activation energy for the silane-based and disilane-based films could be caused by the microstructural difference of these two films, which has been studied in Ref. 8. The microstructural difference of disilane-based and silane-based films is shown in Fig. 3; this figure presents that the dominant structures are ⟨110⟩ and ⟨111⟩ for silane sample while ⟨111⟩ for disilane.

The disilane stacked on disilane (DD) sample has a slightly higher N concentration than the disilane stacked on silane (SD) sample in the polyoxide, which could be ascribed to the smooth surface of the disilane samples. Therefore, the N profile of the DD sample is much sharper than that of the SD sample.

Figure 4 shows the TEM of the (a) DD and (b) SD samples. We can find that the disilane-based polysilicon film is conformal stacked on the conventional polysilicon films. This explains why the nonstacked films have similar surface roughness to the disilane stacked films. Additionally, the interface between the top disilane stacked

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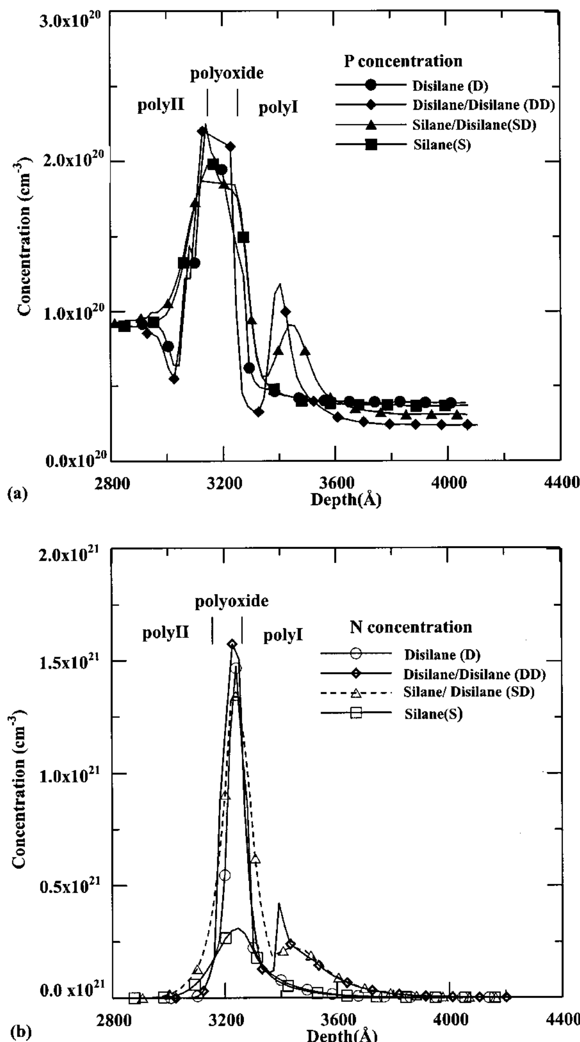

Figure 2. SIMS profiles of the (a) phosphorus, (P) count, and (b) nitrogen (N) count of the disilane (D), disilane stacked with disilane (DD), silane stacked with disilane (SD), and silane (S), respectively.

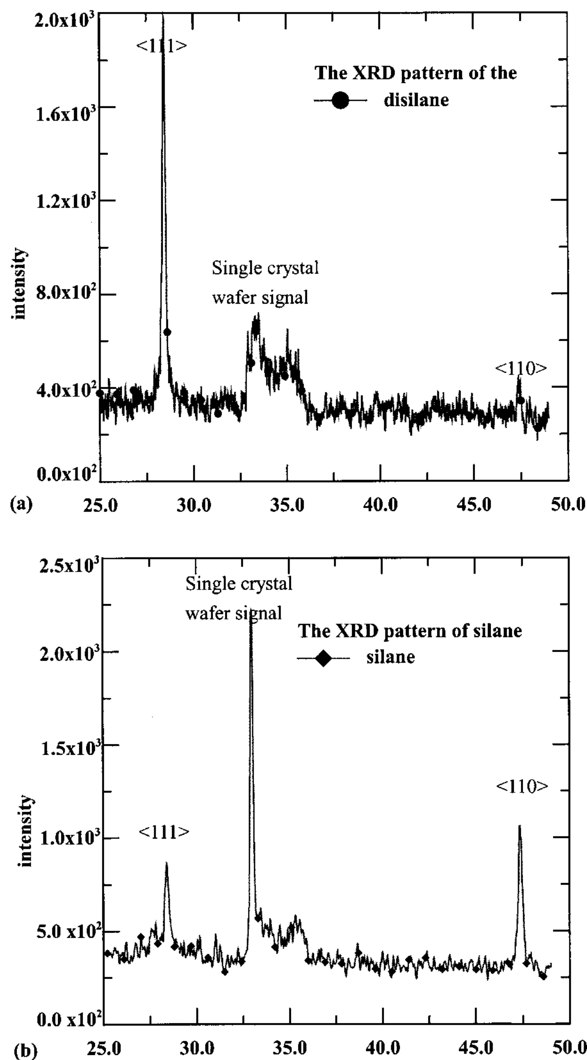

Figure 3. XRD patterns of the (a) disilane and (b) silane samples.

film and bottom conventional films could be observed clearly. With this interface, the impurities that reduce oxide reliability could be trapped; therefore, improve the reliability of the oxides.

Figure 5 shows the *J-E* characteristics of the (a) D and DD, (b) S and SD samples with both polarities. We found that the stacked structure could improve the leakage characteristics of the oxides; especially for S and SD samples.

Figure 6 shows the effective barrier heights of the oxides, which were extracted from the *J-E* characteristics by using the method mentioned in Ref. 10. The figure indicates that the oxides deposited on the stacked structure polysilicon films have higher barrier height than those deposited on the nonstacked polysilicon films do. This is especially true when the polyIIs are positively biased. The improvement can be attributed to the fact that, while the oxides annealed in rapid thermal N_2O ambient, the bottom conventional polysilicon films being isolated by the top disilane stacked polysilicon film. Therefore, a 30 Å higher quality N_2O grown thermal oxide could be achieved by preventing it from contacting with the defects, which remained in bottom conventional polysilicon films during doping process (*i.e.*, implantation and rapid thermal annealing). Note that the difference between the S and SD samples is much larger than the difference between D and DD samples. The result could be because there is much higher nitrogen incorporation in the SD sample than that in the S sample while similar nitrogen distribution of the D and DD samples is shown in Fig. 2.

Figure 7 shows the Weibull plots of the electric field to breakdown (E_{bd}) of the (a) D and DD, (b) S and SD with both polarities. We found that the disilane-stacked films have better E_{bd} characteristic than the nonstacked ones, especially for the SD and S samples.

Figure 8 shows the trapping charge characteristics of the (a) DD and D and (b) SD and S samples (the stress current density is 1 mA/cm^2). We found that the stacked samples have a lower electron-trapping rate, and therefore, higher Q_{bd} distributions. The figure also presents that the DD, SD, and D samples have hole trapping while polyII is positively stressed. This indicates that those samples have higher N incorporation within the oxides because similar phenomenon were observed for the reported nitrogen-rich oxides prepared by N_2O or NO.[9,10]

Figure 9 presents the Weibull plots of the charge to breakdown (Q_{bd}) (the stress current density is 10 mA/cm^2) of the stacked and the nonstacked samples, they are (a) D and DD, (b) S and SD with both polarities. The stacked samples have a higher Q_{bd} distribution, that is, the disilane-based stacked films can improve the quality of polyoxides. Roughly speaking, the disilane-based stacked oxides are improved about two orders of magnitude in Q_{bd} than that of the nonstacked silane polyoxide and about one order of magnitude than that of the nonstacked disilane polyoxide. The improvement can be attributed to the fact that, while depositing or annealing TEOS ox-

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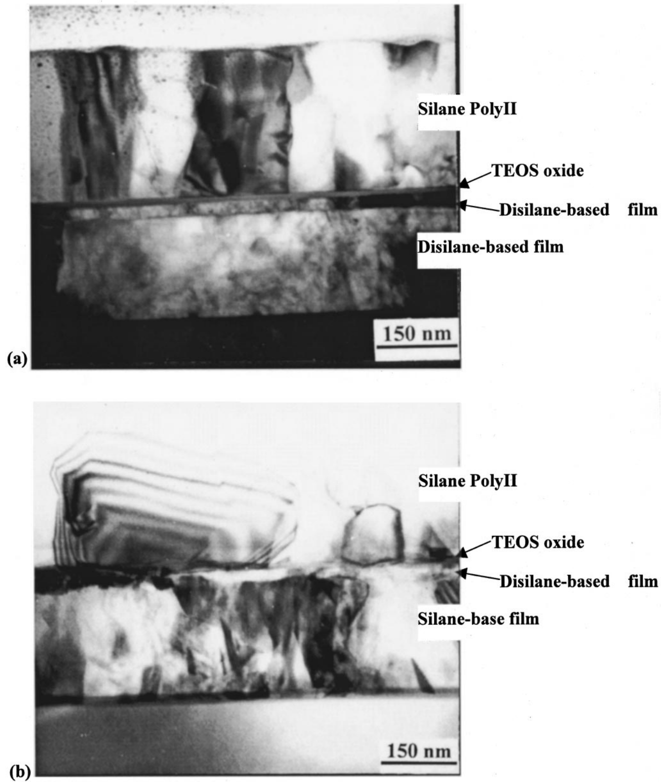

Figure 4. TEM images of the (a) DD (disilane stacked with disilane) and (b) SD (silane stacked with disilane) samples.

ides, the bottom polysilicon films being isolated by the top disilane polysilicon film. Therefore, the polyoxide layers can prevent themselves from contacting with the defects, which remain in the lower conventional polysilicon during doping process. Moreover, the higher N concentration incorporated into polyoxide can be another factor in improving the quality of the silane polyoxide, which can be observed with the SIMS profiles in the Fig. 2.

Conclusions

The TEOS oxides deposited on disilane-based polysilicon films were shown to have higher nitrogen incorporation. The enhancement could be due to the microstructure difference between the disilane-based and silane-based polysilicon films. The higher nitrogen incorporation could improve the characteristics of the oxides; therefore, with the disilane-based polysilicon film stacked structure, the polyoxides could have better quality without changing the surface roughness of the polysilicon.

The effects on the defects and impurities produced during implantation process were also found to be eliminated by adding this thin film.

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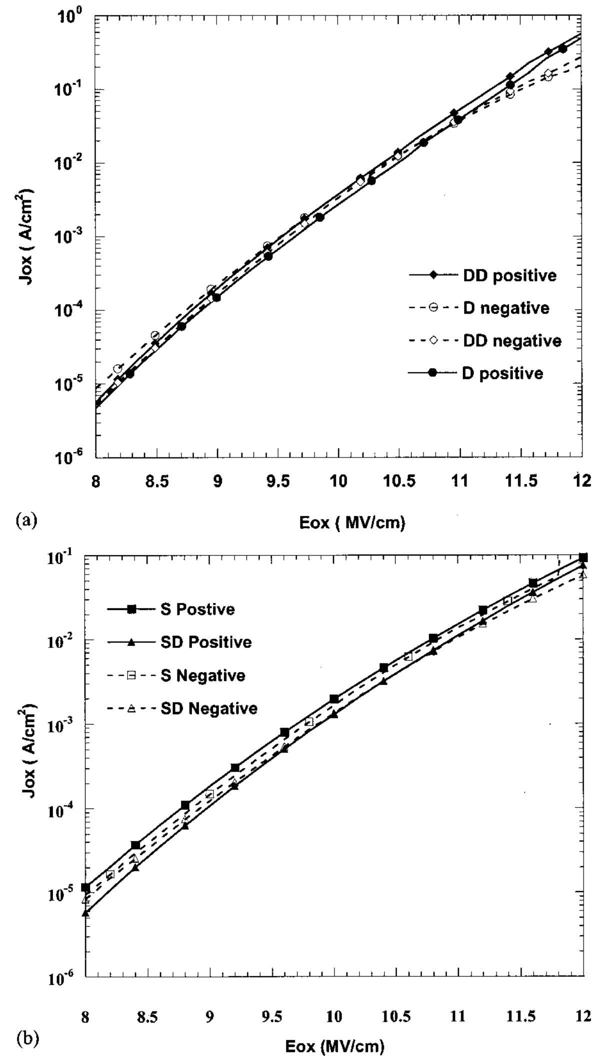

Figure 5. J-E characteristics of the (a) D and DD, (b) S, and SD samples with both polarities.

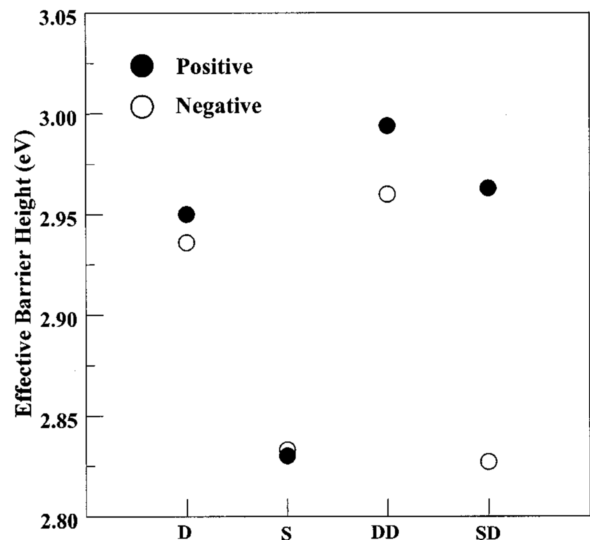

Figure 6. The effective barrier height of the four prepared oxide samples with both polarities.

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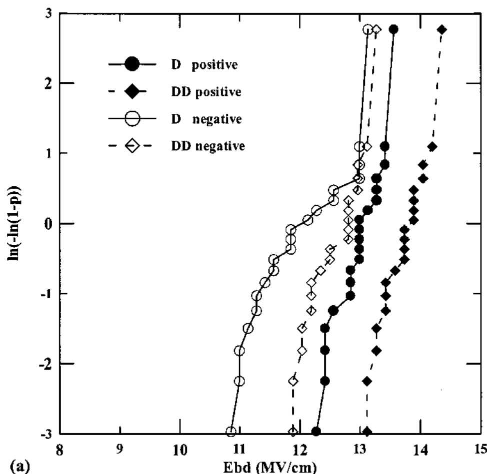


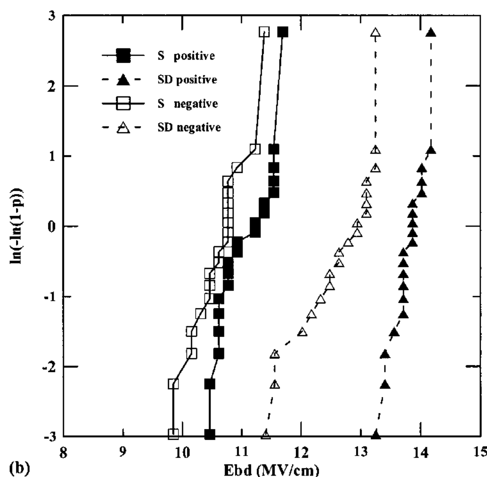
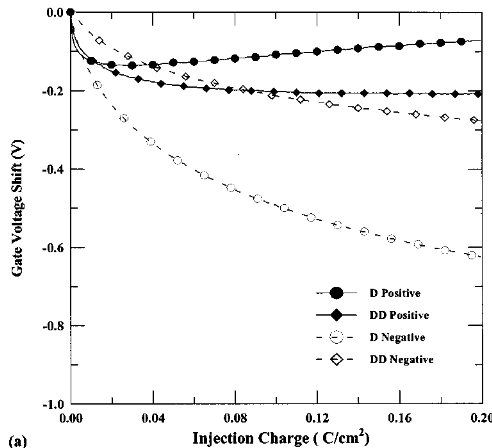


Figure 7. The Weibull plots of E_{bd} of the (a) D (disilane) and DD (disilane stacked with disilane) samples with both polarities, (b) S (silane) and SD (silane stacked with disilane) samples with both polarities.



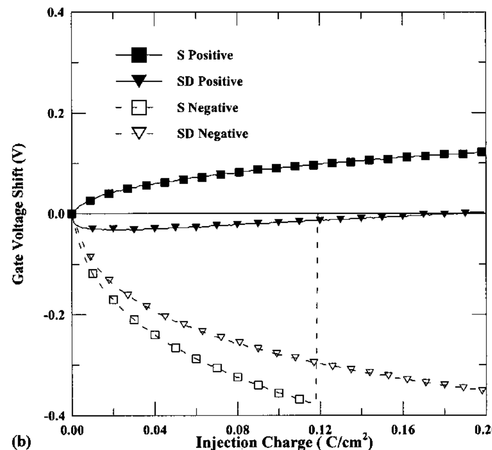
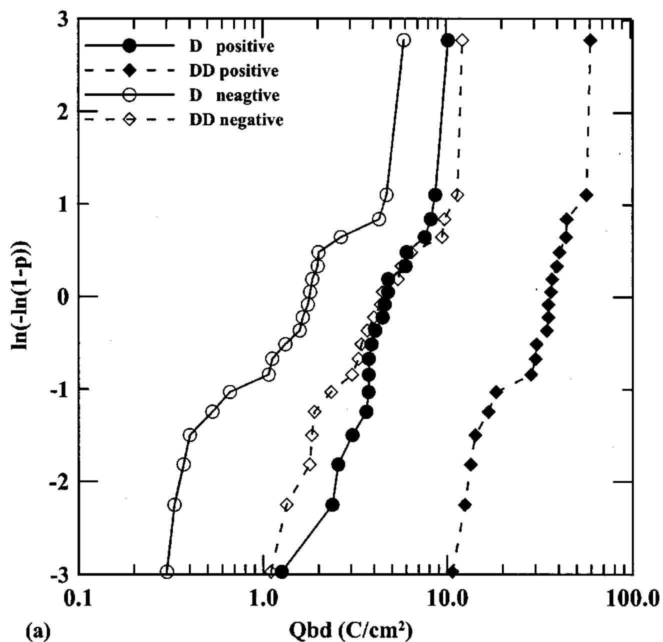


Figure 8. Charge trapping characteristics of the prepared samples. (a) DD and D, (b) SD and S samples with both polarities. The stressed current is 1 mA/cm^2. The injection charge is calculated from the formula $q = J$ (A/cm^2)t(s). The gate voltage shift is calculated from the formula delta $V(t) = V(t) - V(t = 0)$.



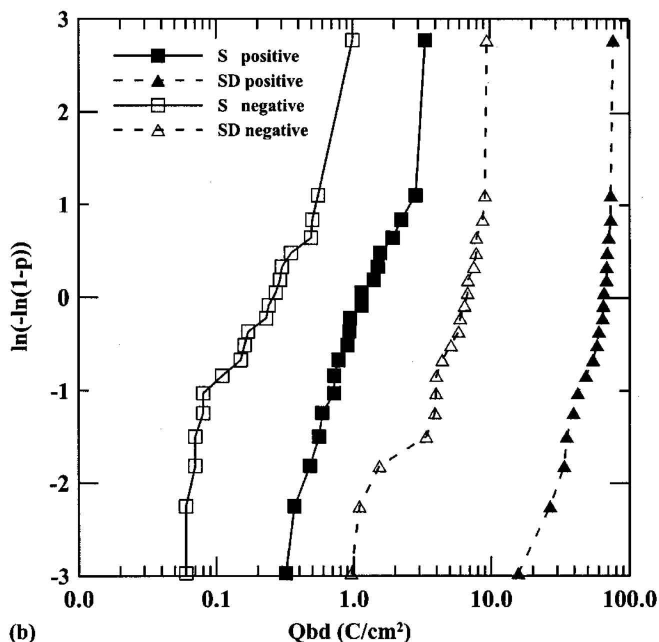


Figure 9. The Weibull plots of Q_{bd} of the (a) D (disilane) and DD (disilane stacked with disilane) samples with both polarities, (b) S (silane) and SD (silane stacked with disilane) samples with both polarities.

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