Low-Capacitance SCR With Waffle Layout Structure for On-Chip ESD Protection in RF ICs

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***Abstract*—The silicon-controlled rectifier (SCR) has been used as an effective on-chip electrostatic discharge (ESD) protection device in CMOS technology due to the highest ESD robustness in nanoscale integrated circuits (ICs). In this study, the SCR realized in a waffle layout structure is proposed to improve ESD current distribution efficiency for ESD protection and to reduce the parasitic capacitance. The waffle layout structure of the SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs. Besides, the desired current to trigger on the SCR device with a waffle layout structure and its turn-on time has also been investigated in a silicon chip.**

***Index Terms*—Electrostatic discharge (ESD), RF integrated circuit (RF IC), silicon-controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC discharge (ESD), which is the major reliability issue for integrated circuits (ICs), must be taken into consideration during the design phase of all ICs. In nanoscale CMOS technologies, the thinner gate oxide in the advanced processes greatly degrades the ESD robustness of IC products. Against ESD damages, ESD protection devices must be included in ICs [1]–[3]. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [4]–[6]. The ESD protection devices must be provided for all I/O pads in RF ICs. The parasitic capacitance ($C_{\rm ESD}$) of the ESD protection device is one of the most important design considerations for RF ICs [7]–[10]. The parasitic capacitance of ESD protection devices will degrade the high-frequency performance of RF ICs. The ESD protection device realized in the conventional stripe layout structure often has a large parasitic capacitance which may not be tolerated in RF ICs. The parasitic capacitance induces *RC* delay on the signal path and lowers the operating frequency of RF ICs. Moreover, the parasitic capacitance of the ESD protection device loses RF signals from the pad to ground. For RF receivers, the noise figure (NF) is an important merit. Adding ESD protection devices to the RF receiver had been proven to degrade the NF [11]. For example, the overall NF of the low-noise amplifier (LNA) with ESD protection device in Fig. 2 is

$$\mathrm{NF}_{\rm total} = \mathrm{NF}_{\rm ESD} + \frac{\mathrm{NF}_{\rm LNA} - 1}{L^{-1}} = L \cdot \mathrm{NF}_{\rm LNA} \qquad (1)$$

where L is the power loss of the ESD protection device, and $\mathrm{NF}_{\rm LNA}$ and $\mathrm{NF}_{\rm ESD}$ denote the NFs of the LNA and ESD protection device, respectively. The NF of the ESD protection device is equal to its power loss because the ESD protection device is a passive reciprocal network [12]. To mitigate the RF performance degradation caused by the ESD protection device, its parasitic capacitance must be minimized. Therefore, devices with a large ratio of ESD robustness to parasitic capacitance are desired. The figure-of-merit (FOM) used in this paper is $V_{\rm MM}/C_{\rm ESD}$, where $V_{\rm MM}$ is the machine-model (MM) ESD level and $C_{\rm ESD}$ is the parasitic capacitance of the ESD protection device.

With the highest ESD robustness within a smaller layout area and lower parasitic capacitance, the silicon-controlled rectifier (SCR) device was reported to be useful for RF ESD protection design [13], [14]. The SCR device has very low holding voltage ($V_{\rm hold}$, approximately $\sim$1.5 V in general bulk CMOS processes) so the power dissipation (power $\cong I_{\rm ESD} \times V_{\rm hold}$) and the joule heating at the SCR device during ESD stresses are significantly less than that at other ESD protection devices such as the diode, MOS, bipolar junction transistor (BJT), or field–oxide device. Therefore, the SCR device can sustain a much higher ESD level

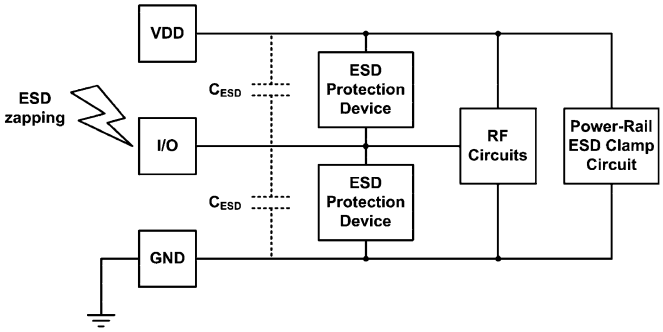

Fig. 1. General concept of on-chip ESD protection in RF ICs.

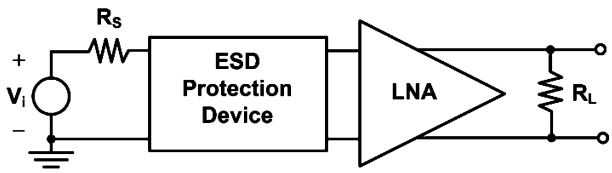

Fig. 2. Diagram of the LNA with ESD protection device.

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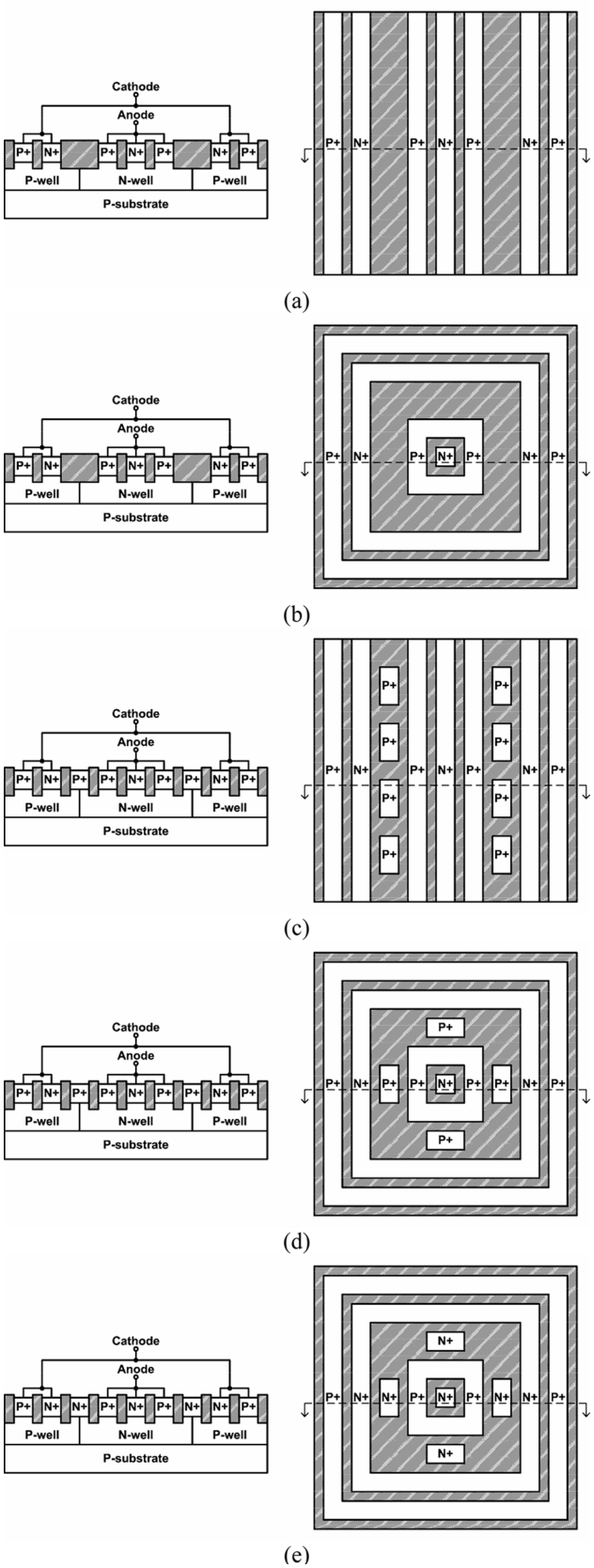

Fig. 3. Device cross-sectional view and layout top view of: (a) SSCR, (b) WSCR, (c) SPMSCR, (d) WPMSCR, and (e) WNMSCR.

within a smaller layout area in CMOS ICs [15], [16]. A smaller layout area introduces less parasitic capacitance. Thus, using an SCR device for RF ESD protection can achieve better FOM of $V_{\rm MM}/C_{\rm ESD}$. Besides, the SCR with holding voltage of approximately ∼1.5 V can be designed safely without latchup danger in advanced CMOS ICs with a low supply voltage.

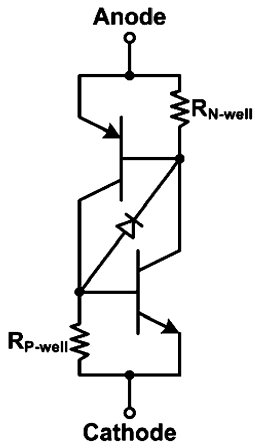

Fig. 4. Equivalent circuit of the SCR device.

The SCR device was traditionally implemented in the stripe and double-sided layout. Under ESD stresses, ESD current primarily flows through the two edges of the SCR, while the other two edges do not discharge the ESD current, but still contribute to parasitic capacitance. The proposed SCR device with a waffle layout structure can discharge ESD current through four edges. Therefore, the FOM of $V_{\rm MM}/C_{\rm ESD}$ can be maximized by using the waffle layout structure to implement the SCR.

The MOS transistors in waffle layout structures had been studied [17]. The waffle layout structures for diodes had also been proposed to reduce its parasitic capacitance for ESD protection in high-speed I/O applications [18]. In this study, the SCR realized in the waffle structure is investigated in a 0.18-μm CMOS process. With the comparison between the conventional stripe SCRs (SSCRs) and the waffle SCRs (WSCRs), the improvements from the new proposed WSCRs have been successfully verified in silicon chips [19].

II. SCR Structures

A. SCR With Stripe Layout

The conventional SSCR is shown in Fig. 3(a), which is implemented in the stripe and double-sided layout. The anode of the SSCR is electrically connected to P+ diffusion and N+ diffusion, which are formed in the N-well. The cathode is electrically connected to N+ diffusion and P+ diffusion, which are formed in the nearby P-well. The shaded regions in the cross-sectional view in Fig. 3(a) are the regions of shallow trench isolation in the CMOS process. The equivalent circuit of the SCR device, which consists of a PNP and an NPN bipolar transistors, is shown in Fig. 4. Due to the reverse-biased junction between the N- and P-well regions, the SCR device is turned off under normal circuit operating conditions. When a positive ESD stress is zapped from the anode with the cathode grounded, the high voltage drop between the anode and cathode causes breakdown on the base–collector junction of the BJT. In the meantime, PNP and NPN transistors will be turned on by the breakdown

TABLE I
COMPARISONS ON THE MEASURED DEVICE CHARACTERISTICS OF SCR UNDER DIFFERENT TEST STRUCTURES

Structure	Name	Device Size (μm^2)	Trigger Diffusion		$V_{trigger}$ (V)	R_{on} (Ω)	+/- It_2 (A)	+/- V_{HBM} (kV)	+/- V_{MM} (kV)	C_{ESD}@ 2.4GHz (fF)
			Type	Area (μm^2)						
Stripe	SSCR	60.62×60.62		0	16.92	0.95	>6 / <-6	>8 / <-8	1.80 / -0.90	118.51
Stripe	$SPMSCR_1$	60.62×60.62	P+	123.2	12.52	1.09	>6 / <-6	>8 / <-8	1.63 / -0.75	178.47
Stripe	$SPMSCR_2$	60.62×60.62	P+	242.48	12.54	1.02	>6 / <-6	>8 / <-8	1.68 / -0.95	212.81
Waffle	WSCR	60.62×60.62		0	16.17	0.96	>6 / -5.2	>8 / <-8	1.53 / -0.65	77.17
Waffle	$WPMSCR_1$	60.62×60.62	P+	70.24	11.91	1.08	>6 / -5.0	>8 / <-8	1.52 / -0.55	115.39
Waffle	$WPMSCR_2$	60.62×60.62	P+	140.48	11.81	1.10	>6 / -4.7	>8 / <-8	1.59 / -0.55	139.63
Waffle	$WPMSCR_3$	60.62×60.62	P+	264.96	12.55	1.22	>6 / -4.8	>8 / <-8	1.56 / -0.65	165.25
Waffle	$WNMSCR_1$	60.62×60.62	N+	70.24	10.08	0.99	>6 / -4.3	>8 / -7.0	1.53 / -0.65	178.67
Waffle	$WNMSCR_2$	60.62×60.62	N+	140.48	10.08	1.08	>6 / -4.1	>8 / -7.5	1.48 / -0.60	205.68
Waffle	$WNMSCR_3$	60.62×60.62	N+	264.96	11.00	1.03	>6 / -4.1	>8 / <-8	1.50 / -0.53	204.78

current. With the positive-feedback mechanism [20], [21] of the cross-coupled bipolar transistors, the SCR device becomes highly conductive. Therefore, the ESD current can be quickly discharged by the SCR device.

While a positive ESD stress is zapped from the anode with cathode grounded, the discharge path of the SCR device is P+/N-well/P-well/N+. The ESD currents primarily flow through only two edges of the N-well in the SSCR. The other two edges of the N-well in the SSCR are unused. While a negative ESD stress is zapped from the anode with cathode grounded, the discharge path in the SCR device is the parasitic N-well/P-well diode. The ESD currents still flow through only two edges of the N-well in the SSCR. The other two edges of the N-well in SSCR are not used to bypass the ESD current.

B. SCR With Waffle Layout

Fig. 3(b) shows the proposed WSCR. The anode of the WSCR is electrically connected to P+ diffusion and N+ diffusion, which are formed in the N-well. The cathode surrounds the anode, and is electrically connected to N+ diffusion and P+ diffusion, which are formed in the nearby P-well. WSCR can discharge both positive and negative ESD current in four edges of the device.

C. Modified SCR With Stripe Layout

In Fig. 3(a) and (b), the trigger voltage $(V_{\rm trigger})$ of the SSCR or WSCR under positive stress is the breakdown voltage of the N-well/P-well junction. The modified SCR can improve the turn-on efficiency and reduce the trigger voltage. As shown in Fig. 3(c), the trigger P+ diffusion is added across the N-well/P-well junction in the stripe p-modified SCR (SPMSCR) to reduce the junction breakdown voltage. When a positive or negative ESD stress is zapped from anode to cathode, the ESD currents primarily flow through two edges of the device.

Since the large trigger diffusion often increases the parasitic capacitance, the SPMSCR was implemented with separated trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of $\rm SPMSCR_1$ and $\rm SPMSCR_2$ are 123.2 and 242.48 μm^2, respectively, as listed in Table I.

D. Modified SCR With Waffle Layout

With the trigger P+ diffusion across the N-well/P-well junction, the proposed waffle p-modified SCR (WPMSCR) is shown in Fig. 3(d). The WPMSCR can discharge both positive and negative ESD current through the four edges of the device, thus the FOM of $V_{\rm MM}/C_{\rm ESD}$ can be increased. The WPMSCR was also implemented with separated trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of $\rm WPMSCR_1$, $\rm WPMSCR_2$, and $\rm WPMSCR_3$ are 70.24, 140.48, and 264.96 μm^2, respectively, as listed in Table I.

The trigger P+ diffusion can be replaced by the trigger N+ diffusion. As shown in Fig. 3(e), the trigger N+ diffusion is added across the N-well/P-well junction of the waffle n-modified SCR (WNMSCR) to characterize the ESD robustness and high-frequency performances.

E. Metal Routing Strategy

The top metal (metal 6) in a 0.18-μm CMOS process, which is far from the grounded P-substrate, is used for routing on the anode of each SCR device. This is critical to reduce the parasitic capacitance at the I/O pad in RF circuits. The bottom metal (metal 1) is used for routing on the cathode of each SCR device. With such a metal routing strategy, the parasitic capacitance between the anode and cathode of the SCR device can be further reduced [22].

All the aforementioned devices have been fabricated in a 0.18-μm fully silicided CMOS process. The size of each SCR device in layout is kept at 60.62×60.62 μm^2. The FOM of $V_{\rm MM}/C_{\rm ESD}$ of the SCR devices in different layout styles have been measured to investigate their effectiveness.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Transmission Line Pulsing (TLP) Measurement

The trigger voltage $(V_{\rm trigger})$, secondary breakdown current $(\rm It_2)$, and turn-on resistance $(R_{\rm on})$ in the holding region of the fabricated SCR devices under positive stresses were characterized by the TLP system. The $\rm It_2$ of the devices under negative stresses were also evaluated by the TLP system. The TLP-measured current–voltage (*I–V*) curves for SSCR and WSCR are

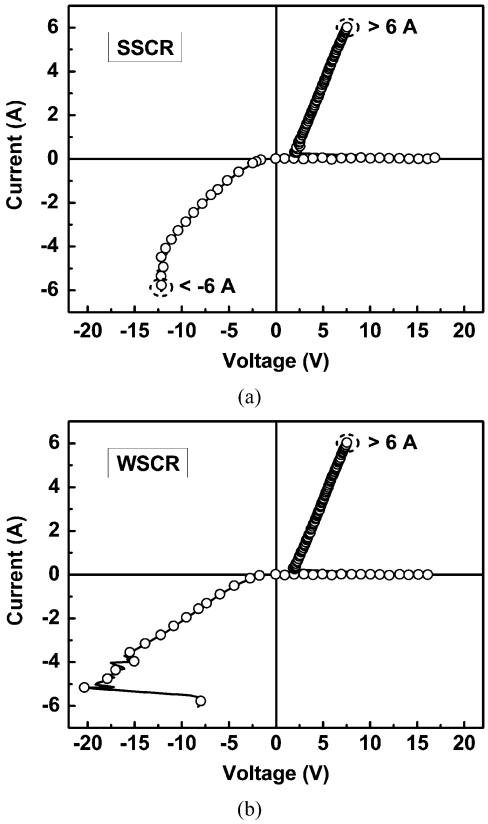

Fig. 5. TLP-measured current–voltage (*I–V*) characteristics of: (a) SSCR and (b) WSCR.

shown in Fig. 5(a) and (b), respectively. Excluding the difference in trigger voltages, the similar *I–V* curves were obtained in the other SCR devices. The trigger voltages among the SCR devices under different trigger diffusion areas are compared in Fig. 6. Both SSCR and WSCR under positive stresses are triggered at approximately 16–17 V. With the P+ or N+ trigger diffusion added into the modified SCR, the trigger voltages can be significantly reduced. The TLP-measured turn-on $R_{\rm on}$ under positive stresses of the stripe and the waffle SCRs in the high-current holding region are as low as $\sim$1 Ω. The $\rm It_2$ of all SCR devices under positive stresses exceed 6 A, which is the measurement limitation of a given TLP system. The secondary breakdown currents of all SCR devices under negative stresses are at least 4.1 A. Due to the reduction of the N+ diffusion area in the N-well in the proposed waffle layout structure, the secondary breakdown currents of devices in the waffle layout were lower than those with the conventional stripe layout. The measured results on the characteristics of the fabricated SCR devices are listed in Table I.

B. ESD Robustness

The human body model (HBM) and MM ESD robustness of the fabricated SCR devices were evaluated by the ESD simulator. The $\rm It_2$ is approximately linear to the HBM ESD level of the device-under-test (DUT). The relationship between the HBM ESD level $(V_{\rm HBM})$ and $\rm It_2$ is

$$V_{\rm HBM} \approx (1500 + R_{\rm on}) \times {\rm It}_2 \tag{2}$$

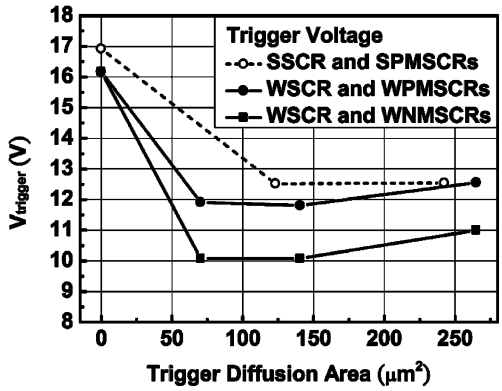

Fig. 6. Dependence of TLP-measured $V_{\rm trigger}$ on the trigger diffusion area of SCR devices with different layout structures.

where $R_{\rm on}$ is the turn-on resistance of the DUT. Since the $\rm It_2$ of each SCR device is larger than 6 A, the HBM ESD robustness of each SCR device is quite high. After measurement, the positive HBM ESD levels of all SCR devices were found to exceed 8 kV, which verifies the relationship between $V_{\rm HBM}$ and $\rm It_2$. The positive MM ESD levels are within the range of 1.4–1.8 kV. The negative HBM ESD levels of all SCR devices are 7 kV at least, and negative MM ESD levels are within the range of 0.5–1.0 kV, as listed in Table I.

C. Parasitic Capacitance

The SCR devices were implemented with ground–signal–ground (G–S–G) pads to facilitate on-wafer two-port S-parameter measurement. The two-port S-parameters were measured by using the vector network analyzer HP 8510C. During the S-parameter measurement, the anode of the SCR device was connected to port 1 and biased at 0.9 V, which is $V_{DD}/2$ in the given 0.18-μm CMOS process, and the cathode was connected to port 2 and biased at 0 V.

In order to extract the characteristics of the intrinsic device in high frequency, the parasitic effects of the bond pad must be removed. The test patterns, one including the DUT and the other excluding the DUT, as shown in Fig. 7(a) and (b), were fabricated in the same experimental test chip. The Y_{11}-parameter can be obtained from the measured two-port S-parameters by using

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0((1 + S_{11})(1 + S_{22}) - S_{12}S_{21})} \tag{3}$$

where Z_0 is the termination resistance and is equal to 50 Ω [23]. The measured Y-parameter of the including-DUT pattern is labeled as $Y_{11\_\rm meas}$, and the measured Y-parameter of the excluding-DUT pattern is labeled as $Y_{11\_\rm par}$. The intrinsic device characteristics $(Y_{11\_\rm DUT})$ can be obtained by subtracting $Y_{11\_\rm par}$ from $Y_{11\_\rm meas}$. The parasitic capacitance $(C_{\rm ESD})$ of each SCR was extracted from the Y-parameter of the intrinsic device by using

$$C_{\rm ESD} = \frac{{\rm Im}(Y_{11\_\rm DUT})}{2\pi f} \tag{4}$$

where f is the operating frequency. Fig. 8 shows the extracted capacitances from 2.4 to 5 GHz of the SCR devices. For each

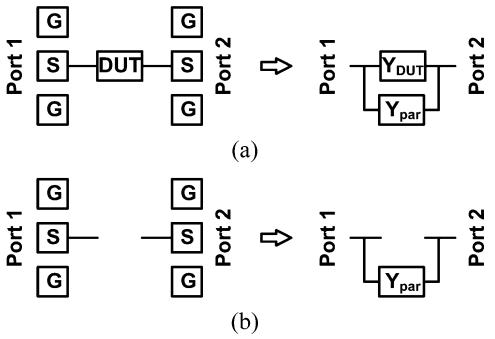

Fig. 7. Layout top view with G–S–G pads and the equivalent model of: (a) including-DUT pattern and (b) excluding-DUT pattern.

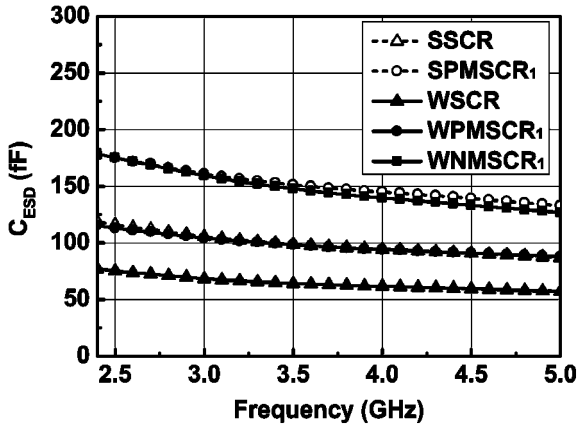

Fig. 8. Extracted capacitances of the SCR devices from 2.4 to 5 GHz.

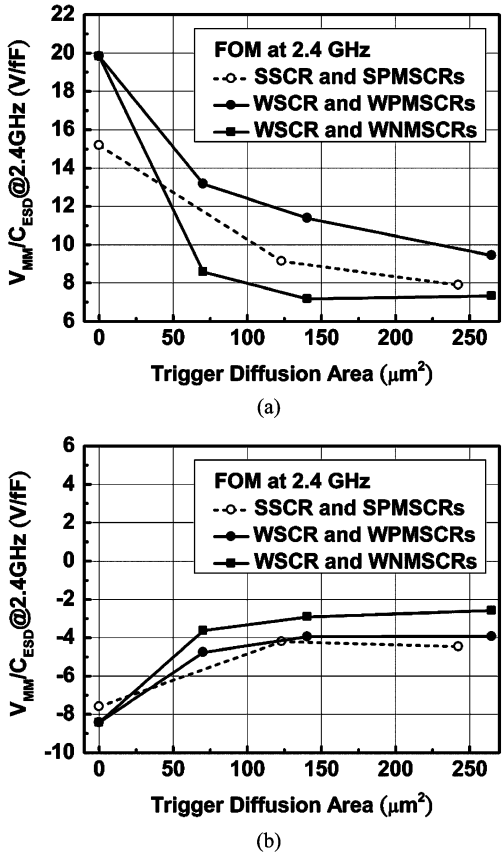

Fig. 9. Dependence of FOM $(V_{\mathrm{MM}}/C_{\mathrm{ESD}})$ at 2.4 GHz under: (a) positive and (b) negative ESD stresses on the trigger diffusion area of SCR devices under different layout structures.

SCR device, the parasitic capacitance is decreasing as the frequency is increasing. Since the parasitic capacitance was in series with a resistor, which is caused by the parasitic N-well resistance and P-well resistance in each SCR device, the parasitic capacitance in high frequency is decreasing with the increasing frequency. The parasitic capacitances of the fabricated SCRs at 2.4 GHz (for wireless local area network (LAN) applications) were listed in Table I.

D. Comparison on FOM

The FOM $(V_{\mathrm{MM}}/C_{\mathrm{ESD}})$ of the SSCR, WSCR, SPMSCR, WPMSCR, and WNMSCR under positive and negative ESD stresses are compared in Fig. 9(a) and (b), respectively. Even though the positive V_{MM} of the WSCR is worse than the SSCR due to the reduction of the N-well area in the proposed waffle layout structure, the parasitic capacitance can be greatly reduced. Without the trigger diffusion, the FOM of the proposed WSCR under positive stress has an increase of approximately 30%, as compared with the conventional SSCR. With the trigger diffusion, the FOM of the proposed WPMSCR under positive stress has an increase of approximately 25%, as compared with the conventional SPMSCR. Although the FOM is decreased with the increase of the trigger diffusion area, the trigger voltage can be significantly reduced to effectively protect the RF circuits. Comparison on the FOM among the SCR devices, the best FOM under positive stress was found in the WPMSCR. The negative MM ESD levels of the SCR devices with waffle layout structures were lower than the SCR devices with stripe layout structures due to the reduction of the N+ diffusion area in the N-well in the proposed waffle layout structure. The FOM of stripe and waffle structure devices under negative stresses are almost the same.

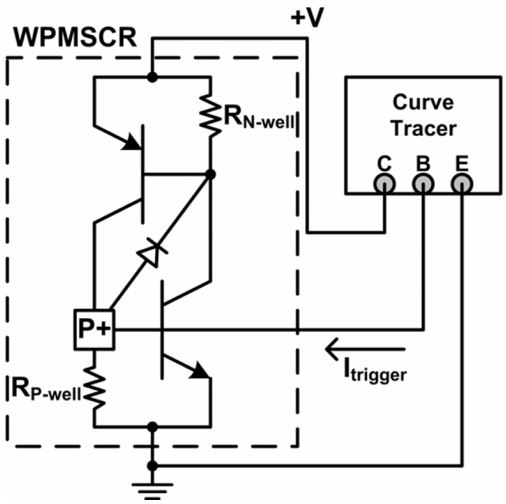

Fig. 10. Measurement setup to find the dc *I–V* curves of each WPMSCR devices under different trigger currents.

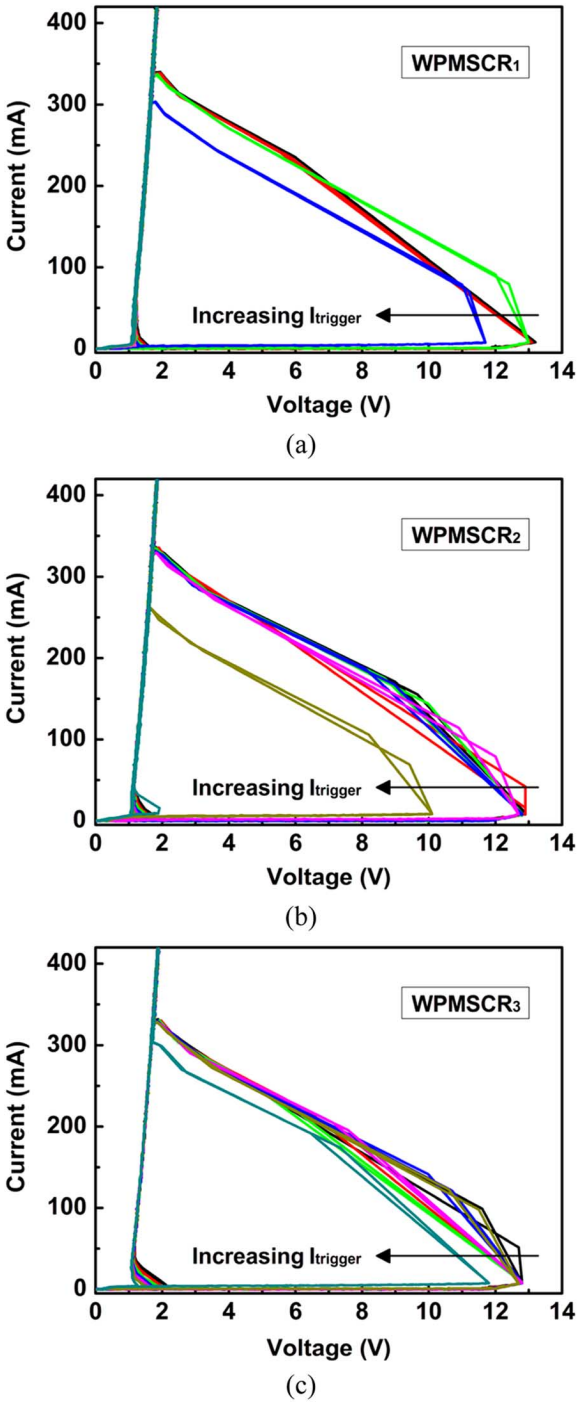

Fig. 11. DC *I–V* curves of: (a) WPMSCR_1, (b) WPMSCR_2, and (c) WPMSCR_3, under different trigger currents.

E. Trigger Mechanism

Among the SCR devices, the WPMSCR was demonstrated to have the improved FOM and the best RF performance. To further reduce the trigger voltage of the WPMSCR, the trigger current (I_{trigger}) can be injected into the P+ trigger diffusion to enhance the turn-on efficiency. To investigate the suitable trigger current for a WPMSCR, the curve tracer (Tektronix 370B) was used to measure the dc *I–V* curves of the WPMSCR, as shown in Fig. 10. The dc *I–V* curves of each WPMSCR under different trigger currents are shown in Fig. 11(a)–(c).

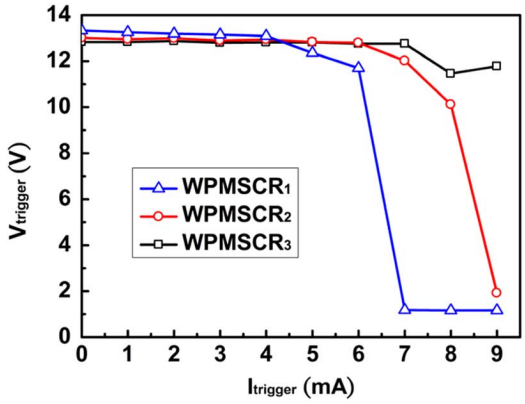

Fig. 12. Dependences of the trigger voltages of WPMSCR devices on the trigger current.

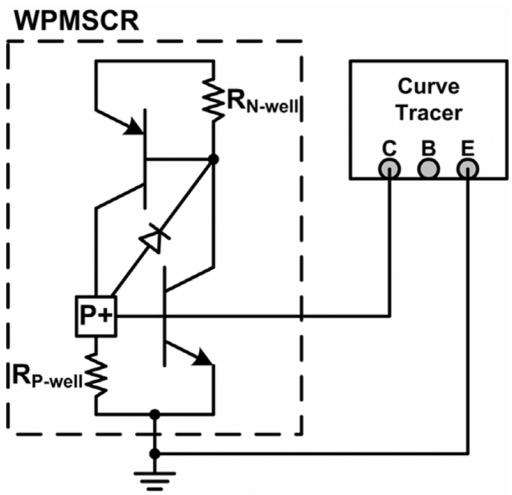

Fig. 13. Measurement setup to find the dc *I–V* curves of the base–emitter junction diode of WPMSCRs.

The static trigger voltages of WPMSCR devices without trigger currents are larger than the dynamic (TLP) trigger voltages listed in Table I, which were measured by TLP and involved in the dV/dt transient current of the ESD-like pulse. The dependences of the static trigger voltage of WPMSCR devices on the trigger current are compared in Fig. 12.

The measurement setup and experimental results of dc *I–V* curves of the base–emitter junction diode of the WPMSCR are shown in Figs. 13 and 14, respectively. The trigger voltage of the WPMSCR can be significantly reduced as long as the base–emitter junction diode of the NPN transistor is turned on. If the trigger current is continually increased, the trigger voltage of each WPMSCR devices will be reduced to a value close to their holding voltages. With large enough trigger current, the SCR can be readily turned on to clamp the voltage across its anode and cathode. Before the SCR is turned on, the P-well resistance of each WPMSCR can be extracted as the reciprocal of the slope of each curve in Fig. 14.

F. Turn-On Speed

In order to investigate the turn-on speed of the WPMSCR devices with different trigger diffusion areas, the experimental

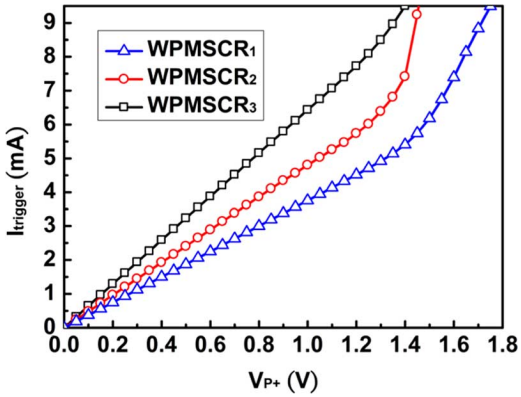

Fig. 14. DC *I–V* curves of the base–emitter junction diode of WPMSCRs.

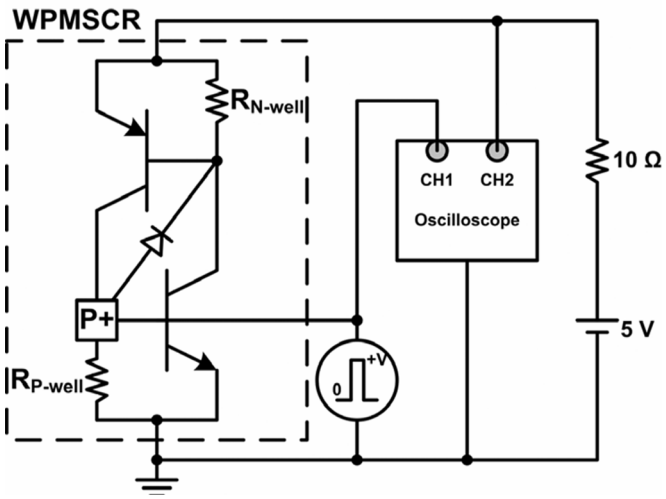

Fig. 15. Measurement setup to find the turn-on time of WPMSCR devices under different voltage pulses.

setup to measure the required turn-on times of the WPMSCR devices is illustrated in Fig. 15. A 5-V voltage bias was connected to the anode of a WPMSCR device through a 10-Ω resistance, which was used to limit the sudden large transient current from power supply when the WPMSCR is turned on. The cathode of the SCR was grounded. The turn-on time of the WPMSCR is defined as the time for the WPMSCR to enter its low-voltage holding region. The measured voltage waveforms on the trigger nodes and anodes, and the turn-on times for three WPMSCR devices with different trigger diffusion areas are shown in Fig. 16(a)–(c). The pulse with amplitude of 5 V, rise time of 10 ns, and pulsewidth of 100 ns was applied to the trigger node. The turn-on times of WPMSCR devices are 10.9, 11.4, and 15.3 ns, respectively. The turn-on time is reduced when the WPMSCR is drawn with a smaller trigger diffusion area. The measured turn-on times and the measured $R_{\text{P-well}}$ of the three WPMSCR devices under different trigger diffusion areas are compared in Fig. 17.

G. Discussion

According to the experimental results of SCR devices with different layout structures, the SCR devices with waffle layout

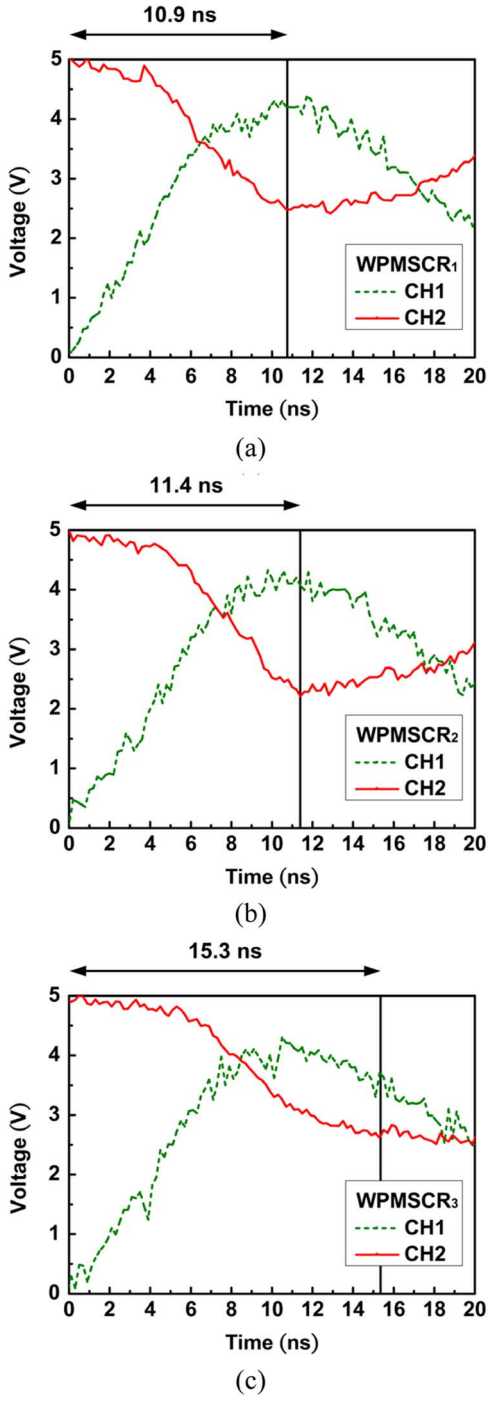

Fig. 16. Measured voltage waveforms on the anode of: (a) WPMSCR_1, (b) WPMSCR_2, and (c) WPMSCR_3, while the WPMSCR is triggering by the 5-V pulse into the trigger node.

structures have the better ESD robustness under the same parasitic capacitance. In other words, the parasitic capacitance of each SCR device in the waffle layout has been reduced under the same ESD robustness. The proposed WSCR and WPMSCRs are more suitable for RF ESD protection because of the reduced parasitic capacitance. For faster turn-on speed, the trigger voltage of the WPMSCRs can be further reduced by an additional trigger circuit to effectively protect the RF circuits against ESD damages. A low parasitic-capacitance ESD detection and

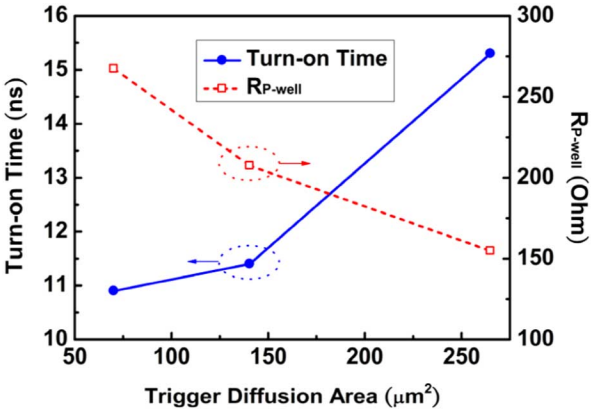

Fig. 17. Dependence of the turn-on time and the $R_{\text{P-well}}$ of WPMSCRs on the different trigger diffusion area.

trigger circuit should be developed to enhance the turn-on speed of the proposed waffle SCR for ESD protection in RF ICs.

IV. Conclusion

The proposed SCR devices with a waffle layout structure had been successfully verified in a 0.18-μm CMOS process. As compared with the conventional SSCR devices, the proposed WSCR and WPMSCR have been demonstrated to improve ESD robustness under the same parasitic capacitance. The FOM $(V_{\text{MM}}/C_{\text{ESD}})$ of the proposed WPMSCR under positive ESD stresses has an increase of approximately 25%, as compared to the conventional SPMSCR. Although the FOM is decreased with the increased trigger diffusion area, the trigger voltage can be reduced to effectively protect the RF circuits against ESD damages. The FOM of SSCR and WSCR under negative ESD stresses are almost the same in this study. The trigger voltage of WPMSCR can be further reduced by injecting trigger current to the P+ trigger diffusion. The dependences of the trigger voltage of the WPMSCR on the trigger current had also been investigated. Besides, the dependence of turn-on time on the trigger diffusion area had been investigated. With the investigation on trigger current and turn-on time, the ESD detection circuit can be properly designed to quickly trigger on the WPMSCR under ESD stress conditions.

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