High Quality Interpoly Dielectrics Deposited on the Nitrided-Polysilicon for Nonvolatile Memory Devices

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***Abstract*—High quality interpoly dielectrics have been fabricated by using NH_3 and N_2O nitridation on polysilicon and deposition of tetra-ethyl-ortho-silicate (TEOS) oxide with N_2O annealing. The surface roughness of polysilicon is improved and the value of weak bonds is reduced due to nitrogen incorporation at the interface, which improves the integrity of interpoly dielectrics. The improvements include a higher barrier height, breakdown strength, and charge-to-breakdown, and a lower leakage current and charge trapping rate than counterparts. It is found that this method can simutaneously improve both charge-to-breakdown (up to 20 C/cm^2) and electric breakdown field (up to 17 MV/cm).**

***Index Terms*—Barrier height, charge-to-breakdown, dielectric, electric breakdown field, interpoly, nonvolatile memories, polysilicon.**

I. Introduction

THERMALLY grown or deposited oxides on n^+ polysilicon have been used as the inter-dielectric for nonvolatile memories such as erasable-programmable read-only memory (EPROM), electrical-erasable programmable read-only memory (EEPROM), and flash memories. In order to obtain good data retention and endurance characteristics, inter-dielectrics with a low conductivity (low leakage current) and a high electric breakdown field $(E_{\rm bd})$ have been topics of research for a long time [1]–[3]. Because thermal oxidation of polysilicon leads to a rough polysilicon surface, thermally grown polyoxides exhibit a lower dielectric strength and a higher leakage current than those of oxide grown on single crystal silicon [4]–[12]. Recently, in contrast to thermal oxides, deposited dielectric layers have been investigated as a very promising alternative, since these dielectric layers are deposited on the polysilicon layer without silicon consumption. Consequently, the surface of polysilicon for a deposited polyoxide structure is found to be smoother than oxidizing counterpart. Low-temperature oxides (LTO) with an annealing in a rapid thermal processing (RTP) system or oxides deposited in a low-pressure chemical-vapor-deposition (LPCVD) system have been used, but resultant electrical properties of LTO are not good enough for EEPROM applications even with additional postdeposition treatments [13]–[15]. In contrast to LTO, dielectrics deposited at a high temperature, like tetra-ethyl-ortho-silicate (TEOS), exhibit an improved performance [16]–[18]. In addition, high-temperature oxides (HTO) with the postdeposition treatment in a rapid thermal annealing (RTA) system are proposed to improve electrical properties, which can achieve effects of densification, reoxidation, and nitridation [19]–[21]. Furthermore, Klootwijk *et al.* [19] found that the oxide deposited with an additional N_2O-annealing is an attractive alternative for conventional polyoxide, which results in an improved endurance of EEPROM devices by a factor of ten.

The underlying polysilicon layer also plays a dominant role in the dielectric strength. Lei *et al.* [22], [23] found that the strength of deposited dielectric depends on the roughness of polysilicon. Using chemical-mechanical polishing (CMP) on polysilicon, the dielectric integrity is significantly improved due to the smooth interface of the polysilicon, but charge-to-breakdown $(Q_{\rm bd})$ values are not improved simutaneously [23]. The method using both CMP and CVD oxide yields a high breakdown field $(E_{\rm bd})$ and low electron-trapping rate. Recent reports show that the reliability of MOS and polyoxide capacitors can be improved by introducing proper amounts of nitrogen or fluorine [1], [24], [25]. It is also reported that the N_2O-grown and N_2O-annealing polyoxides have better electrical performances than O_2-grown polyoxides, which contributes to the nitrogen incorporation at the polyoxide/polysilicon interface [21], [26]–[29]. However, this treatment moderately improves the dielectric strength only.

In this paper, polyoxides are fabricated by utilizing a NH_3-nitridation and RTA N_2O-annealing on polysilicon to incorporate nitrogen at the surface of polysilicon. TEOS-oxides are then deposited on this nitrided polysilicon and followed with or without a densification in an N_2O ambient. It is found that this method can simutaneously improve both $Q_{\rm bd}$ and $E_{\rm bd}$.

II. Experiments

The n^+-polysilicon/polyoxide/n^+-polysilicon capacitors were fabricated on the p-type (100) silicon wafers. First, silicon wafers were thermally oxidized at 1000°C to form a 100-nm-thick isolation oxide. Then a 300-nm polysilicon layer (poly-1) was deposited in a LPCVD system using SiH_4 gas at 620 °C and subsequently doped with $POCl_3$ at 900 °C for 30 min, resulting in a sheet resistance of 30∼40 Ω/□. After the p-glass was stripped off, the samples were then annealed

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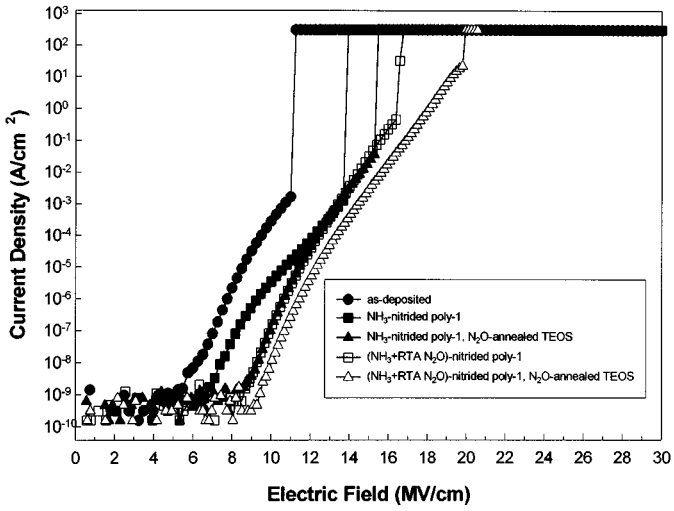
in NH_3 ambient at 800 °C for 2 h followed with or without a N_2O-RTA annealing at 800 °C for 20 s. After that, a TEOS oxide with thickness to 100 Å was deposited in a LPCVD system at 650 °C, followed by a RTA at 900 °C for 30 s in the N_2 or N_2O ambient for densification of oxides to a final 90 Å. Then a second polysilicon layer (poly-2) of 300-nm was deposited by a LPCVD system at 620 °C and doped to a sheet resistance of 30∼40 $\Omega/\square$ with the same $POCl_3$ process as poly-1. After definition of the poly-2, all samples were covered with a 100-nm oxide as a passivation layer. Contact holes were opened and aluminum was deposited and patterned to form the final capacitor structures. Finally, all devices were sintered at 400 °C for 30-min in a N_2 ambient.

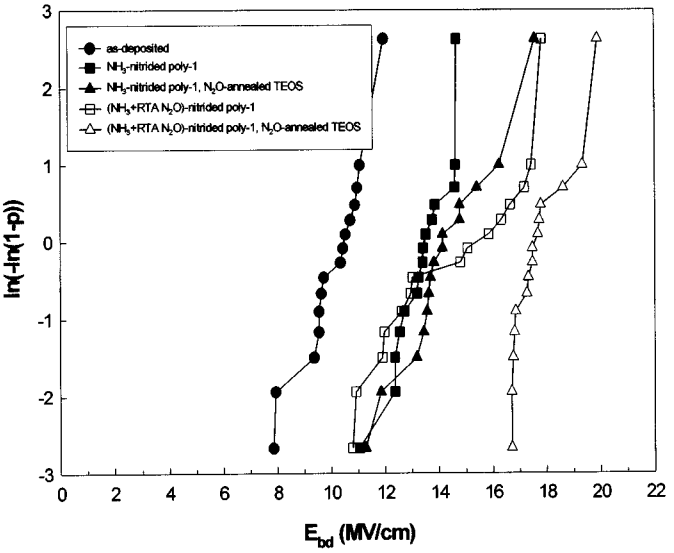
Atomic force microscope (AFM) was used to characterize the surface morphology of polysilicon films with or without nitridation. Polyoxide thickness was determined by the high-frequency capacitance-voltage measurements with Keithley 590 and 595. The electrical properties, effective electron barrier height, electron trapping characteristics, and charge-to-breakdown were measured by a HP-4145B semiconductor parameter analyzer.

III. Results and Discussion

Impacts of nitridation on poly-1 and densification of TEOS in N_2O are evaluated by the measurement of current–voltage (I–V) and breakdown field. In this measurement, the poly-2 is positively biased. (i.e., electrons are injected from the dielectric/poly-1 interface). Fig. 1(a) shows curves of current density versus electrical field, and Fig. 1(b) depicts the Weibull distributions of breakdown field for 75 capacitors corresponding to Fig. 1(a). The electrical field ($E_{\rm ox}$) is defined as $V_g/T_{\rm ox}$, where V_g is the applied gate voltage, and $T_{\rm ox}$ is the effective dielectric thickness as determined by the (capacitance–voltage (C-V) measurement. It is found that samples with nitridation of poly-1 have higher breakdown fields ($E_{\rm bd}$) than control samples (as deposited). They exhibit a lower leakage current and start conducting at higher voltages than control samples. It is also noted in Fig. 1 that samples with the RTA N_2O-treatment on poly-1 exhibit an improved $E_{\rm bd}$ and reduced leakage current. Since the NH_3-nitridation will introduce hydrogen into the polysilicon, leading to unstable Si-H bonds. The NH_3-nitridation of poly-1 only moderately improves the dielectric strength. With an additional RTA N_2O-treatment, the unstable Si-H bonds will be annealed out, resulting in the better electrical characteristics with respect to the NH_3-treated samples, as shown in Fig. 1. Secondary ion mass spectroscopy (SIMS) measurements of two samples fabricated with and without nitridation of poly-1 are shown in Fig. 2. The profiles of Si+N within the dielectric film are significantly increased by the nitridation treatment. In comparison with the control sample, a relatively high peak of Si+N profile within the dielectric film was observed for the (NH_3+RTA N_2O)-nitrided sample. It has been well recognized that the quality improvement of dielectrics by nitridation is thought to be the replacement of strained Si-O bonds or dangling bonds by Si-N bonds, leading to a relaxation of the interface stress [19], [25], [32]. In addition, annealing of dielectric in N_2O ambient has been used to achieve an oxidation



(a)



(b)

Fig. 1. (a) Typical J-E characteristics of interpoly dielectric layers with or without NH_3 and RTA N_2O nitridation of poly-1 and N_2O densification of TEOS under positive applied voltages, i.e., electrons are being injected from the bottom electrode. (b) Typical Weibull distribution of the electrical breakdown field for the as-deposited, deposited on the nitrided-poly-1, and postdeposition annealing interdielectrics.

of the bulk nonstoichiometric SiO_2, a nitridation at the Si-SiO_2 interface and a densification of the dielectric [19]. Hence, a very high $E_{\rm bd}$ up to 17 MV/cm (average of 50%) was achieved for the sample by using the (NH_3+RTA N_2O)-nitridation of poly-1 and the N_2O-densification of TEOS.

Plotting the J-E characteristics in the form of a Fowler-Nordheim (F-N) plot (J/E^2 versus $1/E$) [30], [31], straight lines were obtained for all samples as shown in Fig. 3, indicating that F–N tunneling is the major conducting mechanism. The transport of F-N tunneling has the form $J = C_1E^2\exp(-\phi_B/E)$, where E is the field, and C_1 and ϕ_B are constants in terms of effective mass and barrier height. Indeed, the barrier height increased upon nitridation of poly-1, and N_2O densification of TEOS. In all fabrication conditions, samples with (NH_3+RTA N_2O) nitridation of poly-1 and N_2O-densification of TEOS has

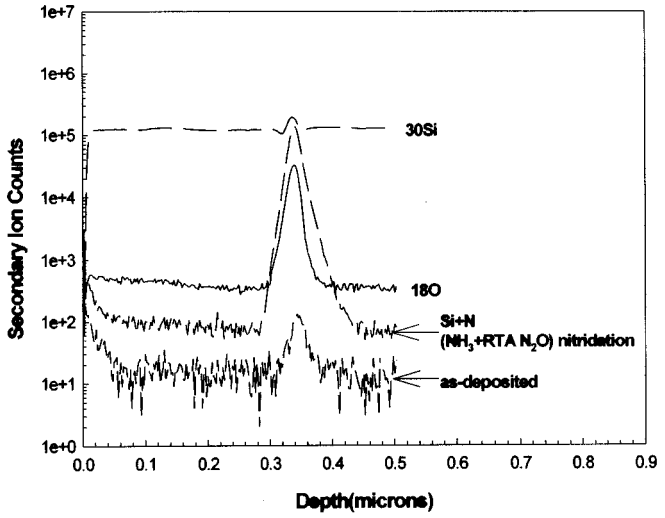


Fig. 2. SIMS profile of two samples fabricated with (NH_3+RTA N_2O) and without nitridation of poly-1.

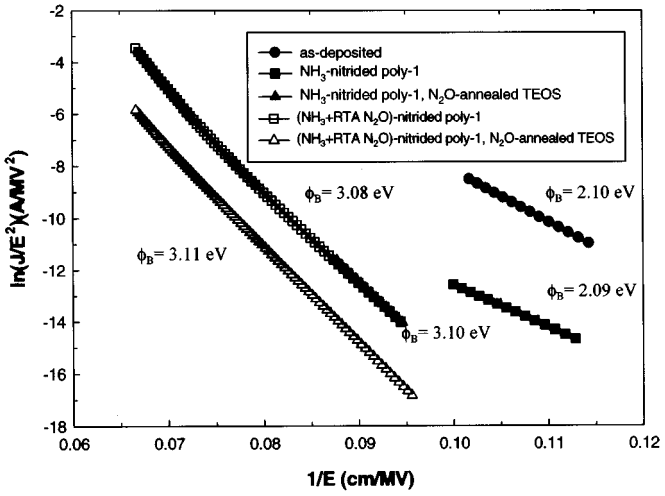
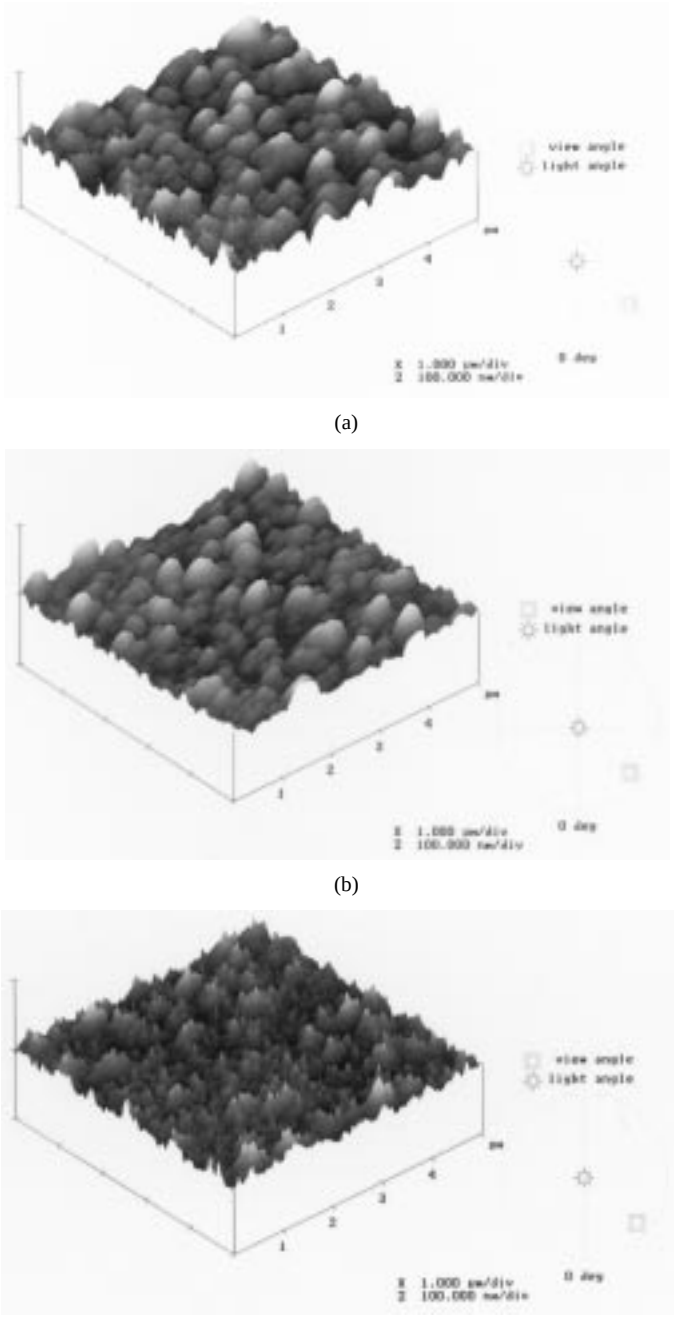


Fig. 3. J-E characteristics in the form of a Fowler-Nordheim plot (J/E^2 versus $1/E$) for all dielectric layers. According to the F-N model, from the corresponding slopes of these lines the barrier heights foe the electron were obtained.

the highest effective electron barrier height. Fig. 4 displays the surface images of the poly-1 film with or without nitridation of poly-1 and N_2O-densification of TEOS by the atomic force microscope (AFM) measurement. The surface morphology of the poly-1 without/with the nitridation, and RTA N_2O-densification of TEOS are shown in Fig. 4(a)–(c). Root mean square (RMS) roughness for these three samples are 97.8, 85.6, and 71.8 Å, respectively. This implies NH_3 and RTA N_2O-nitridation results in a smooth surface. The dielectrics deposited on the (NH_3+RTA N_2O)-nitrided poly-1 and N_2O- densification of TEOS exhibit the smoothest interface and hence result in the higher breakdown field.

Fig. 5 shows shift of gate-voltage under the constant current stressing at 100 μA/cm^2 for all capacitors. It reveals that the additional RTA N_2O-nitridation of poly-1 has a smaller voltage shift than the NH_3 nitrided-only sample. This implies that samples with the additional RTA N_2O-nitridation of poly-1



(a)

(b)

(c)

Fig. 4. Surface images of the polysilicon film by AFM measurement. (a) As-deposited, (b) NH_3-nitrided poly-1, and (c) NH_3 and RTA N_2O-nitrided poly-1 with additional N_2O densification of TEOS.

yield a better immunity to the trapping of charges. Relatively, the rougher dielectric/poly-1 interface leads to a smaller conduction area and a higher local current density, subsequently causing a higher trapping rate of charge [23]. For the sample of (NH_3+RTA N_2O)-nitrided poly-1 and N_2O-densification of TEOS, a small initial hole trapping is found, after that, no significant trapping is observed. This is due to the highest nitrogen incorporation among these samples.

Regarding the reliability of polyoxide in nonvolatile memories, charge-to-breakdown ($Q_{\rm bd}$) is also a critical parameter of interest. Dielectrics with large value of $Q_{\rm bd}$ are needed to guaranty long read/write cycles. In the conventional polyoxide fab-

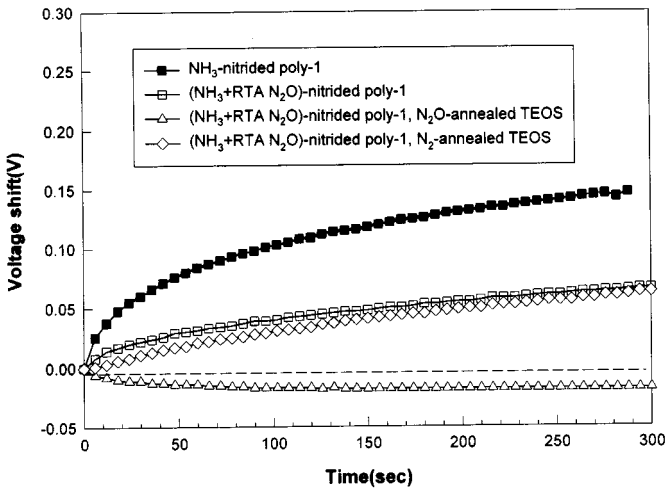


Fig. 5. Charge trapping characteristics, i.e., curves of gate voltage shifts versus stress time under positive top bias with a constant current stressing at 100 μA/cm^2.

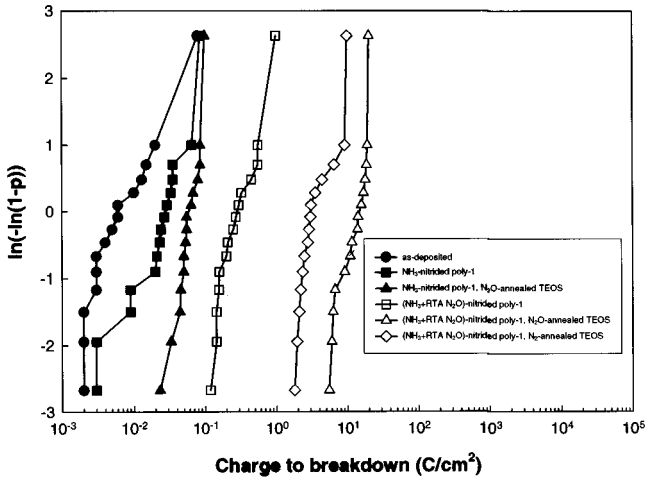


Fig. 6. Typical Weibull plots of the charge-to-breakdown for the as-deposited, nitrided-poly-1, and postdeposition annealed interdielectric layers under positive stress.

rication, $Q_{\rm bd}$ values are very small (in the range of 0.01 °C/cm^2 to 0.1 °C/cm^2) due to surface roughness and nonuniform poly-oxide thickness. In Fig. 6, the Weibull distributions of charge-to-breakdown of 90-capacitor (100 × 100 μm^2) are shown for positive bias at top-gate. In the measurement, a constant current of 1 mA/cm^2 was used to stress the control and NH_3-nitrided samples (solid symbols) and a constant current of 100 mA/cm^2 was stressed for the RTA N_2O-nitrided samples (empty symbols).It is seen that the NH_3-nitridation of poly-1 improves dielectric layer slightly, while the additional RTA N_2O-nitridation of poly-1 increases $Q_{\rm bd}$ significantly. It can be seen in Fig. 6 that the improvement of $Q_{\rm bd}$ is about from 0.01 C/cm^2 to 0.1 C/cm^2 by using NH_3-nitridation only. This may be due to the incorporation of hydrogen atoms at the dielectric/poly-1 interface. But if the poly-1 was nitrided with the additional RTA N_2O, $Q_{\rm bd}$ increases significantly. In addition to the improvement on roughness of poly-1 as discussed in Fig. 4, the improved integrity is also due to the incorporation of nitrogen atoms, which reduce

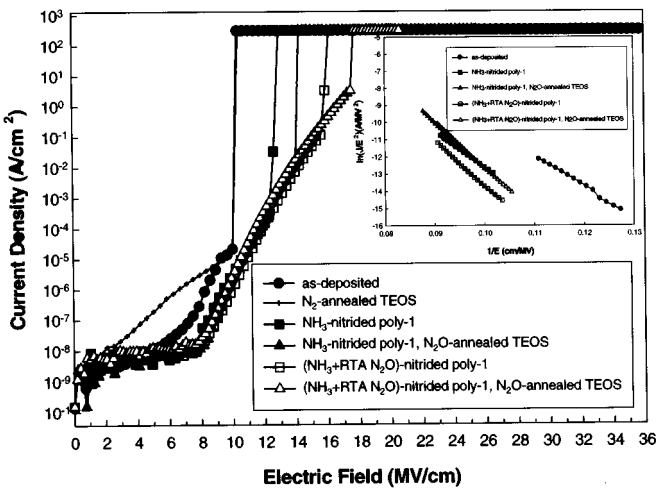


Fig. 7. Typical J-E characteristics of interpoly dielectric layers with or without NH_3 and RTA N_2O nitridation of poly-1 and N_2O densification of TEOS under negative applied voltages, i.e., electrons are being injected from the top electrode. The inset is a Fowler-Nordheim plot (J/E^2 versus $1/E$) under negative top bias.

the weak Si-O (Si-H) bonds and relax the interface stress [19], [25]. Again, it is seen that a densification of TEOS by N_2O (or N_2) annealing can further improve the dielectric integrity. It is found that $Q_{\rm bd}$ up to 20 C/cm^2 can be obtained as the poly-1 was nitrided by the NH_3 and RTA N_2O-annealing and the TEOS annealed with N_2O postdeposition.

So far, only the electron injection from the bottom electrode has been considered. For the negative top electrode bias, i.e., electron injection from the top electrode, it had been shown that dielectrics with an additional N_2O postannealing conducted a higher current than the as-deposited oxides [19], which is in contrast to positive top bias. This polarity preference was also observed for interdielectric layers directly grown from N_2O [25]. Fig. 7 shows the J–E characteristics for the samples under negative bias at top-gate. Although the postdeposition annealing results in the polarity asymmetry, it is found that samples with nitridation of poly-1 still exhibit a better performance than the as-deposited samples. As compared to Fig. 1, the leakage currents of negative bias are one order of magnitude higher than those obtained from the positive bias. This is mainly ascribed to the nitrogen incorporated at the interdielectric/poly-1 interface. The inset in Fig. 7 depicts the F-N plots for electron injection from the top gate. Although the barrier height for the electron tunneling from poly-2 to the SiO_2 is not strongly related to the nitridation of poly-1 and the densification of TEOS, it is found that the barrier height is slightly improved with nitridation and N_2O densification of TEOS as shown in Fig. 7. The Weibull distributions of $Q_{\rm bd}$ under the negative bias are shown in Fig. 8. It is noted that the improvements of $Q_{\rm bd}$ using nitridation of poly-1 and densification of TEOS are similar to the positive top gate bias. The inset of Fig. 8 shows the charge trapping characteristics under constant current stressing at 100 (μA/cm^2 for the negative bias at top-gate. The shift of gate-voltage increases with time. The additional RTA N_2O-nitridation of poly-1 has a smaller voltage shift than the NH_3-nitrided capacitor. This finding also implies that the additional RTA N_2O-nitridation of

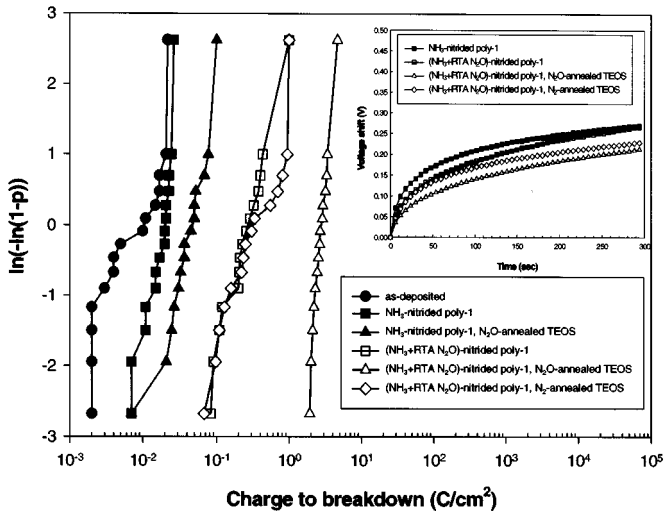


Fig. 8. Typical Weibull plots of the charge-to-breakdown for the as-deposited, nitrided-poly-1, and postdeposition annealed interdielectric layers under positive stress. The inset is the charge trapping characteristics under negative top bias.

poly-1 yields a better immunity to electron trapping, no matter what directions of electrons are injected. Furthermore, as TEOS was annealed in N_2O ambient, the sample exhibits a better performance of charge trapping characteristic, which results in a higher charge-to-breakdown as seen in Fig. 8. However, as compared to Fig. 5, the electron trapping rates of capacitors under the negative bias at top gate are higher than those obtained from the positive bias counterpart. This is due to the different position of trapped charges in the N_2O-annealed oxide under different gate bias, which is similar to the physical model proposed in [4].

IV. Conclusion

In this study, an NH_3 with RTA N_2O process to incorporate nitrogen at dielectric/polysilicon interface has demonstrated to improve integrity of polyoxides. Polyoxides deposited on this nitrided polysilicon with the additional N_2O-densification exhibit a lower leakage current, higher electric breakdown field, higher electron barrier height, lower electron trapping rate, and much higher charge-to-breakdown than the as-deposited polyoxides. SIMS results show the incorporation of nitrogen at the polyoxide/poly-1 interface, which improves electrical properties in return. Polyoxides formed by this method can achieve a high breakdown field up to 17 MV/cm and charge-to-breakdown more than 20 °C/cm^2. This process appears to be a very attractive alternative for conventional polyoxides.

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