A 2.4-Gsample/s DVFS FFT Processor for MIMO OFDM Communication Systems

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***Abstract*—This paper presents a new dynamic voltage and frequency scaling (DVFS) FFT processor for MIMO OFDM applications. By the proposed multimode multipath-delay-feedback (MMDF) architecture, our FFT processor can process 1–8-stream 256-point FFTs or a high-speed 256-point FFT in two processing domains at minimum clock frequency for DVFS operations. A parallelized radix-2^4 FFT algorithm is also employed to save the power consumption and hardware cost of complex multipliers. Furthermore, a novel open-loop voltage detection and scaling (OLVDS) mechanism is proposed for fast and robust voltage management. With these schemes, the proposed FFT processor can operate at adequate voltage/frequency under different configurations to support the power-aware feature. A test chip of the proposed FFT processor has been fabricated using UMC 90 nm single-poly nine-metal CMOS process with a core area of 1.88×1.88 mm^2. The SQNR performance of this FFT chip is over 35.8 dB for QPSK/16-QAM modulation. Power dissipation of 2.4 Gsample/s 256-point FFT computations is about 119.7 mW at 0.85 V. Depending on the operation mode, power can be saved by 18%–43% with voltage scaling in TT corner.**

***Index Terms*—Dynamic voltage and frequency scaling (DVFS), fast Fourier transform (FFT), multiple-input multiple-output (MIMO), orthogonal frequency division multiplexing (OFDM).**

I. Introduction

THE rapid development of broadband wireless applications is driving new solutions for high-throughput, bandwidth-efficient, and reliable communications in wireless fading environments. Among the possible candidates, multiple-input multiple-output (MIMO) orthogonal frequency division multiplexing (OFDM) technology is considered the main stream for the next-generation broadband wireless systems due to its inherent benefits of multipath immunity and spatial diversity. Although MIMO OFDM systems can achieve better reliability and higher capacity, the power consumption also increases because of the extended complexity for the multi-stream processing. Therefore, low power becomes a major target in designing MIMO OFDM devices, especially for portable applications. In the MIMO OFDM receiver, the fast Fourier transform (FFT) processor is a key component with high computational complexity. The power consumption of the FFT processor grows proportionally to the stream number which occupies a large percentage of system power budget. Thus, it is demanded to design a power-efficient FFT processor for MIMO OFDM communication systems.

There have been several studies on low-power FFT processors for MIMO OFDM systems [1], [2] which focus on reducing the peak power at maximum throughput rate. From the system point of view; however, it is more desired to optimize the power consumption for all operation modes since full MIMO streams are not always needed depending on the channel condition and data rate. The dynamic voltage and frequency scaling (DVFS) [3]–[5] is an effective technique to achieve low power under different operation conditions. Both voltage and frequency can be scaled to optimal values in real time according to the processing needs. Therefore, we propose a novel DVFS FFT processor to satisfy the high-throughput and low-power requirements for MIMO OFDM systems. By a new multimode multipath-delay-feedback (MMDF) architecture and a novel open-loop voltage detection and scaling (OLVDS) scheme, the proposed FFT processor can perform 1–8-stream FFT computations in optimized voltage and frequency. Furthermore, compared to the previous DVS designs [5]–[7], the proposed method can achieve not only accurate and robust voltage scaling under process, voltage, and temperature (PVT) variations but also a faster scaling speed for better power-saving efficiency.

This paper is organized as follows. Section II identifies the system specification and design issues of the proposed DVFS FFT processor. Section III describes the radix-2^4 algorithm for the 256-point FFT computation. Section IV focuses on describing the proposed MMDF architecture of the FFT processing engine supporting both DVFS and multiple streams. The voltage detection and scaling scheme is shown in Section V. In Sections VI and VII, the implementation flow and the measurement results of the fabricated FFT chip are presented, respectively. Finally, the conclusion is given in Section VIII.

II. System Specification and Design Consideration

To demonstrate the idea of the proposed DVFS FFT processor, a high-throughput OFDM system supporting up to 300-MHz 8×8 MIMO or 2.4-GHz wideband transmissions with QPSK/16-QAM modulation is considered as our design target. The block diagram of the multimode receiver for this OFDM system is shown in Fig. 1. It consists of eight radio frequency (RF) modules, eight analog-to-digital converters (ADCs), eight filters, a 256-point MIMO FFT processor, a space-time code (STC) decoder, a QPSK/16-QAM demodulator, and a forward error correction (FEC) decoder. Based on the two scenarios in Fig. 1, the receiver demodulates 1–8-stream MIMO OFDM signals from multiple antennas or

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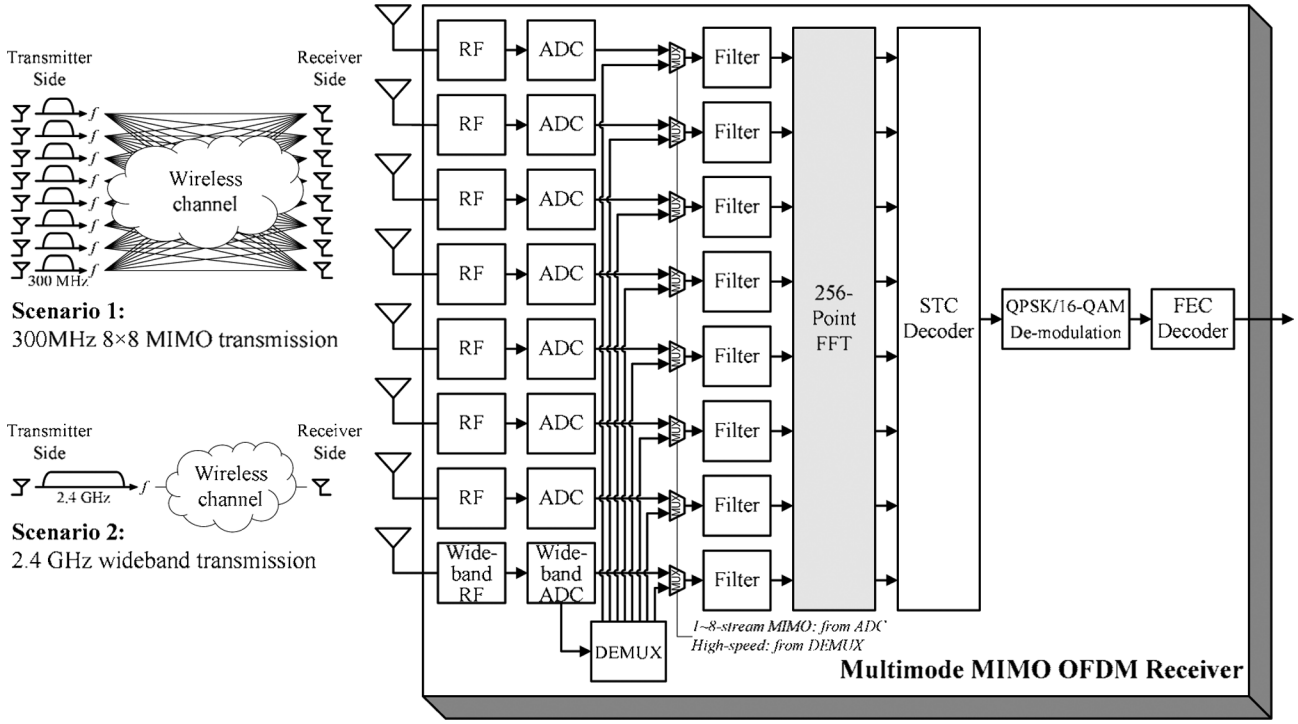


Fig. 1. Block diagram of the multimode MIMO OFDM receiver.

TABLE I
SPECIFICATION OF THE MULTIMODE MIMO OFDM SYSTEM

Operation mode	Channel bandwidth	FFT size	Max. multipath delay (1/4 guard interval)	FFT input/output throughput rate
1~8-stream MIMO	300 MHz	256-point	213.33 ns	1~8×300 Msample/s
High-speed	2.4 GHz	256-point	26.67 ns	2.4 Gsample/s

a wideband OFDM signal from a single antenna. Thus, the system has high scalability to choose suitable MIMO configuration and bandwidth depending on different applications and channel conditions which is the trend for advanced wireless communications. The specification of this MIMO OFDM system is summarized in Table I. It can cover 213.33 ns and 26.67 ns delay spread in MIMO mode and high-speed mode, respectively.

Before designing the DVFS FFT processor for our MIMO OFDM system, two issues should be taken into account. First, to fulfill the system specification in different modes, the 256-point FFT unit needs to support 1–8-stream 300-Msample/s or 2.4-Gsample/s FFT computations. Besides, since the operation mode may be changed from packet to packet, both DFS and DVS schemes must have fast response time to increase the scaling efficiency for low power consumption. To satisfy these two requirements, a novel multimode DVFS FFT processor with fast voltage/frequency scaling is proposed as shown in Fig. 2. It consists of a clock generator, a DVFS controller, a DVS detection unit, and an FFT processing engine. Here we employ a divider-based clock generator to provide different clock frequencies for DFS as shown in Fig. 3. It can achieve fast control of clock phase/frequency compared to the phase-locked loop (PLL). Cooperating with this divided clock, the FFT processing engine in Fig. 2 is designed to support multimode FFT computations with DVFS capability. FFT inputs are first scheduled by the input scheduler and then calculated by the two FFT cores in different power and clock domains. The minimal supply voltages are estimated by the DVS detection unit where two voltage detectors are employed for each FFT core. Based on these detection results, the off-chip DC-DC converter adjusts its two power supplies to reduce the power consumption. More detailed descriptions of the FFT processing engine and the voltage scaling scheme will be presented in Sections III–VII.

III. RADIX-2^4 FFT ALGORITHM

Given a complex input sequence $x(n)$, an N-point discrete Fourier transform (DFT) is defined as

$$X(k) = \sum_{n=0}^{N} x(n) W_N^{kn}, \quad k = 0, 1, \ldots, N-1 \qquad (1)$$

where $W_N^{nk} = e^{-j(2\pi nk/N)}$ is known as the twiddle factor. Due to the high computational complexity $O(N^2)$ in (1), the radix-r FFT algorithms which have lower complexity $O(N \log_r N)$ have been widely adopted in DFT implementations. Besides, since high-radix FFT algorithm has less number of complex multiplications, it is preferred in the hardware design to reduce the number of complex multipliers. As the 256-point FFT comparison shown in Table II, the number of complex multiplication for radix-16 algorithm is 225, which is only about

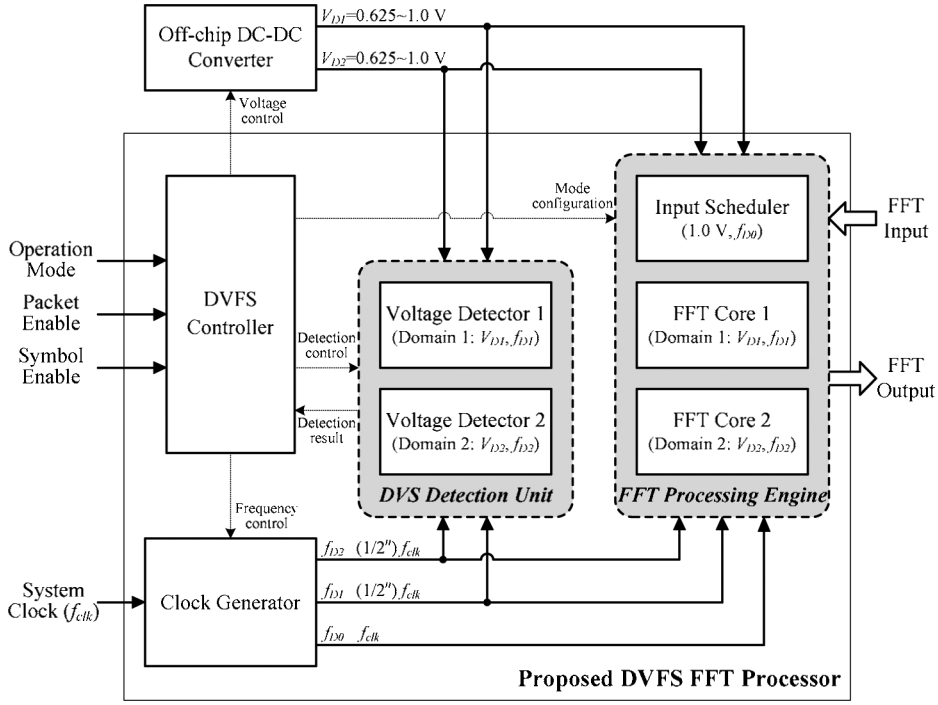
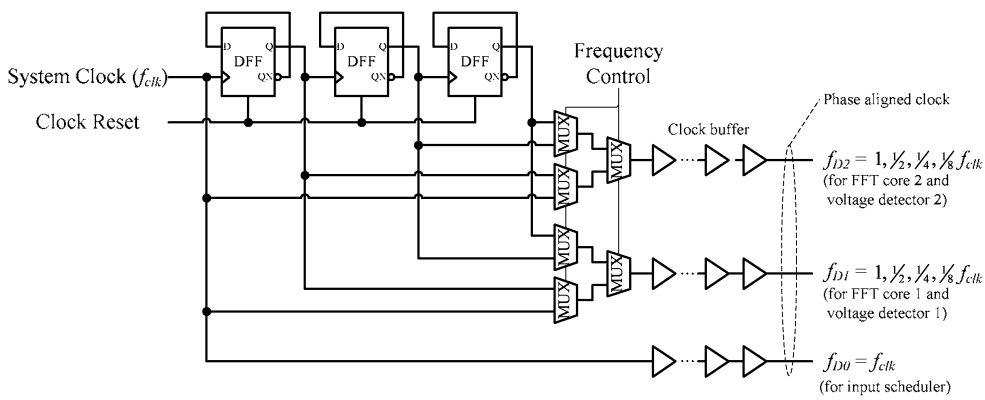


Fig. 2. Block diagram of the proposed DVFS FFT processor.



Mode	Domain 1 frequency (f_{D1})	Domain 2 frequency (f_{D2})
1-stream MIMO	$\frac{1}{8} f_{clk}$	$\frac{1}{8} f_{clk}$
2-stream MIMO	$\frac{1}{4} f_{clk}$	$\frac{1}{4} f_{clk}$
3-stream MIMO	$\frac{1}{2} f_{clk}$	$\frac{1}{4} f_{clk}$
4-stream MIMO	$\frac{1}{2} f_{clk}$	$\frac{1}{2} f_{clk}$
5-stream MIMO	f_{clk}	$\frac{1}{4} f_{clk}$
6-stream MIMO	f_{clk}	$\frac{1}{2} f_{clk}$
7-stream MIMO	f_{clk}	f_{clk}
8-stream MIMO	f_{clk}	f_{clk}
High-speed	f_{clk}	f_{clk}

Fig. 3. Divider-based clock generator for DFS.

TABLE II
COMPARISON OF DIFFERENT ALGORITHMS FOR A 256-POINT FFT

Algorithm	Radix-2	Radix-4	Radix-8/4	Radix-16
Number of complex multiplication	769 (100%)	513 (66.7%)	385 (50.1%)	225 (29.3%)

29.3% of that for radix-2 algorithm. Therefore, we choose radix-16 algorithm in our 256-point FFT design. The derivation is described below. Since $N = 256$ in (1), we first let

$$\begin{aligned} n &= 16n_1 + n_2, \text{ where } n_1, n_2 = 0, 1, \ldots, 15 \\ k &= k_1 + 16k_2, \text{ where } k_1, k_2 = 0, 1, \ldots, 15. \end{aligned} \tag{2}$$

By (2), (1) can be rewritten as

$$\begin{aligned} &X(16k_2 + k_1) \\ &= \sum_{n_2=0}^{15} \sum_{n_1=0}^{15} x(16n_1 + n_2)\, W_{256}^{(16n_1+n_2)(16k_2+k_1)} \\ &= \underbrace{\sum_{n_2=0}^{15} \left\{ \underbrace{\sum_{n_1=0}^{15} x(16n_1 + n_2) W_{16}^{n_1 k_1}}_{16-\text{point DFT}} \underbrace{W_{256}^{n_2 k_1}}_{\text{twiddle factor}} \right\} W_{16}^{n_2 k_2}}_{16-\text{point DFT}} \\ &= \sum_{n_2=0}^{15} \{\mathrm{BU}_{16}(k_1, n_2)\}\, W_{16}^{n_2 k_2}. \end{aligned} \tag{3}$$

Eq. (3) can be considered as processing a two-dimensional DFT where each dimension is built by a 16-point DFT. To implement the 16-pint DFT more efficiently, we use the radix-2^4 FFT algorithm which can easily be derived from the radix-2^3 algorithm [8]. By further decomposing the radix-16 DFT into four steps by applying radix-2 index map, we first rewrite n_1 and k_1 as

$$\begin{aligned} n_1 &= 8\alpha_1 + 4\alpha_2 + 2\alpha_3 + \alpha_4, \text{ where } \alpha_1, \alpha_2, \alpha_3, \alpha_4 = 0, 1 \\ k_1 &= \beta_1 + 2\beta_2 + 4\beta_3 + 8\beta_4, \text{ where } \beta_1, \beta_2, \beta_3, \beta_4 = 0, 1. \end{aligned} \tag{4}$$

By means of (4), the first 16-point DFT in (3) is rewritten as (5), shown at the bottom of the page, where the radix-16 DFT is completed by the four-step radix-2^4 algorithm. Similarly, by reformulating n_2 and k_2 with

$$\begin{aligned} n_2 &= 8\gamma_1 + 4\gamma_2 + 2\gamma_3 + \gamma_4, \text{ where } \gamma_1, \gamma_2, \gamma_3, \gamma_4 = 0, 1 \\ k_2 &= \lambda_1 + 2\lambda_2 + 4\lambda_3 + 8\lambda_4, \text{ where } \lambda_1, \lambda_2, \lambda_3, \lambda_4 = 0, 1. \end{aligned} \tag{6}$$

The second 16-point DFT in (3) can also be transformed to radix-2^4 FFT as (7), shown at the bottom of the next page.

Thus, by (3), (5), and (7), the 256-point radix-2^4 FFT is fully computed. The corresponding signal flow graph (SFG) of this 256-point FFT is shown in Fig. 4. Note that the 256-point FFT is divided into two stages, where radix-16 FFT algorithm is employed in each stage. The black point between these two stages means that the twiddle factor will be multiplied at that point. Each butterfly of the radix-16 algorithm is further decomposed into four steps. The twiddle factors, W_8^1 and W_8^3 in the second step and W_{16}^n in the third step, can be implemented by constant complex multiplications with simple shifters and adders. The canonical signed digit (CSD) technique [9] can also be applied to further reduce the hardware complexity.

IV. Architecture of the FFT Processing Engine

According to the radix-2^4 algorithm described in Section III, we propose a novel MMDF structure for the FFT processing engine in Fig. 2 supporting DVFS operations and multi-stream computations. This 256-point FFT processing engine consists of an input scheduler, FFT core 1, FFT core 2, and level shifters as shown in Fig. 5. The features of the proposed FFT structure are as follows.

- high throughput rate up to 8-stream 300-Msample/s or 2.4-Gsample/s computations can be provided by using parallel-8 data-paths;
- multimode operations such as 1–8-stream 256-point FFTs or a high-speed 256-point FFT are supported for MIMO OFDM applications;

$$\begin{aligned} &\sum_{n_1=0}^{15} x(16n_1 + n_2) W_{16}^{n_1 k_1} \\ &= \sum_{\alpha_4=0}^{1} \sum_{\alpha_3=0}^{1} \sum_{\alpha_2=0}^{1} \sum_{\alpha_1=0}^{1} x(16(8\alpha_1 + 4\alpha_2 + 2\alpha_3 + \alpha_4) + n_2) W_{16}^{(8\alpha_1+4\alpha_2+2\alpha_3+\alpha_4)(\beta_1+2\beta_2+4\beta_3+8\beta_4)} \\ &= \underbrace{\sum_{\alpha_4=0}^{1} \underbrace{\sum_{\alpha_3=}^{1} \underbrace{\sum_{\alpha_2=0}^{1} \underbrace{\sum_{\alpha_1=0}^{1} x(16(8\alpha_1 + 4\alpha_2 + 2\alpha_3 + \alpha_4) + n_2) W_2^{\alpha_1\beta_1} \underbrace{W_4^{\alpha_2\beta_1}}_{\text{twiddle factor}} W_2^{\alpha_2\beta_2}}_{\text{step 1}} \underbrace{W_8^{\alpha_3(\beta_1+2\beta_2)}}_{\text{twiddle factor}} W_2^{\alpha_3\beta_3}}_{\text{step 2}} \underbrace{W_{16}^{\alpha_4(\beta_1+2\beta_2+4\beta_3)}}_{\text{twiddle factor}} W_2^{\alpha_4\beta_4}}_{\text{step 3}}}_{\text{step 4}} \end{aligned} \tag{5}$$

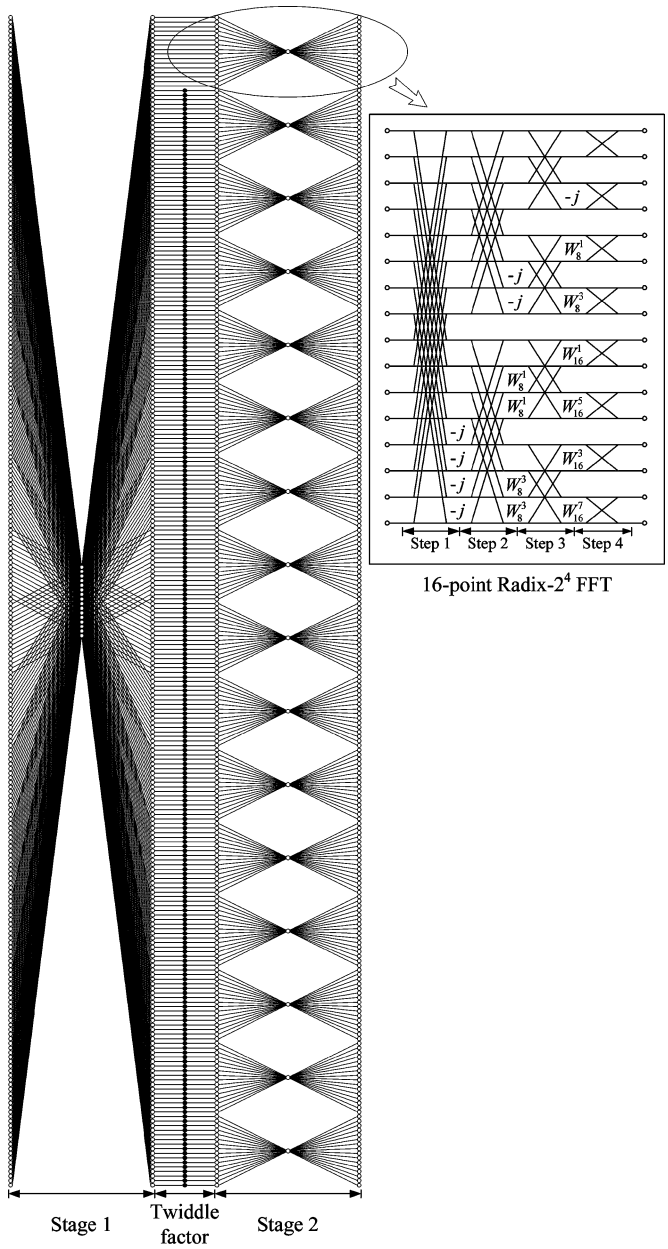


Fig. 4. Signal flow graph (SFG) of the radix-2^4 256-point FFT.

- data-paths are slowed down by the input scheduler in low-throughput modes to support both frequency and voltage scaling;
- radix-2^4 algorithm and scheduling technique are employed to reduce the number of complex multipliers and the power consumption.

In the proposed MMDF structure, the function of the input scheduler is to rearrange the input order and data rate for FFT core 1 and core 2. Because the operation speed remains the same for all modes, the input scheduler is located in the fixed supply domain (default 1.0 V). After the scheduling, the multimode 256-point FFT computations are processed by the two FFT cores in which eight parallel-paths are adopted to increase the maximum throughput. Due to various MIMO configurations, FFT core 1 and core 2 are operated in separated power domains (0.625–1.0 V) for independent voltage and frequency scaling as shown in Fig. 5. The FFT cores are further partitioned into Module 1 to 4 for detailed explanation. Modules 1 and 2 are used to implement the first radix-2^4 stage, the twiddle factor multiplications and the first step of the second radix-2^4 stage. Then, the last three steps of the second radix-2^4 stage are mapped to Modules 3 and 4. Between the power domain boundaries, high-to-low or low-to-high level shifters are employed for voltage level conversion. More detailed descriptions of each functional block will be given below.

A. Input Scheduler

The input scheduler is designed in the FFT processing engine for two purposes. One is to schedule the order of the input sequence such that multimode FFT computations can be processed efficiently and correctly. The other is to distribute the multiple FFT streams into eight paths to slow down the data sample rate in low-throughput modes. Block diagram of the input scheduler is shown in Fig. 6(a). It is composed of seven input delay units, a switch and hold unit, and seven output delay units. The switch and hold unit further consists of a switch network, a bus Barrel shifter [10], and 8-word registers. Here the scheduling of 3-stream MIMO is shown as an example in Fig. 6(b). Ai, Bi, and Ci are the three input streams where i is the index number from 0 to 255. These inputs are first adjusted by different input delay and then passed to the switch and hold unit. The initial switch path (at $t0$) is determined by the switch

$$X(16k_2+k_1) = \underbrace{\underbrace{\underbrace{\underbrace{\sum_{\gamma_4=0}^{1}\sum_{\gamma_3=}^{1}\sum_{\gamma_2=0}^{1}\sum_{\gamma_1=0}^{1}\mathrm{BU}_{16}(k_1,\gamma_1,\gamma_2,\gamma_3,\gamma_4)W_2^{\gamma_1\lambda_1}\ \underbrace{W_4^{\gamma_2\lambda_1}}_{\text{twiddle factor}}}_{\text{step 1}}\ W_2^{\gamma_2\lambda 2}\ \underbrace{W_8^{\gamma_3(\lambda_1+2\lambda_2)}}_{\text{twiddle factor}}}_{\text{step 2}}\ W_2^{\gamma_3\lambda 3}\ \underbrace{W_{16}^{\gamma_4(\lambda_1+2\lambda_2+4\lambda_3)}}_{\text{twiddle factor}}}_{\text{step 3}}\ W_2^{\gamma_4\lambda_4}}_{\text{step 4}} \tag{7}$$

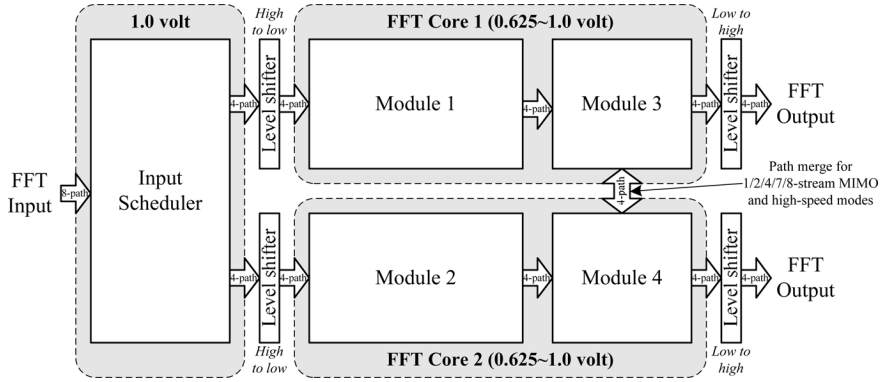


Fig. 5. Block diagram of the FFT processing engine.

network and the succeeding switching (from $t1$ to $t255$) is the cyclic shifting of the initial configuration which is performed by the bus Barrel shifter. Since only three streams are distributed into eight data-paths, five-path data are held by registers in each time slot as shown in Fig. 6(b). Afterward, the outputs of the switch and hold unit are adjusted by the output delay units which completes the input scheduling. As we can see, streams A and B with the same index number are scheduled in neighbor that allows the same twiddle factor to be multiplied successively for reduced switching power. Besides, the output sample rate becomes half and one fourth of the original one such that the FFT cores can work in lower clock frequency. The outputs of the input scheduler for all operation modes are depicted in Fig. 6(c). We can see that every stream inputs are evenly distributed to the eight paths in 1/2/4/7/8-stream MIMO and high-speed modes. As for 3/5/6-stream MIMO mode, the stream inputs are separated into two groups which has four paths. By this way, the two-group data can be processed using independent clock frequencies for better scaling efficiency. Also shown in Fig. 6(c), since the required order for high-speed mode can be obtained from the de-multiplexer (DEMUX) output directly (Fig. 1), the operation of the input scheduling is skipped in this mode.

B. Module 1 and Module 2

The block diagram of Module 1 (Module 2) with four data-paths is shown in Fig. 7. It consists of five butterfly units (BU), five FIFOs, four trivial complex multipliers, and a complex multiplier in each path. Module 1 and 2 are mapped from the four-step radix-2^4 algorithm to implement the first radix-2^4 stage, the twiddle factor multiplications and the first step of the second radix-2^4 stage in Fig. 4. Since the parallel 8-path FFT structure does not have a path merging (data for BU processing come from different paths) until the final three steps, each path in Module 1 and 2 has independent data flow as shown in Fig. 7. Besides, to support MIMO FFT, the FIFO size is configured according to the stream number such that data with correct indexes can be acquired by BU to perform complex addition and subtraction. Take the first-stage FIFO for example, the FFT inputs $x(n)$ and $x(n+128)$ must arrive at BU inputs simultaneously to implement the radix-2^4 algorithm. In 1/2/4/7/8-stream MIMO and high-speed modes, the FFT inputs are evenly distributed into eight paths as shown in Fig. 6(c). Therefore, the FIFO size should be $16p$-word where p is the total stream number. As for 3/5/6-stream MIMO mode, since Modules 1 and 2 work separately (inputs are distributed into four paths), the FIFO size should be $32q$-word where q is the stream number processed by the corresponding Module. Thus, the structure of the first-stage FIFO can be found in Fig. 7 where a table of FIFO size is also included. Among the BU outputs, only the fourth stage adopts complex multipliers for twiddle factor multiplication. The trivial twiddle factors in other stages can be implemented with simple constant multipliers and multiplexers (MUXs).

C. Module 3 and Module 4

The block diagram of Module 3 and 4 is depicted in Fig. 8. They consist of 16 BUs, eight FIFOs, eight trivial complex multipliers, and eight MUXs. Module 3 and 4 are responsible to calculate the last three steps of the second radix-2^4 stage in Fig. 4. For 3/5/6-stream MIMO modes, since these two Modules work independently, the MUXs are configured such that there is no data transfer between Modules 3 and 4. On the other hand, only the four first-stage BUs in Module 4 are required (first-stage BUs in Module 3 are skipped) to perform the path merging for 1/2/4/7/8-stream MIMO and high-speed modes. Similar to Modules 1 and 2, the FIFO size also depends upon the stream number as shown in Fig. 8. Note that for 1/2/4/7/8-stream MIMO and high-speed modes, no FIFO is required because the data can be directly acquired by BU from different paths.

V. Open-Loop Voltage Detection and Scaling Scheme

For DVFS designs, a robust, accurate, and fast voltage scaling mechanism is important to insure the chip performance and to reduce the power consumption. However, due to the increasing chip variation in advanced process technologies, it is difficult to achieve these three goals simultaneously. Traditionally, the voltage scaling scheme can be categorized into two types. One is to scale the supply voltage to a predetermined value from simulated results for each operation frequency [3], [4], and the other is to perform real-time voltage detection and scaling during the chip operations [5]–[7]. For the first method, because of the process uncertainty, the scaled supply voltage is estimated from worst-case simulation. Although the correct chip functionality can be assured in these designs; however, the scaling efficiency for power consumption is low due to a conservative voltage reduction. To reach more optimal scaling results, the real-time

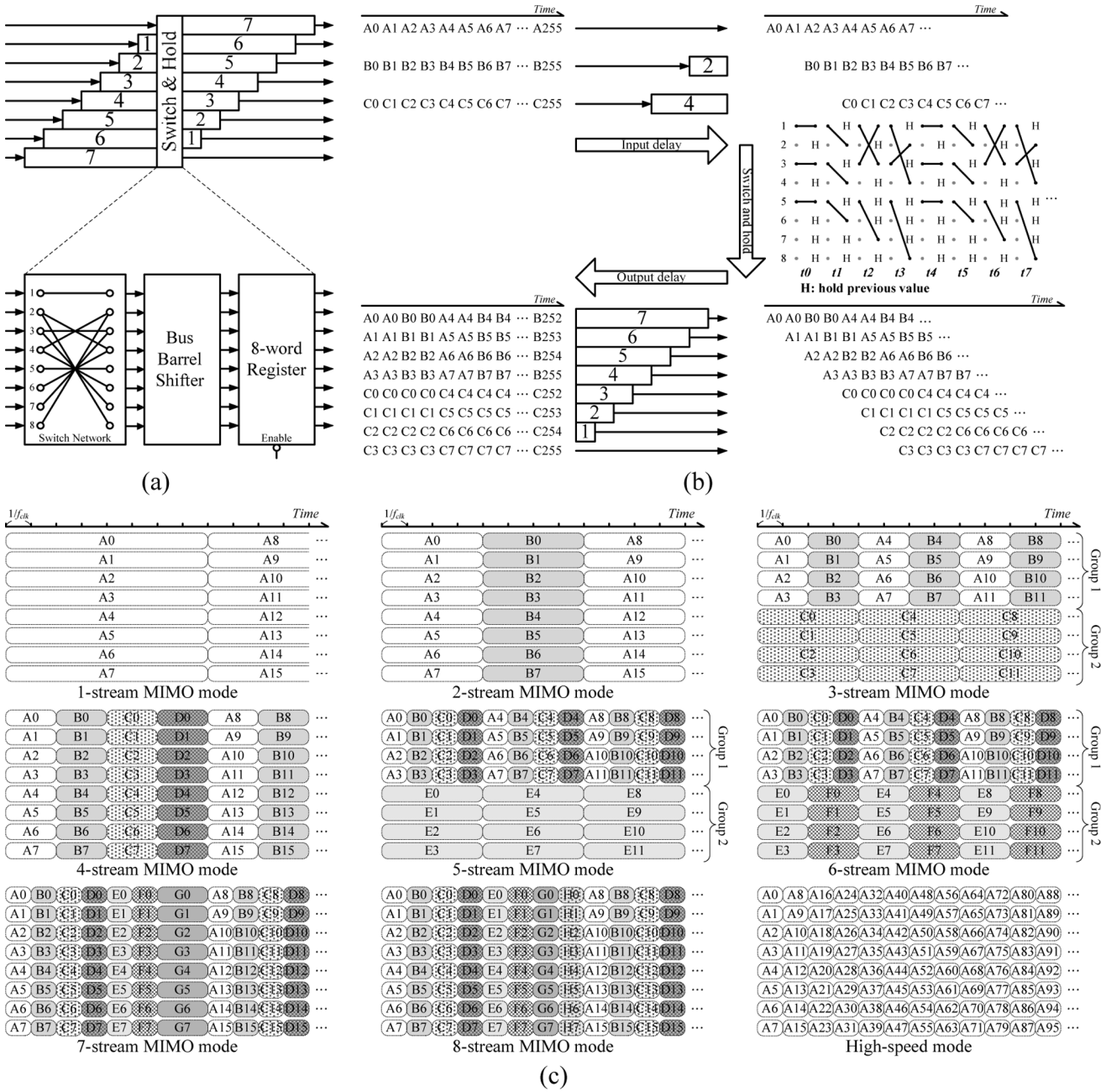
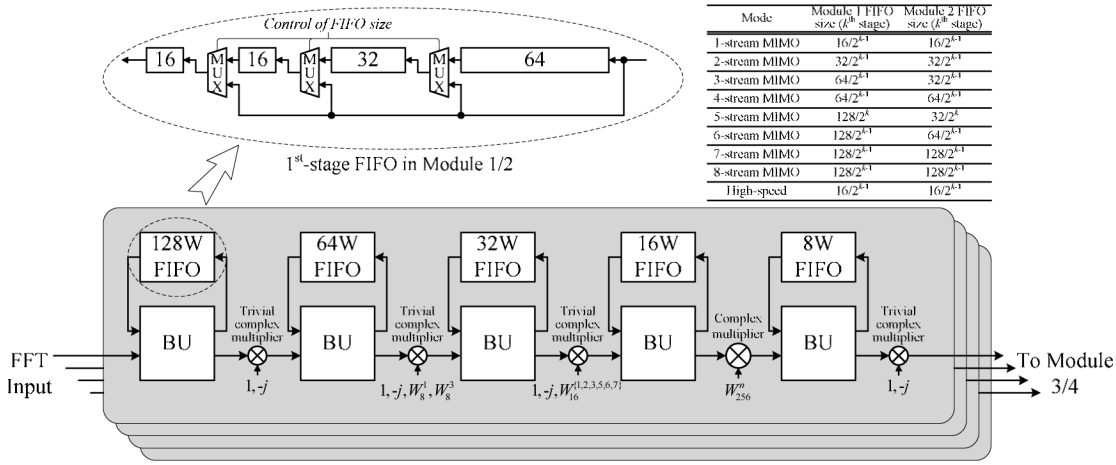


Fig. 6. (a) Block diagram. (b) 3-stream MIMO operation. (c) Output of the input scheduler.

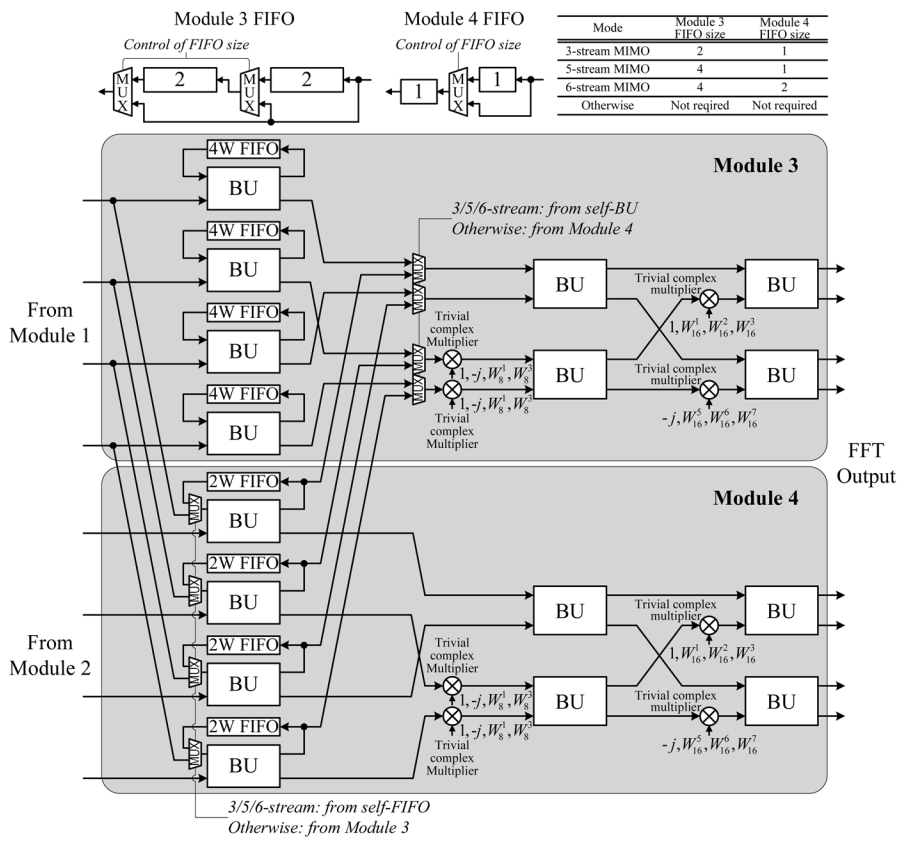
voltage detection has been proposed using a critical-path replica to monitor the functionality under different supply voltages [5]–[7]. In these detection-based designs, different control algorithms have been proposed for aggressive voltage scaling and robust operations, but long convergence time is required for the scaling operation. This is because that the voltage must be decreased gradually to find the optimal operation point without causing any errors. For our DVFS FFT processor, since the operation mode may switch rapidly from packet to packet, a fast voltage detection scheme is demanded to increase the scaling efficiency.

To achieve better scaling efficiency, we propose an open-loop voltage detection and scaling mechanism with calibration. At the beginning, the detector's calibration is performed once when the chip is powered on as shown in Fig. 9. For each operation frequency (1, 1/2, 1/4, and 1/8 f_{clk}), the timing margin is calculated from high to low voltages until a timing violation occurs. After all the timing information is collected in the detector's calibration, the proposed OLVDS scheme switches to the voltage detection and scaling mode for FFT processing. Whenever a new OFDM packet arrives (in different operation modes), the supply voltage is scaled to a "safe" voltage shortly according to the calibration data for the current operation frequency. Thus, fast and robust voltage scaling can be easily achieved. Besides, voltage detection for further voltage scaling is then performed during FFT processing to take account of voltage and temperature variations. By calculating the timing margin for the target voltage without changing the supply voltage, the proposed detection method decides if further voltage reduction can be applied with fast response. The de-



Mode	Module 1 FIFO size (k^{th} stage)	Module 2 FIFO size (k^{th} stage)
1-stream MIMO	$16/2^{k-1}$	$16/2^{k-1}$
2-stream MIMO	$32/2^{k-1}$	$32/2^{k-1}$
3-stream MIMO	$64/2^{k-1}$	$32/2^{k-1}$
4-stream MIMO	$64/2^{k-1}$	$64/2^{k-1}$
5-stream MIMO	$128/2^{k}$	$32/2^{k}$
6-stream MIMO	$128/2^{k-1}$	$64/2^{k-1}$
7-stream MIMO	$128/2^{k-1}$	$128/2^{k-1}$
8-stream MIMO	$128/2^{k-1}$	$128/2^{k-1}$
High-speed	$16/2^{k-1}$	$16/2^{k-1}$

Fig. 7. Block diagram of Module 1/2 in the FFT processing engine.



Mode	Module 3 FIFO size	Module 4 FIFO size
3-stream MIMO	2	1
5-stream MIMO	4	1
6-stream MIMO	4	2
Otherwise	Not reqired	Not required

Fig. 8. Block diagram of Module 3 and 4 in the FFT processing engine.

tailed OLVDS design and its operation procedure are described as follows.

A. Hardware Structure of the OLVDS Design

Block diagram of the proposed OLVDS design is shown in Fig. 10. It consists of a DVFS controller, two voltage detectors, an off-chip DC-DC converter, a clock generator, and level shifters for voltage level conversion. Each voltage detector including four identical detection units is responsible to detect the minimal supply voltage for one FFT core. To take geometry variation into account, the detection units are placed in different chip locations. Each detection unit further comprises of two D-type flip-flops (DFF) as I/O registers, a critical-path replica of the FFT core, and a tunable delay line. As shown in Fig. 10, the critical-path replica is built by a series of delay line cells and inverters with balance rise/fall time. These delay line cells have the same channel length as other logic cells such that they have similar delay characteristics over different voltages. Here the inverters are employed to balance the overall rise/fall delay of the critical-path replica. In our current design, additional 160 picosecond delay (in nominal voltage) is included in the critical-path replica as the design margin accounting for PVT variations and the mismatch of critical-path replica. The tunable delay line is built by buffer (BUF) and transmission-gate MUX

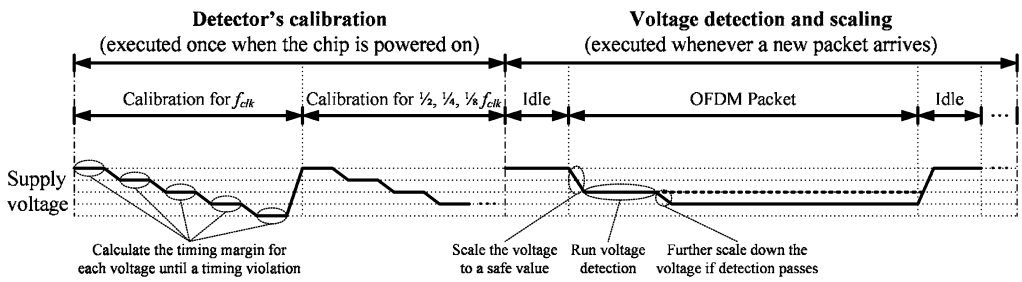


Fig. 9. Scheduling of the proposed OLVDS scheme.

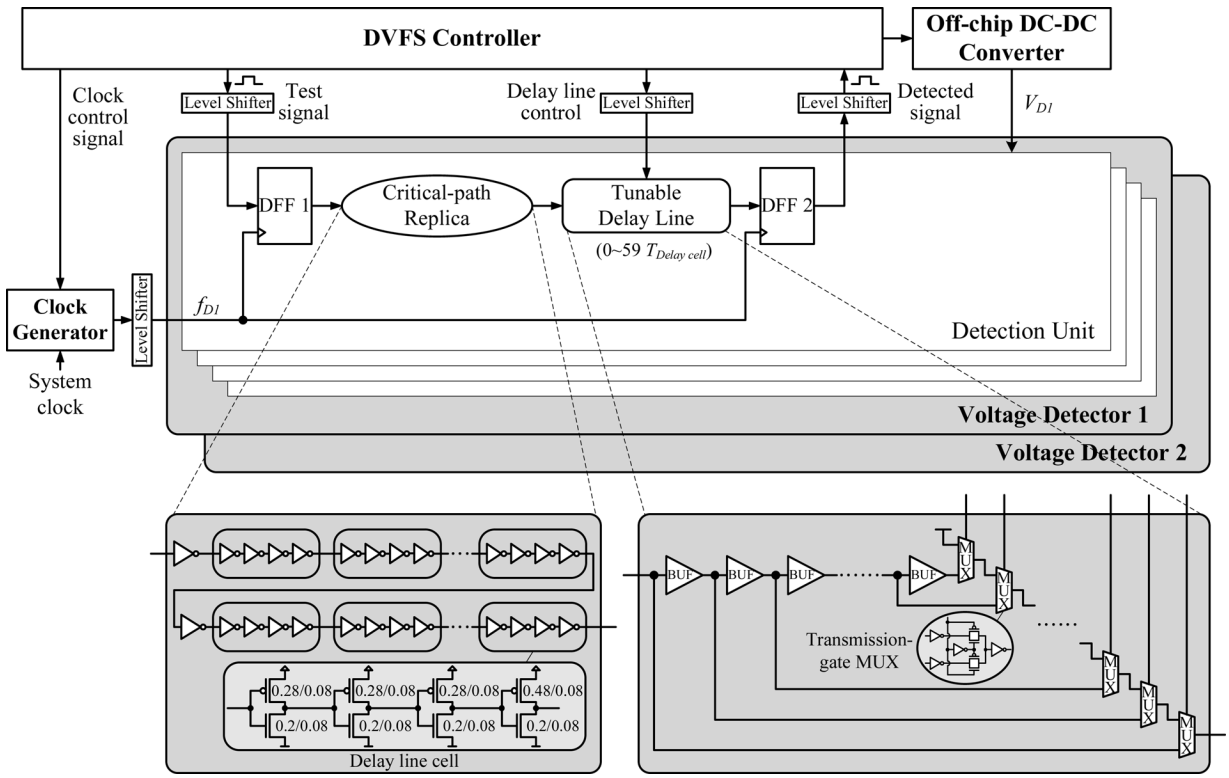


Fig. 10. Block diagram of the proposed OLVDS design.

cells with balanced rise/fall time. The overall OLVDS design is verified at design time by running fast SPICE simulation under corner conditions.

B. Operations of the OLVDS Scheme

Since the same OLVDS operation is employed for the two power domains, only the control flow for domain 1 is depicted in Fig. 11 for simplicity. When the chip is powered on as shown in Fig. 11(a), OLVDS starts in the detector's calibration mode. At the beginning, the operation frequency is set to f_{clk} and supply voltage is set to the nominal value (1.0 volt) for timing margin estimation. Here we define one BUF plus one MUX in Fig. 10 as the delay unit. As the timing chart shown in Fig. 12, a one-cycle pulse train is used as the test signal for the voltage detector in Fig. 10. If the delay under test (critical-path replica plus tunable delay line) is longer than the clock period, the detected signal will be shifted from its expected position. To estimate the timing margin in V_{D1_0}, the number of added delay units in the tunable delay line is swept from 59 to 0 to find the number of allowed delay units (timing margin) which is to be saved in the table. If this number is greater than or equal to 0, the supply voltage is scaled down by Δ (25 mV) and the same timing margin estimation is performed. This procedure repeats until the delay of critical-path replica is longer than the clock period (timing violation) in a certain voltage as shown in Fig. 12. In this way, a calibration table for f_{clk} can be obtained as shown in Table III where $N(V_{D1_i})$ is the number of allowed delay units in V_{D1_i}. Because four clock frequencies (1, 1/2, 1/4, and 1/8 f_{clk}) are adopted for different operation modes in the proposed design, the calibration tables for 1/2, 1/4, and 1/8 f_{clk} must also be generated as shown in Fig. 11(a) for further voltage detection and scaling operations.

After the calibration tables for all operation frequencies are collected in the detector's calibration mode, OLVDS goes to the voltage detection and scaling mode. As shown in Fig. 11(b), whenever a new OFDM packet arrives, the corresponding calibration table is chosen according to the operation mode of the incoming packet. Here we assume that the minimal supply

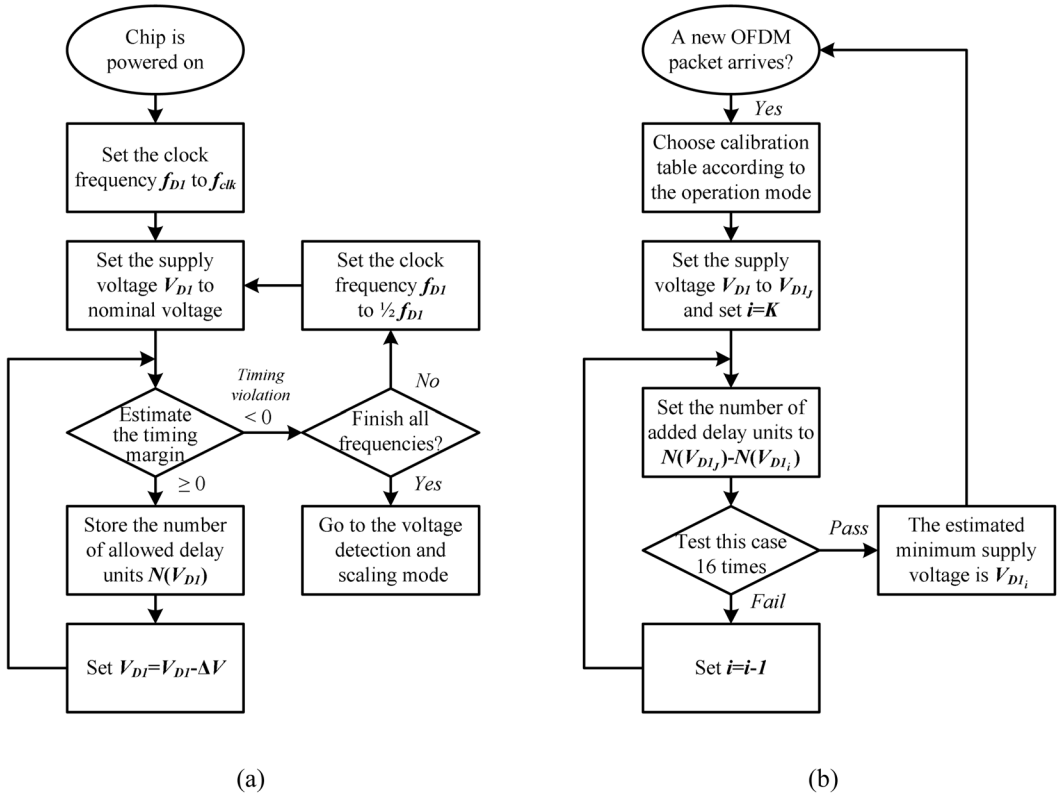


Fig. 11. Control flow of the OLVDS scheme for domain 1. (a) Detector's calibration mode. (b) Voltage detection and scaling mode.

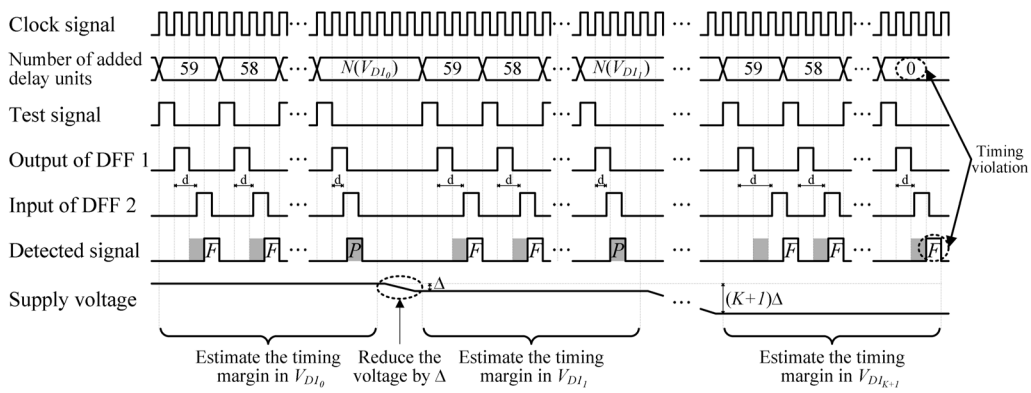


Fig. 12. Timing chart in the detector's calibration for domain 1.

TABLE III
CALIBRATION DOMAIN 1

Supply voltage	Allowed number of delay units
$V_{D1_0}=1.0$	$N(V_{D1_0})$
$V_{D1_1}=1.0-\Delta$	$N(V_{D1_1})$
$V_{D1_2}=1.0-2\Delta$	$N(V_{D1_2})$
⋮	⋮
$V_{D1_K}=1.0-K\Delta$	$N(V_{D1_K})$
$V_{D1_{K+1}}=1.0-(K+1)\Delta$	Timing violation

voltage is V_{D1_K} from the calibration table and the "safe" voltage is V_{D1_J} which is $(K-J)\Delta$ higher than V_{D1_K}. The supply voltage is scaled to V_{D1_J} for low power at the beginning of the packet. Then the critical-path replica plus additional $N(V_{D1_J})-N(V_{D1_K})$ delay units (from tunable delay line) are tested for 16 times to see if the voltage can be scaled to V_{D1_K}. If all 16 tests pass, the supply voltage is scaled to V_{D1_K} to save more power. Otherwise, a Δ higher voltage is tested again and the procedure repeats. An example is given in Fig. 13 for illustration. In this example, the nth test signal for V_{D1_K} is not received in the correct cycle which means V_{D1_K} is not a stable voltage for chip operations. Therefore, the number of added delay units is set to $N(V_{D1_J})-N(V_{D1_{K-1}})$ for detection of $V_{D1_{K-1}}$. Since all 16 tests for $V_{D1_{K-1}}$ are passed in this example, further $(K-J-1)\Delta$ can be reduced in the supply voltage. As described above, the proposed OLVDS scheme does not adjust the supply voltage for voltage detection, and therefore it has fast response time. Besides, the voltage detection has good accuracy by taking account of real-time

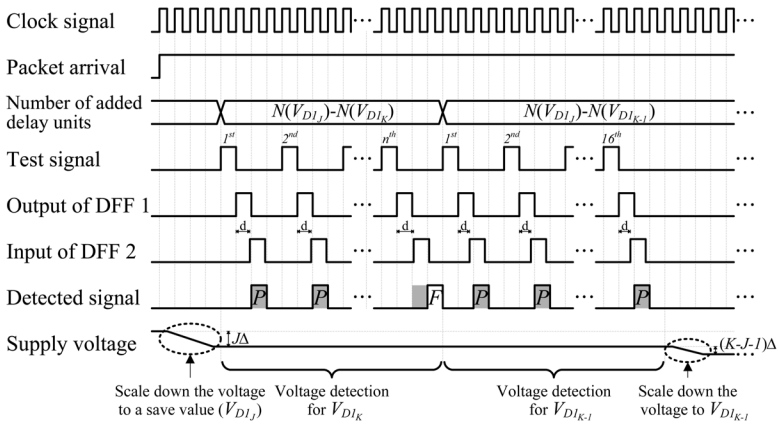


Fig. 13. Timing chart in the voltage detection and scaling for domain 1.

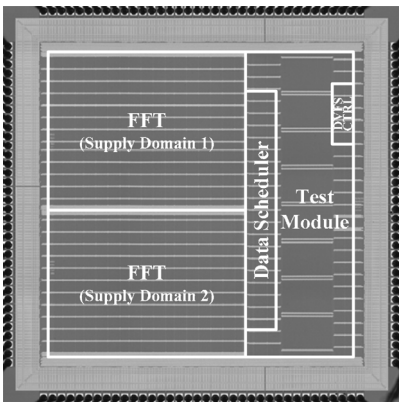


Fig. 14. Chip micrograph.

TABLE IV
CHIP SUMMARY OF THE PROPOSED DVFS FFT PROCESSOR

Items	Specification
FFT size	256-point
Technology	UMC 90 nm 1P9M CMOS process $\|V_{TH}\|$=0.26±0.04 V
Package	144 CQFP
Core supply voltage	1.0 V (Test module and scheduler) 0.625~1.0 V (FFT cores)
Max. working frequency	447 MHz@1.0 V (TT) 340 MHz@1.0 V (SS) 500 MHz@1.0 V (FF)
Core size (incl. test module)	1.88×1.88 mm^2
Gate count (excl. test module)	583K
Core power consumption for 8-stream 300-Msample/s FFT	160.5 mW@1.0 V (TT) 160.9 mW@1.0 V (SS) 177.7 mW@1.0 V (FF)
Core power consumption for 2.4-Gsample/s FFT	145.5 mW@1.0 V (TT) 143.2 mW@1.0 V (SS) 164.7 mW@1.0 V (FF)

voltage and temperature variations during packet receiving (FFT processing).

VI. CHIP IMPLEMENTATION

At the beginning of the chip design, the parallelized radix-2^4 FFT algorithm is coded in MATLAB language. From fixed-point simulation, 8-bit input wordlength and 11-bit output wordlength are chosen and the implementation loss is within 0.1 dB for QPSK/16-QAM modulation at 17 dB signal-to-noise ratio (SNR). The resulting signal-to-quantization-noise ratio (SQNR) of this 256-point FFT processor is over 35.8 dB. Then the architecture of the proposed FFT processor is modeled in Verilog and functionally verified using NC-Verilog simulator. Besides, we also use UltraSim mixed-mode simulator with Verilog/SPICE language to verify the DVFS operation under different process and temperature conditions. A test chip of the proposed DVFS FFT processor has been fabricated in UMC 90-nm single-poly nine-metal (1P9M) CMOS process. The core size including the test module is 1.88×1.88 mm^2 as shown in Fig. 14. The gate count of the OLVDS design (including DVFS controller and voltage detectors) is only 4.6 K which occupies 0.8% of the chip gate count. Due to the speed limitation of chip I/O, a digitally controlled oscillator (DCO) [11] and 11.3-kbit two-port SRAM with 8 banks are employed in the test module for high-speed testing. FFT inputs are first read from the input pins and stored to SRAM serially using the external clock (normal-speed). Then, the DVFS FFT processor starts to calculate 256-point FFT in parallel from the eight-bank outputs of SRAM using the DCO clock (high-speed). After the results are stored back to SRAM, it can be read from the output pins serially using the external clock. This chip is packaged in a 144-pin CQFP where 85 pins are signal pins and others are power pins.

VII. MEASUREMENT RESULT AND ANALYSIS

In order to verify the proposed ideas, fifteen chips from three process corners (TT, SS, and FF) have been packaged for testing. These chips are measured using Agilent 93000 SOC test system and the chip summary is shown in Table IV. The maximum throughput of our proposed FFT IC in TT corner is up to 3.58 Gsample/s at the nominal voltage. The power consumption for 8-stream 300-Msample/s FFTs and a 2.4-Gsample/s FFT is 160.5 mW and 145.5 mW, respectively (TT corner at 1.0 V). Besides, the voltage detection result and the scaled power performance for all operation modes are also measured. As shown in Table V, the differences between the detected and the required supply voltages are within 0.1 V for all process corners without causing functional errors (in steps of 25-mV resolution). This voltage detection error mainly comes from the critical-path replica and it can be improved by adopting more sophisticated designs [5], [12]. The power

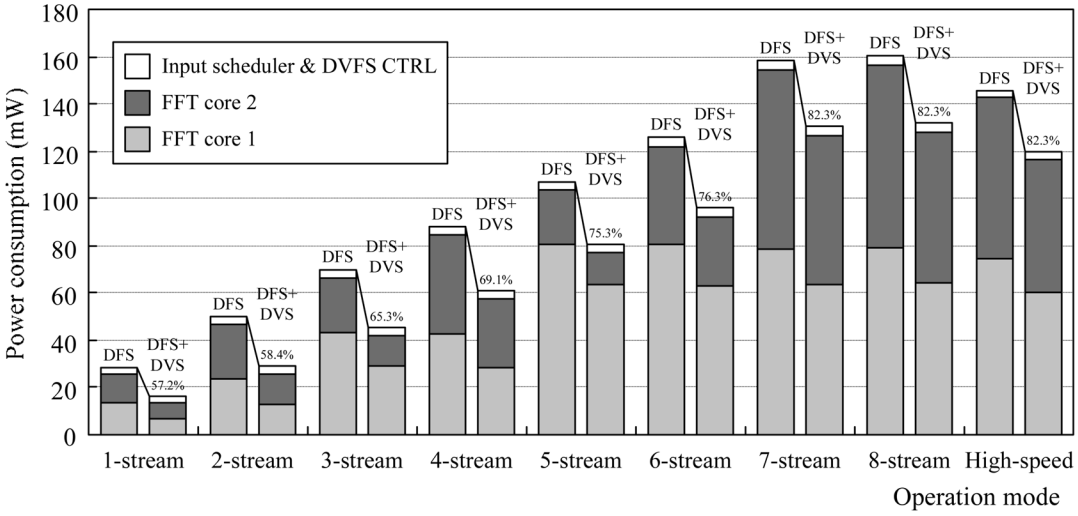


Fig. 15. Measured power consumption under different operation modes (TT corner).

TABLE V
DETECTED SUPPLY VOLTAGE AND REQUIRED SUPPLY VOLTAGE

Mode	1-stream MIMO	2-stream MIMO	3-stream MIMO	4-stream MIMO	5-stream MIMO	6-stream MIMO	7-stream MIMO	8-stream MIMO	High-speed
Required supply voltage in TT (volt)	0.625	0.625	0.65/ 0.625	0.675	0.75/ 0.625	0.775/ 0.625	0.825	0.825	0.8
Detected supply voltage in TT (volt)	0.625	0.625	0.725/ 0.625	0.725	0.825/ 0.625	0.825/ 0.725	0.85	0.85	0.85
Required supply voltage in FF (volt)	0.625	0.625	0.625/ 0.625	0.625	0.7/ 0.625	0.7/ 0.625	0.75	0.75	0.725
Detected supply voltage in FF (volt)	0.625	0.625	0.675/ 0.625	0.675	0.75/ 0.625	0.75/ 0.675	0.8	0.8	0.725
Required supply voltage in SS (volt)	0.7	0.725	0.75/ 0.725	0.75	0.9/ 0.725	0.9/ 0.75	0.875	0.875	0.9
Detected supply voltage in SS (volt)	0.7	0.725	0.775/ 0.725	0.775	0.975/ 0.725	0.975/ 0.775	0.975	0.975	0.975

consumption of the proposed FFT processor with voltage/frequency scaling is shown in Fig. 15. As we can see, the chip power scales with the throughput rate when DFS is employed. Therefore, the overall power consumption can be optimized for the MIMO OFDM system. Moreover, additional 18% to 43% of the total power can be saved by further including the DVS scheme.

For comparison, the traditional method adopting eight single-path delay feedback (SDF) structures [8] is also implemented with clock gating and the same radix-2^4 algorithm is adopted in this reference design. Assuming all operation modes have equal operation period, the averaged power consumption for different process corners is shown in Fig. 16. When only DFS is activated in our DVFS FFT chip, about 10% of power consumption can be saved which results mainly from the scheduling of multiplication as described earlier. In DFS mode, it is also found that the proposed chip in FF corner has the maximum power consumption among process corners due to large leakage power. This effect can be compensated after DVS is turned on since the chip in FF corner has more timing margin for voltage scaling. The averaged power reduction by DVS is from 11% to 33% for the three process corners and the overall power saving including both DFS and DVS is 39%, 31%, and 19% for FF, TT, and SS corners, respectively. Finally, the chip comparison is given in Table VI. Here we choose two variable-length FFT chips supporting 256-point FFT [13], [14] to compare the energy efficiency. Besides, to mitigate the impact of different technologies and wordlength, the normalized FFTs per energy shown in (8) [15] is employed as the performance index. From Table VI, we can find that [14] and our proposed FFT processor have similar energy efficiency which is higher than that of [13]. However, it should be noted that the FFT processor in [14] is a full-custom

$$\text{Normalized FFTs per energy} = \frac{\left(\frac{\text{Tech}}{90\ \text{nm}}\right) \times \left(\frac{2}{3}\frac{\text{Wordlength}}{10} + \frac{1}{3}\left(\frac{\text{Wordlength}}{10}\right)^2\right) \times \left(\frac{V_{\text{DD}}}{1.0}\right)^2}{\text{Energy} \times 10^{-6}} \tag{8}$$

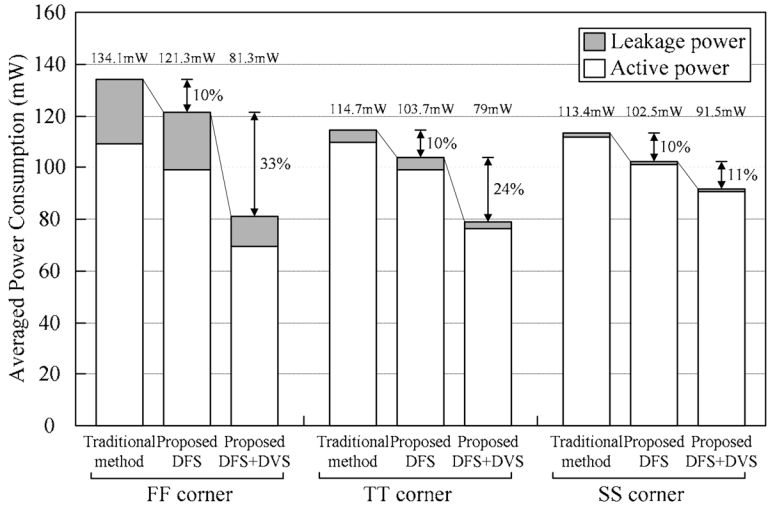


Fig. 16. Averaged power consumption for different process corners.

TABLE VI
FFT CHIP COMPARISON

	Proposed			[13]	[14]
Technology	90 nm			0.25 μm	0.18 μm
Operation voltage	0.625~1.0 V			2.5 V	0.18~0.9 V
FFT mode	1~8 stream MIMO/high-speed 256-point FFT			8~4096-point FFT/IFFT	128~1024-point real-valued FFT
Wordlength	10 bit			16 bit	16 bit
Max. clock rate	447 MHz			200 MHz	6 MHz
Die area	2.26×2.26 mm^2			4.28×4.28 mm^2	2.6×2.1 mm^2
Comparison condition	1-stream @0.625 V, 300 MHz	8-stream @0.85 V, 300 MHz	High-speed @0.85 V, 300 MHz	256-point FFT @2.5 V, 200 MHz	256-point FFT @0.35 V, 10 KHz
Power	16.4 mW	132.2 mW	119.7 mW	360mW	NA
Energy for 256-point complex-valued FFT	14.0 nJ	14.1 nJ	12.8 nJ	2143 nJ	40 nJ*1
Normalized FFTs (million) per energy*2	71.5	70.9	78.3	15.6	77.8

*1: this value is estimated by doubling the energy of a 256-point real-valued FFT.
*2: this value is normalized to the maximum operation voltage of each chip.

design working in the subthreshold region (350 mV) for very low-throughput applications. See equation (8) at the bottom of the previous page.

VIII. CONCLUSION

In this paper, a novel DVFS FFT processor for high-throughput and low-power MIMO OFDM systems has been proposed. By the proposed MMDF architecture and OLVDS scheme, our FFT processor can process 1–8-stream 300-Msample/s 256-point FFTs or a 2.4-Gsample/s 256-point FFT at minimum voltage/frequency. Besides, a parallelized radix-2^4 FFT structure is adopted to save the power consumption and hardware cost of complex multipliers. A test chip of the proposed FFT processor has been designed and fabricated using UMC 90-nm single-poly nine-metal CMOS process with a core area of 1.88×1.88 mm^2. The SQNR performance of this FFT processor is over 35.8 dB to support QPSK/16-QAM modulation. Power dissipation of 2.4 Gsample/s 256-point FFT computations is about 119.7 mW at 0.85 V. Compared to the traditional method, the averaged power reduction by the proposed DVFS FFT design is 39%, 31%, and 19% for FF, TT, and SS corners, respectively.

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