ESD Protection Under Grounded-Up Bond Pads in 0.13 μm Eight-Level Copper Metal, Fluorinated Silicate Glass Low-k Intermetal Dielectric CMOS Process Technology

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***Abstract*—Electrostatic discharge (ESD) protection device under the grounded-up bond pad is investigated in 0.13 μm full eight-level copper metal CMOS process technology with fluorinated silicate glass (FSG) low-k intermetal dielectric (IMD). The bonding force and power produces no cracking and no noticeable change in the second breakdown trigger point (V_{t2}, I_{t2}). High current I–V measured from the different level metal layers stack structures shows that 1) I_{t2} depends very weakly on metal layers used, as expected due to certain junction power dissipation criterion and 2) V_{t2} increases with the number of metal layers. The origin of the latter is increased dynamic impedance for increased metal layer number, as clarified by a simple RC model. The model also yields the *intrinsic* second breakdown trigger current and voltage for the underlying ESD protection device. Successfully configuring ESD protection circuits under the bond pads, therefore, not only is wholly free from the traditional area consumption, but also can substantially relax design constraints, enabling much more flexible and robust ESD schemes for various applications.**

***Index Terms*—Copper metal, die cracking, ESD, fluorinated silicate glass, FSG, IMD, intermetal dielectric, low-k, stress mismatch, wire bonding.**

I. Introduction

AGGRESSIVELY scaled CMOS technologies have significantly driven integrated circuits design toward high-speed and high-performance applications. Owing to requirements for protection of internal circuits during handling and packaging, however, there exists a bottleneck around the I/O pads that ESD protection circuits can not be scaled proportionally as internal ones. Consequently, from generation to generation the traditional ESD protection circuits continue occupying a relatively large I/O region, and such area consumption significantly increases with increased growth of high pin count. Even a large area I/O pad itself can severely deteriorate the performance of the high-speed circuits. To alleviate these problems, moving ESD protection circuits under the bond pads seems to be a solution [1], as long as the manufacturability and reliability issues involved are met in advance: cracks due to bonding mechanical stress and thermal stress mismatch, induced device degradations, etc. The effectiveness of such solution is demonstrated in this paper in a 0.13 μm full eight-layer Cu metal/FSG low-k intermetal dielectric (IMD) CMOS process technology [2].

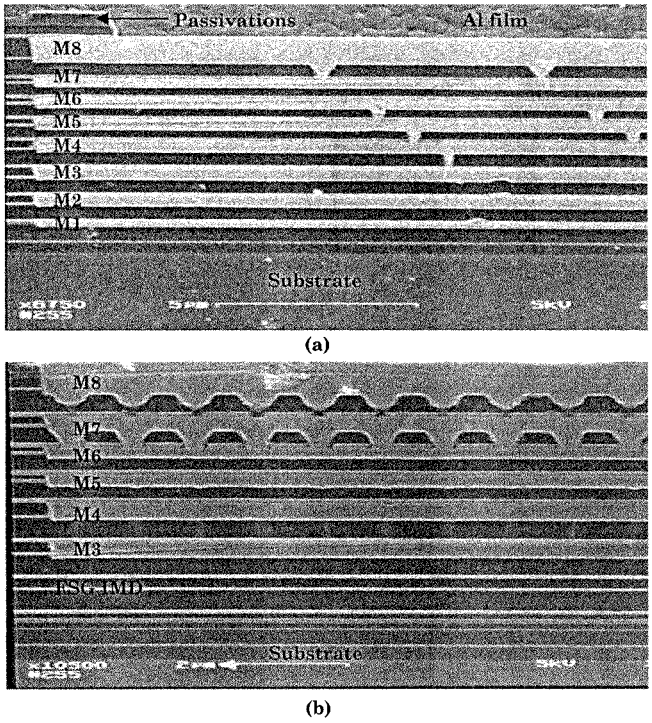

Fig. 1. SEM image of cross section of (a) a full eight-level metal I/O bond pad and (b) a six-level metal, metal-3 to metal-8, grounded-up bond pad.

II. Experimental

A 0.13 μm full eight-layer Cu metal/FSG low-k IMD CMOS process technology [2] can offer different combinations of metal layers such as a full eight levels metal bond pad and a single level metal band pad. The ESD protection device in this study was simple 4 shunted 2 cascaded NMOS transistors each with W/L = 15 μm/0.4 μm. The bond pad size was 70 μm $\times$ 70 μm. Fig. 1(a) shows SEM image of cross section of the eight-level metal I/O

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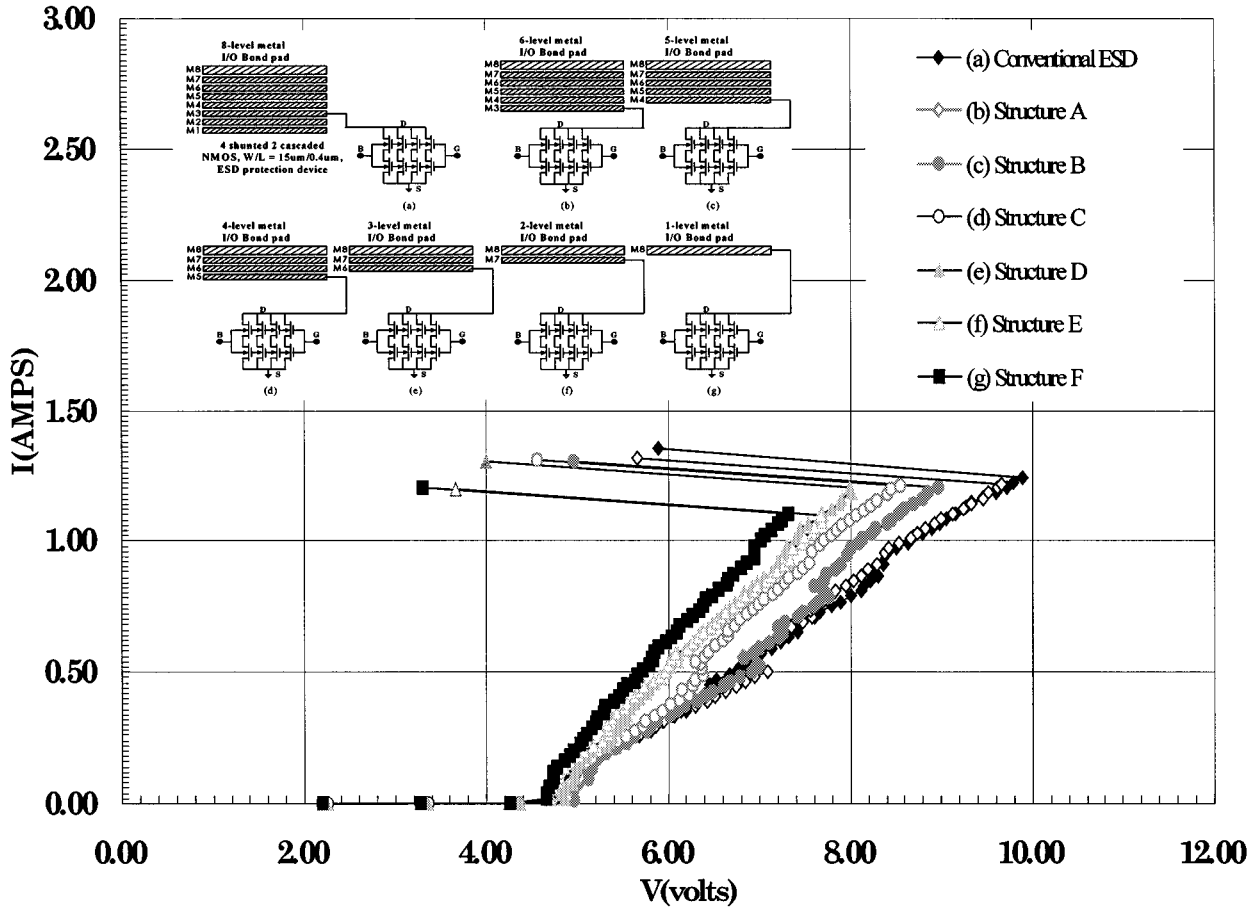

Fig. 2. I–V curves of the seven different structures obtained by TLP.

bond pad and Fig. 1(b) that of the six-level metal, metal-3 to metal-8, grounded-up I/O bond pad. A series of test structures were fabricated: 1) the ESD protection device with no band pad above, which is connected to a nearby conventional full eight levels metal bond pad, as schematically depicted in the inset of Fig. 2 for configuration (a); and 2) the ESD protection devices each under different metal stacks structures of the grounded-up bond pads, as all drawn for configuration (b) to (g) in the inset of Fig. 2. 12 kÅ Al metal film was deposited on 10 kÅ Cu top metal pad for Al wedge wire bonding with 100-mW bonding power and 20-g bonding force. Transmission line pulsing (TLP) technique with 100-ns pulse width was performed on the assembled test chips to build high current I–V from which the second breakdown trigger current I_{t2}, a measure of ESD robustness, and the second breakdown trigger voltage V_{t2} can all be gotten.

III. Results and Discussion

During Al wedge wire bonding, the ESD protection device under the bond pad experienced a high bonding power and force, then followed by SEM for physical inspection. No cracking phenomenon of the bond pad and the underlying IMD layers was found, as displayed in Fig. 1(b), relative to a full eight-level metal I/O bond pad in Fig. 1(a). In TLP experiment, a current pulse generated by discharging a charged transmission line was forced to enter into the device under test. By monitoring the current flowing through and the voltage on the pad, a high current I–V point was gotten; and adjusting current pulse height created more such points as shown in Fig. 2 for all structures. The I–V line (below the second breakdown trigger point) of structure F quite matches that of the conventional one [i.e., ESD protection device with no bond pad above as shown in configuration (a)], and even their second breakdown trigger points are very close to each other. This apparently evidences that the bonding power and force produces no change in the underlying lateral bipolar snapback high current properties.

Further analyzes point out that 1) I_{t2} depends very weakly on metal layers used and 2) V_{t2} increases with the number of metal layers. Thus, the constant I_{t2} is solely determined by the underlying protection device, regardless of pad structures used; and the certain junction power dissipation criterion can serve as the origin of such relationship. As for relatively significant dependencies of V_{t2}, it does not mean that the ESD protection device under the bond pad would be degraded. The mechanism responsible is the presence of the dynamic impedance of the metal layer stacks bond pad structures, and more metal layers yield more impedance values. Taking the equivalent RC circuit model of I/O bond pads into account, the impedance of a specified grounded-up I/O bond pad, Z_{pi}, can be written as

$$Z_{pi} = \sum_{n=i}^{8} R_{Mn} + \sum_{m=i+1}^{8} \int_0^t dt / C_{Mn,\,m-1} \qquad (1)$$

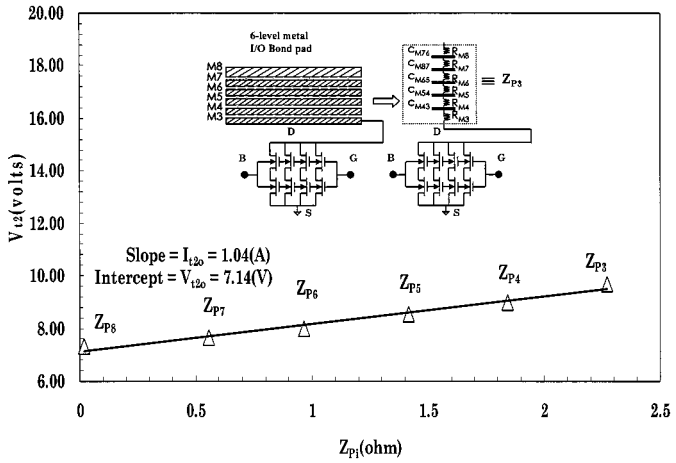

Fig. 3. Measured V_{t2} versus calculated impedance for structure A to F.

where R_{Mn} is the level metal resistance, $C_{Mm,m-1}$ is the capacitance between two metal layers, and the current pulse width is 100 ns in the work. The resulting impedance values are very low, ranging from 0.02 Ω to 2.27 Ω. Fig. 3 displays the measured V_{t2} versus calculated impedance for structure A to F. Strikingly, a linear relationship is built between the two. In particular, the slope and intercept of the line provides relevant information for the underlying ESD protection devices: the intrinsic second breakdown trigger current $I_{t2o}(= 1.04$ A) and voltage $V_{t2o}(=$ 7.14 V). Since I_{t2}, a measure of ESD robust ability, shows weak dependency on bond pads, structure A to F features comparable ESD immunity each other. This indicates that moving ESD protection circuits under the bond pads proves reliable in our work. Therefore, it is argued that not only the traditional area consumption can be avoided, but also design constraints for I/O pads can be substantially relaxed. This enables much more flexible and robust ESD schemes such as a distributed ESD protection one [3]. Promising potential can be further expected in the microprocessor and ASIC applications where high-level ESD protection is essential [4].

IV. Conclusion

The ESD protection devices under the grounded-up bond pads have been successfully realized in 0.13 μm full eight-level Copper metal/FSG low-k IMD CMOS technology. The underlying mechanism has been clarified and the promising potential has been projected. The impact of other parameters such as metal thickness or metal linewidth on the ESD performances, which would provide practical condition for reliability and manufacturability issues, will be further researched.

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