Post-Soft-Breakdown Characteristics of Deep Submicron NMOSFETs with Ultrathin Gate Oxide

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***Abstract*—The impacts of soft-breakdown (SBD) on the characteristics of deep sub-micron NMOSFETs were investigated. It is shown that the BD location plays a crucial role in the post-BD switching function of the device. When BD occurs at the channel, the turn-on behavior of the drain current would not be significantly affected, which is in strong contrast to the case of BD at the drain. Nevertheless, significant increase in gate current is observed in the off-state when the gate voltage is more negative than −1 V. Its origin is identified to be due to the action of two parasitic bipolar transistors formed after SBD occurrence at the channel.**

***Index Terms*—Gate induced drain leakage, gate leakage, parasitic bipolar transistor, soft-breakdown.**

I. Introduction

SOFT-BREAKDOWN (SBD) events are frequently observed as oxide is thinner than 5 nm [1]–[7]. One interesting feature associated with this BD mode is that the device switching behavior may be retained even after its occurrence, in strong contrast to the case of conventional hard breakdown (HBD) [3]. In addition, impacts of SBD on device characteristics also depend on the BD location. For example, Pompl *et al.* [4] reported that, when SBD occurs within the gate/drain overlap region, gate induced drain leakage (GIDL) current will be increased. On the other hand, Wu *et al.* [5] observed that the gate leakage, rather than the GIDL, dominates the off-state drain current when BD is induced in the drain region. Their results also indicated that the device's switching function could be destroyed, if BD occurs at the drain. In order to distinguish the disparity among different reports, we characterized the post-SBD characteristics of deep submicron n-channel devices in this study. Special attention was paid to the effects of BD location and their impacts on the device performance, especially the off-state leakage characteristics.

II. Experimental

N-channel MOS transistors with n^+ poly-Si gate were fabricated on 6-inch Si wafers. Nominal gate oxide thickness and channel length/width are 2.5 nm and 0.2/10 μm, respectively. Electrical characterizations were performed using a HP-4156

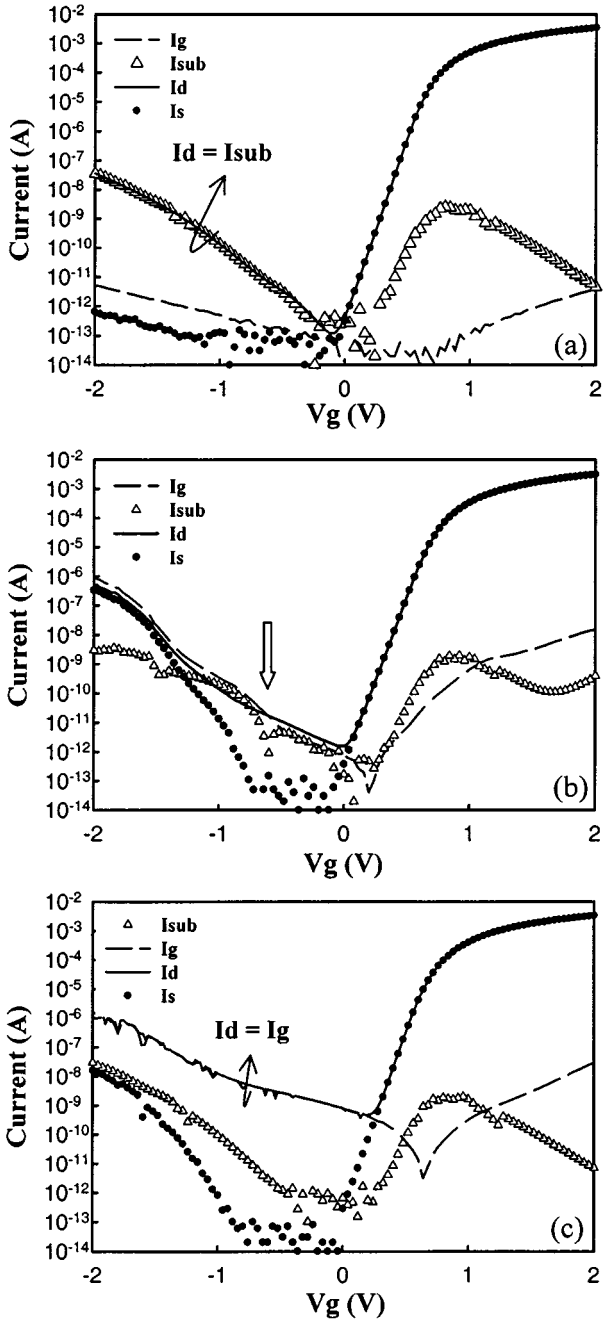

Fig. 1. Current–voltage characteristics of (a) a fresh device, and devices with first SBD event occurs (b) within the channel, and (c) at the drain. ($V_d = 1.5$ V). The arrow in (b) indicates the point where the substrate current flow reverses its direction.

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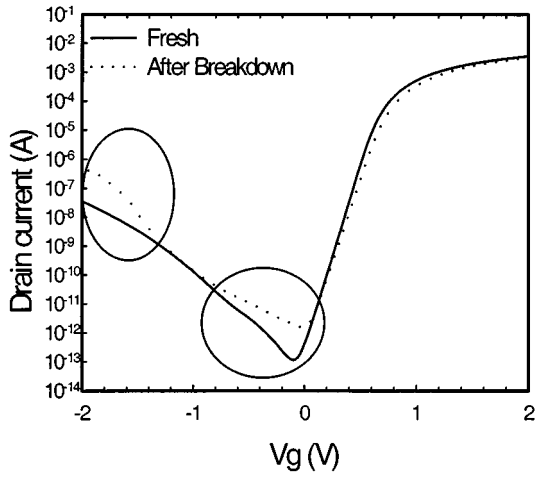

Fig. 2. I_d–V_g characteristics of a device before and after BD occurs within the channel.

parameter analyzer. Some devices were stressed at room temperature under a gate bias of -4.5 V with all other terminals (i.e., source, drain, and substrate) grounded. Device characteristics before and after BD were measured and analyzed.

III. Results and Discussion

Occurrence of the first soft breakdown (SBD) event in oxide could be located at the drain, source, or the channel region of a device. In [5], it was shown that most BD events would be induced in the source/drain overlapped region for deep sub-micron devices. In this work, similar trend was observed. Nevertheless, we have indeed detected all these types of BD events. Fig. 1(a)–(c) show typical characteristics of fresh device, BD at the channel, and BD at the drain, respectively. In Fig. 1(b), the substrate current changes its sign (i.e., flow direction) at $V_g \sim -0.7$ V (highlighted by the arrow in the figure), indicating that the BD location is within the channel region. In Fig. 1(c), BD occurs at the drain, since I_g coincides with I_d in the off-state. As can be seen in Fig. 1, when BD occurs at the channel, the subthreshold and on-state characteristics of the drain current are not significantly affected. In contrast, BD at the drain would increase dramatically the off-state drain current, severely degrading the device switching behavior [5].

For devices with BD at the channel, as mentioned above, the tun-on behaviors will not be significantly affected. When the off-state I_d characteristics after BD are compared with those of the fresh devices, however, it is interesting to find that two regions, one in the range from $0 \geq V_g \geq -0.8$ V and the other with $V_g < -1.2$ V, show increased I_d, as illustrated in Fig. 2. The I_d increase in the range from $0 \geq V_g \geq -0.8$ V is also observed before BD is induced. By carefully analyzing I_d and I_{sub} characteristics in the V_g range of interest as a function of stressing time (data not shown), it is concluded that the I_d increase after stressing is mainly contributed by the increased I_{sub}. The other contribution is from the gate leakage, albeit minor. One possible explanation is that the stressing would increase the interface-state density, and thus enhance the trap-assisted gate-induced drain leakage (GIDL), ΔI_{sub}, and the stress-induced leakage currents (SILC), ΔI_g [8].

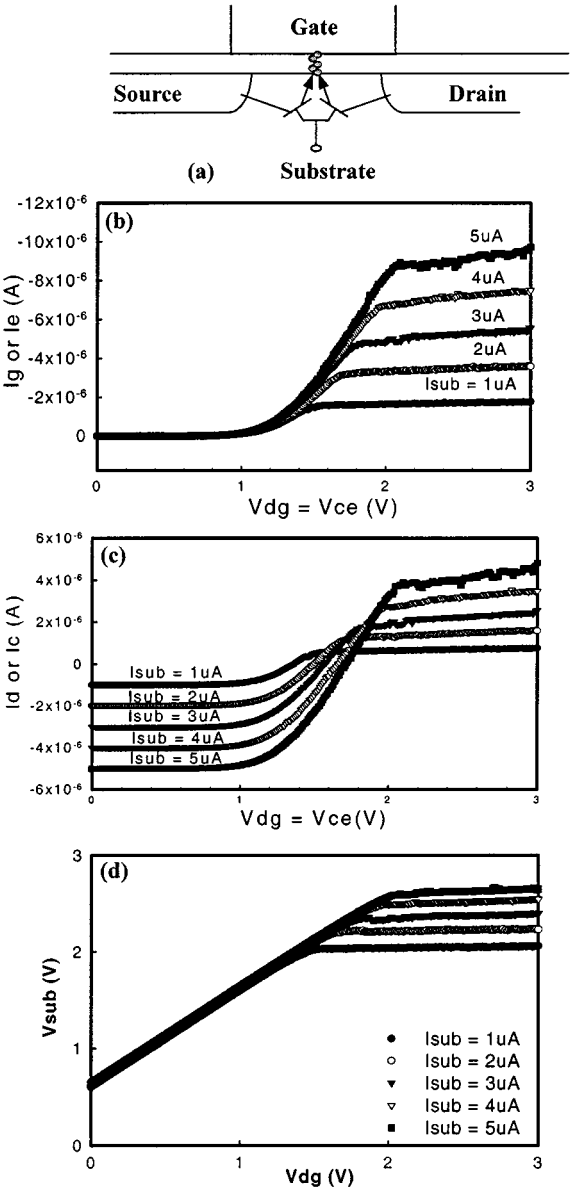

Fig. 3. (a) Formation of two parasitic bipolar junction transistors (BJTs) after BD occurs within the channel. Results in (b)–(d) are characteristics of the drain-side BJT characterized with common-emitter scheme (i.e., $V_g = 0$ and source floating). The device is the same as that shown on Fig. 1(b).

On the other hand, the increase in I_d after SBD for $V_g < -1.2$ V is believed to be due to the action of the parasitic bipolar transistors formed after SBD. When BD occurs at the channel, two parasitic npn bipolar transistors would be formed in the substrate, as shown in Fig. 3(a). The two transistors share a common base (i.e., substrate) and a common emitter (i.e., n^+ poly-Si), but with separate collectors (i.e., drain and source, respectively). In this work, the action of the bipolar transistor is clearly demonstrated. One example is shown in Fig. 3. Here, only the drain-side bipolar transistor was characterized by floating the source during measurement. Fig. 3(b) and (c) show I_g (or I_e) and I_d (or I_c) as a function of V_{dg} (or V_{ce}), respectively. The measurements were performed with the common-emitter configuration, i.e., $V_g = 0$. Base (substrate) current is used as the input parameter. We can see that the

device is essentially operating in the saturation region when V_{dg} is smaller than 2 V, as evidenced by the results shown in Fig. 3(d) in which V_{sub} is larger than both V_d and V_g. This indicates that both the emitter-base and the base-collector junctions are forward-biased. On the other hand, the device will be operating in the active mode when V_{dg} is larger than 2 V, so the base-collector junction becomes reverse-biased. The large offset in the V_{ce} axis is mainly ascribed to the large parasitic emitter resistance, due to the small area of BD spot [9].

For the current–voltage characteristics of the device with BD spot located within the channel region [Figs. 1(b) and Fig. 2], the parasitic bipolar transistors would be triggered into the active mode in the negative gate voltage region when $|V_g|$ is large enough. As a result, the drain current would be amplified, resulting in the I_d increase in the large negative V_g region, as observed.

Note that the enhanced GIDL phenomenon after the occurrence of SBD reported in [4] is not detected in this work. The enhanced GIDL could be observed only in the small V_g range before the SBD is induced. This discrepancy is presumably related to the thicker gate oxide used in the previous work [4] (3 and 4 nm), and implies that the SBD mechanism could be different as oxide is scaled below 3 nm.

IV. Conclusions

In summary, we have investigated the post-SBD characteristics of n-channel MOSFETs with 2.5 nm-thick gate oxide. Several important findings are obtained. 1) The BD location plays an important role in affecting the switching function of the device. If BD occurs at the drain, significant leakage form the gate would destroy the normal operation of the device. 2) During stressing, enhanced GIDL and SILC gate currents caused by the generated interface states account for the increased drain leakage in the small negative V_g range. 3) When BD occurs in the channel, large increase in I_d for $V_g < -1.5$ V is identified to be due to the action of the parasitic npn transistors.

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